University of Michigan – Shanghai Jiao Tong University Joint Institute
Center of Optics and Optoelectronics

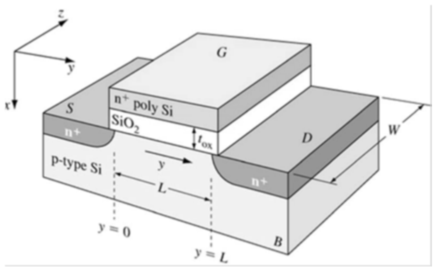
VE 320 – Summer 2012
Introduction to Semiconductor Device

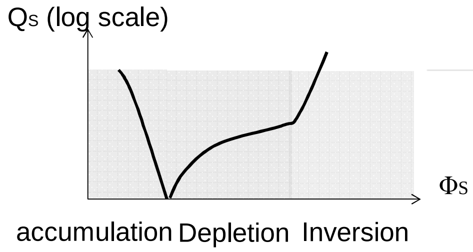
MOSFET I-V Characteristics

Instructor: Professor Hua Bao

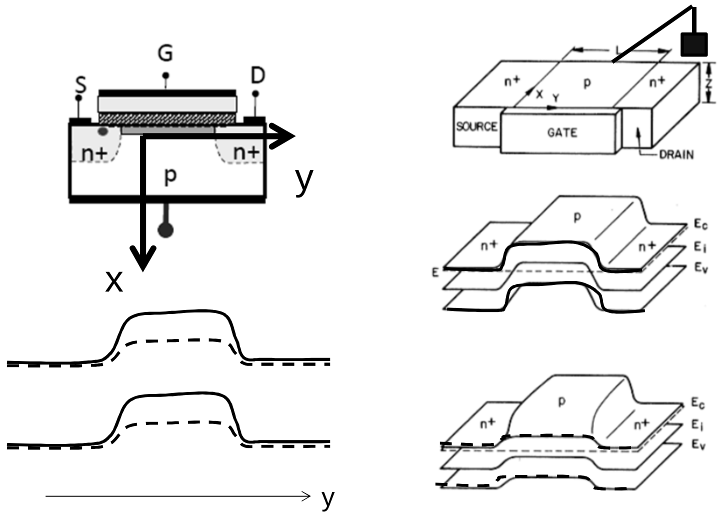
MOSFET Operation: Qualitative

Control current flow between source/drain by gate potential

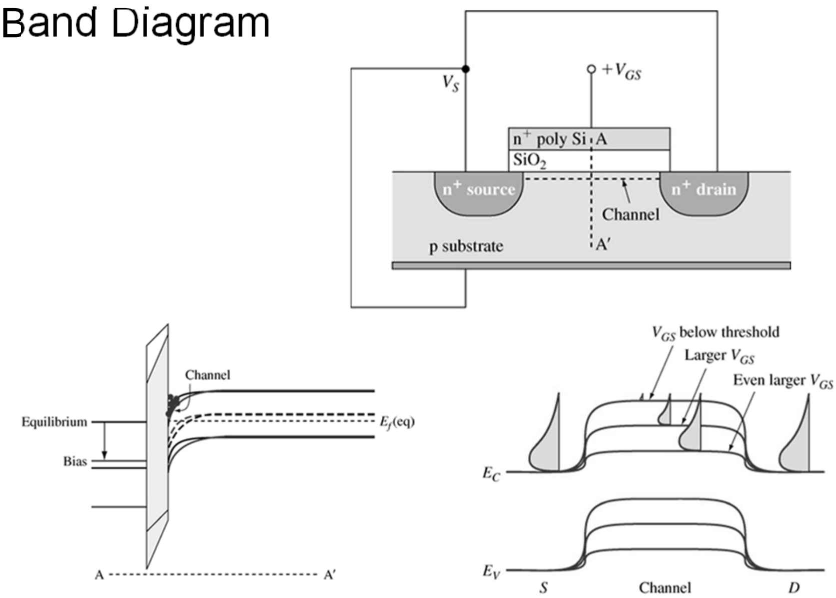




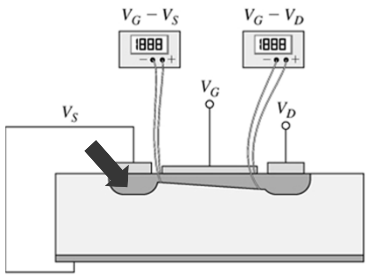
2D Band Diagram

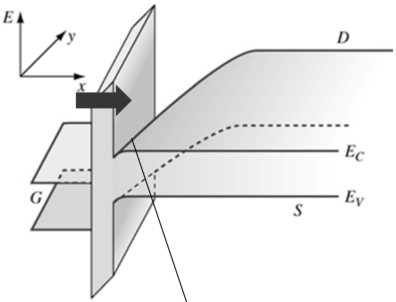


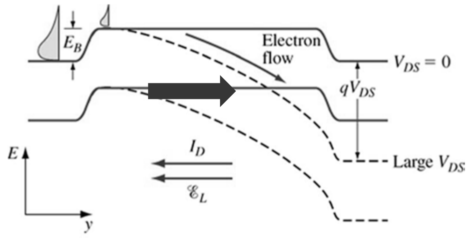
Band Diagram

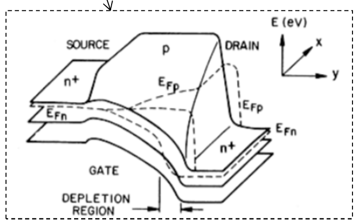


Under Bias



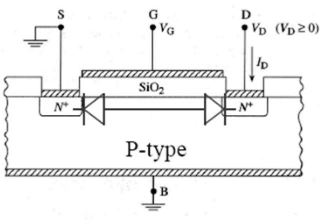




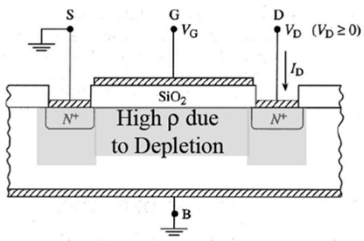


MOSFET, OFF State

Accumulation $V_G < 0$



Depletion $0<V_G<V_T$



Device is off for $V_G< V_T$

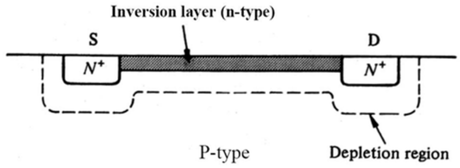
Threshold voltage, V_T, is the V_G at the onset of inversion.

For n-channel device (p-bulk) $$V_T = 2\phi_F + \frac{K_S x_o}{K_O}\sqrt{\frac{4qN_A}{K_S\varepsilon_0}\phi_F}$$

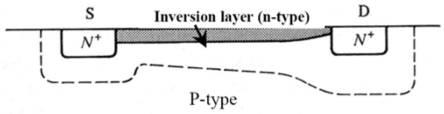
For p-channel device (n-bulk) $$V_T = 2\phi_F - \frac{K_S x_o}{K_O}\sqrt{\frac{4qN_A}{K_S\varepsilon_0}(-\phi_F)}$$

MOSFET, Linear Region

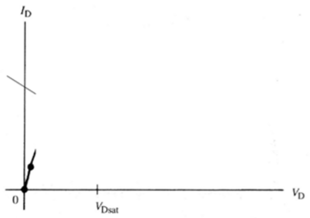
$V_G > V_T$
$V_D = 0$



$V_G > V_T$
V_D small



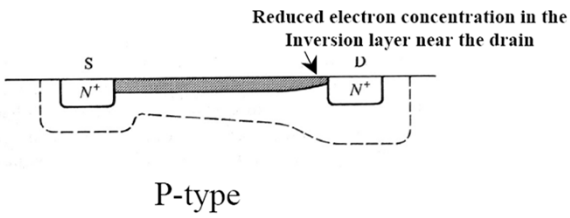
Linear region

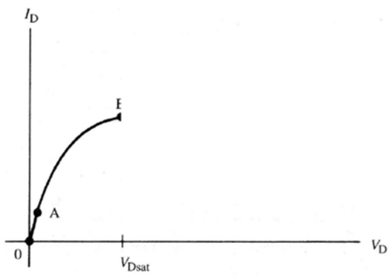


- **Low V_D**
- **Channel resistance determined by inversion charge, controlled by V_G**

MOSFET, Linear Region

$V_G > V_T$
$V_D > 0$

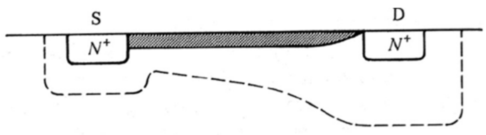




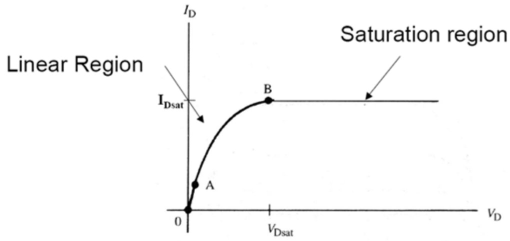
Depletion width and inversion charge varies along channel at larger V_D

MOSFET Saturation

$V_G > V_T$
$V_D = V_{sat}$



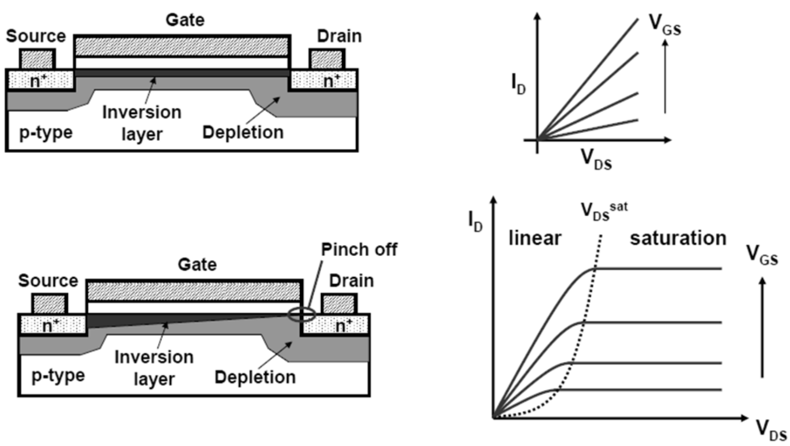
Channel pinches off at larger V_D (V_{sat})



V_{Dsat} = saturation voltage = V_{GS}-V_T

Question: after pinch-off, why we can still get current?

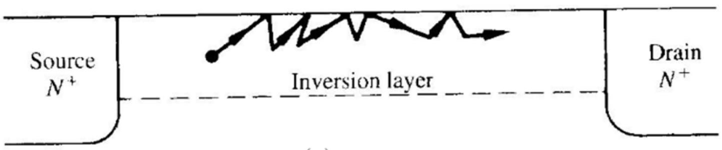
Qualitative I-V Characteristics



Larger V_G, larger conductance, larger V_{Dsat}

Before Quantitative Analysis…

The electrons are constantly colliding with the surface…



$$\bar{\mu}_n = \frac{\int_0^{x_c(y)} \mu_n(x,y) n(x,y)\, dx}{\int_0^{x_c(y)} n(x,y)\, dx}$$

Define $$Q_N(y) = -q \int_0^{x_c(y)} n(x,y)\, dx$$

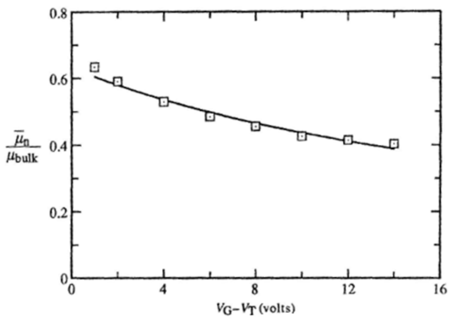
$$\Rightarrow \quad \bar{\mu}_n = -\frac{q}{Q_N(y)} \int_0^{x_c(y)} \mu_n(x,y) n(x,y)\, dx$$

Here we consider effective mobility as a device parameter independent of V_D

Effective Mobility

Effective mobility has a dependence on gate voltage.
Larger gate voltage brings electrons closer to the oxide.

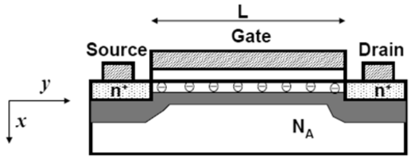
Empirical relationship $$\bar{\mu}_n = \frac{\mu_0}{1 + \theta(V_G - V_T)}$$



Note that this is just for one device, and should not the generalized.

Current

- Current flow in y-direction
- Neglect carrier diffusion



$$J_N \approx J_{Ny} \approx q\mu_n n \mathscr{E}_y = -q\mu_n n \frac{d\phi}{dy}$$

$$I_D = -\int\int J_{Ny} dx dz = \left(-Z\frac{d\phi}{dy}\right)\left(-q\int_0^{x_c(y)} \mu_n(x,y)n(x,y)dx\right)$$

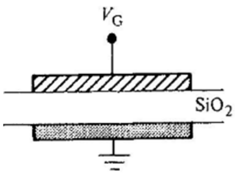
$$I_D = -Z\bar{\mu}_n Q_N \frac{d\phi}{dy}$$

Current Invariant $\displaystyle \int_0^L I_D dy = I_D L = -Z\int_0^{V_D} \bar{\mu}_n Q_N d\phi$

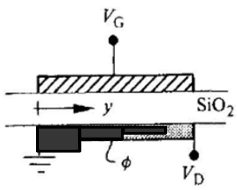
$$I_D = -\frac{Z\bar{\mu}_n}{L}\int_0^{V_D} Q_N d\phi$$

All we need to do is to find Q_N

Square Law Theory



MOS-C



MOSFET

Assume the MOS is a parallel capacitor

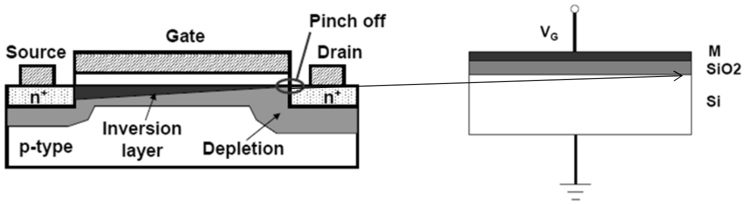
$$Q_N \approx -C_o(V_G - V_T) \qquad C_o \equiv \frac{C_O}{A_G} = \frac{K_O\varepsilon_0}{x_o}$$

There is voltage drop along y axis, therefore…

$$Q_N(y) \approx -C_o(V_G - V_T - \phi) \quad \Rightarrow \quad I_D = \frac{Z\bar{\mu}_n C_o}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right]$$

$$I_D = -\frac{Z\bar{\mu}_n}{L}\int_0^{V_D} Q_N d\phi \qquad (\ 0 \le V_D \le V_{Dsat} \quad V_G \ge V_T\ )$$

Saturation Current



$$Q_N(L) \rightarrow 0 \quad \text{when} \quad \phi(L) = V_D \rightarrow V_{Dsat}$$

Drain voltage removes the effect of gate voltage on the capacitor

$$V_{Dsat} = V_G - V_T$$

$$I_{Dsat} = \frac{Z\bar{\mu}_n C_o}{2L}(V_G - V_T)^2$$

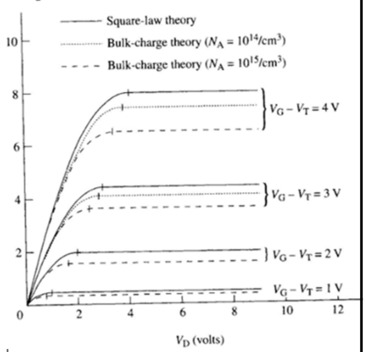
Bulk Charge Theory

Depletion width varies with y …

$$Q_N(y) = -C_o(V_G - V_T - \phi) + qN_A[W(y) - W_T]$$

$$W(y) = \left[\frac{2K_S\varepsilon_0}{qN_A}(2\phi_F + \phi)\right]^{1/2}$$

$$W_T = \left[\frac{2K_S\varepsilon_0}{qN_A}(2\phi_F)\right]^{1/2}$$

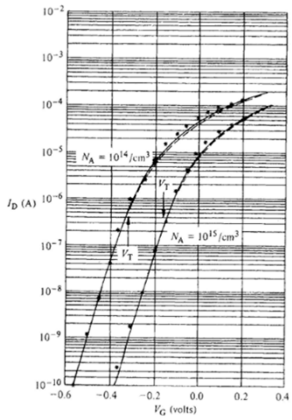


$$I_D = \frac{Z\bar{\mu}_n C_o}{L}\left\{(V_G - V_T)V_D - \frac{V_D^2}{2} - \frac{4}{3}V_W\phi_F\left[\left(1 + \frac{V_D}{2\phi_F}\right)^{3/2} - \left(1 + \frac{3V_D}{4\phi_F}\right)\right]\right\}$$

for $0 \le V_D \le V_{Dsat}$ (17.28)
and $V_G \ge V_T$

Limitations

- The charge in MOSFET is assumed to be zero. Actually a residue drain current flows in the sub threshold regime.
- Both theories do not self-saturate- it is necessary to artificially construct the saturation current.
- Other theories like charge-sheet and exact-charge theory.



Summary

- MOSFET differs from MOSCAP in that the field from the S/D contacts now causes a current to flow.
- Two regimes, diffusion-dominated subthreshold and drift-dominated super-threshold characteristics, define the I_D-V_D-V_G characteristics of a MOSFET.
- We can use simple square law theory or bulk charge theory to describe the I-V characteristics, but there are also limitations.