

五、目标代码生成

(1. RISC-V 概述)

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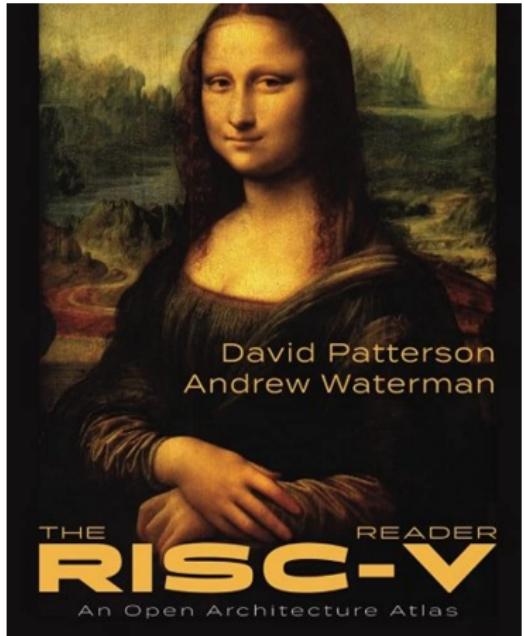
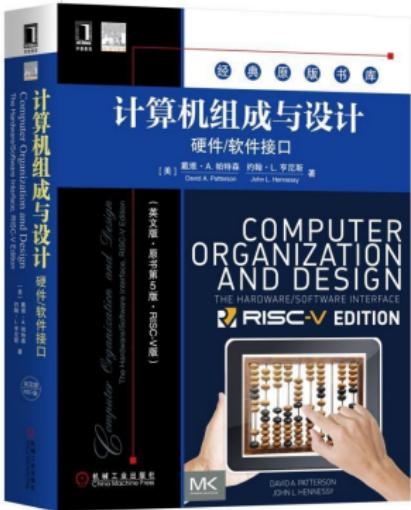




David Andrew Patterson (1947 ~)



“Hennessy and Patterson created a systematic and quantitative approach to designing faster, lower power, and **reduced instruction set computer (RISC)** microprocessors.”





2019 年国际芯片大会



“未来 *RISC-V* 很可能发展成为世界主流 *CPU*之一，
从而在 *CPU* 领域形成 *Intel*、*ARM*、*RISC-V* 三分天下的格局。
”

— 中国工程院院士 倪光南

RISC-V Assembly Language Programming

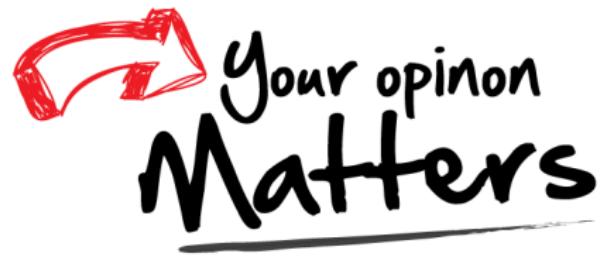
Using the ESP32-C3 and QEMU



Warren Gay



Thank You!



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