五、目标代码生成
(13. RISC-V 概述)

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2024 年 05 月 24 日

RISC: Reduced Instruction Set Computer (精简指令集计算机)

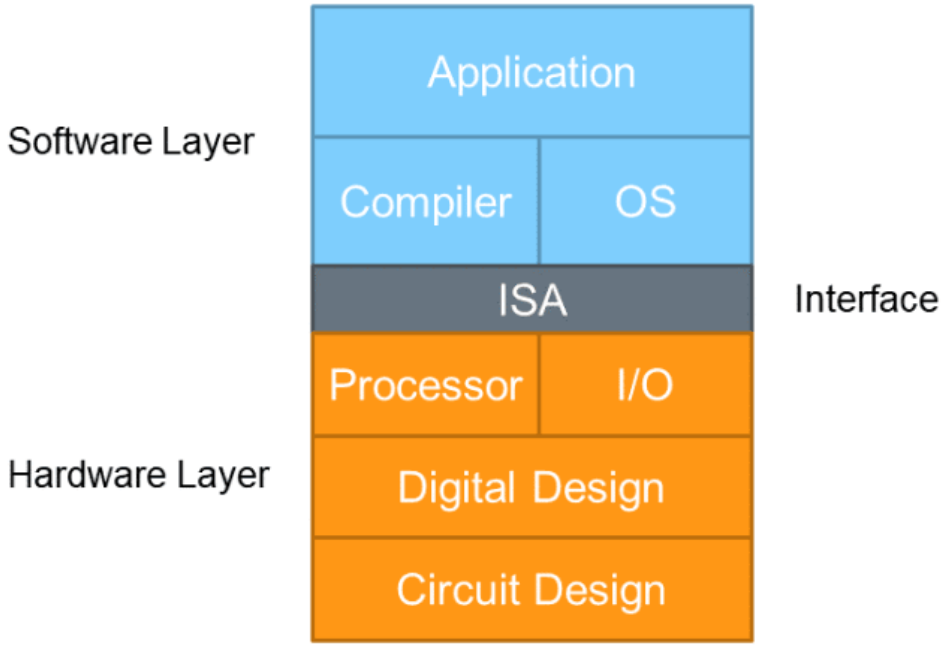
V: Five

CISC: Complex Instruction Set Computer (复杂指令集计算机)

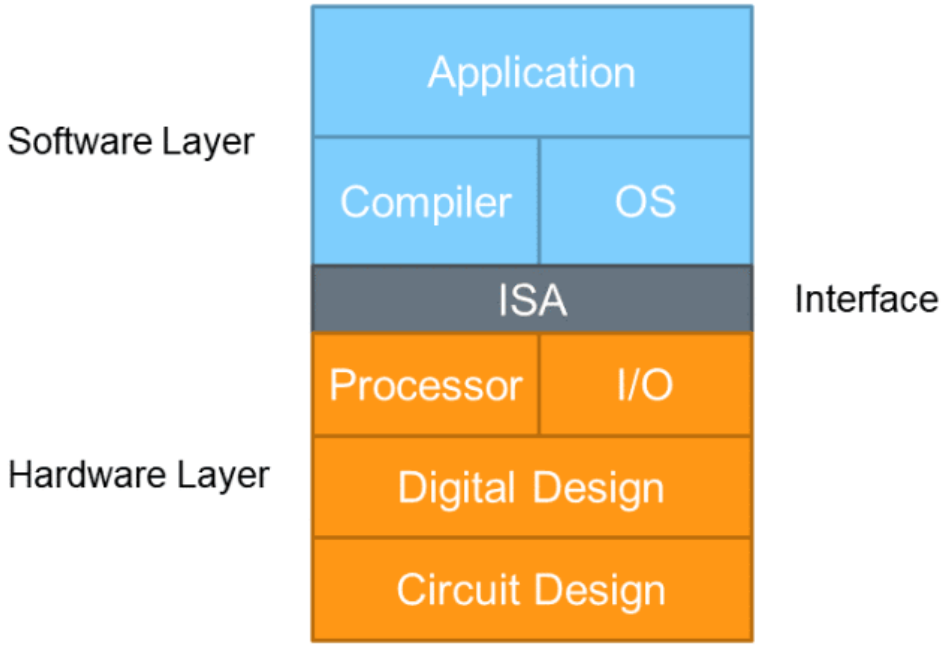
RISC: Each instruction performs only one function.

CISC: `SUBL val, %eax ;` `%eax <- %eax - val`

ISA (Instruction Set Architecture) as the Software/Hardware Interface



ISA (Instruction Set Architecture) as the Software/Hardware Interface

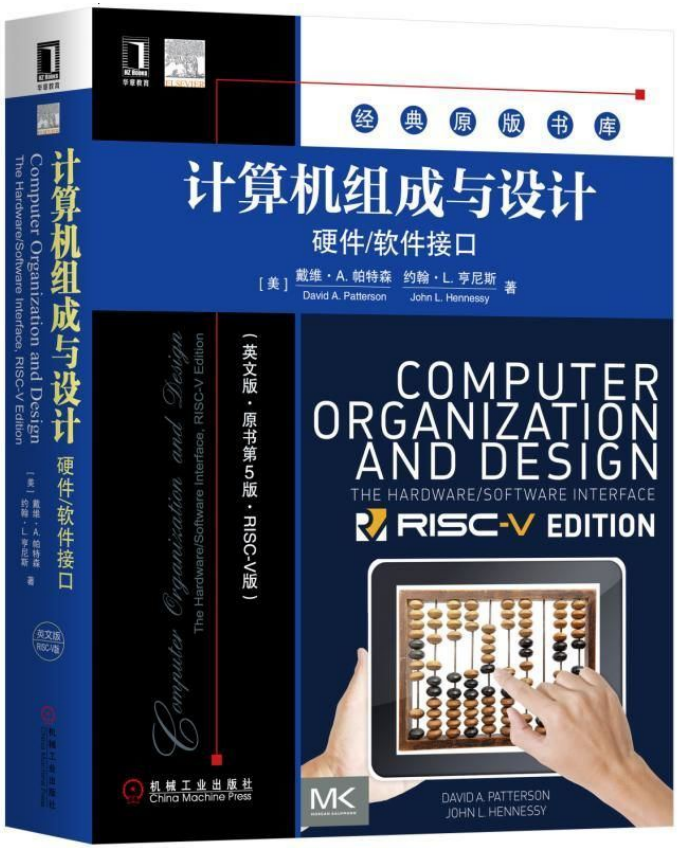


In general, an ISA defines the supported instructions, data types, registers, the hardware support for managing main memory, fundamental features (such as the memory consistency, addressing modes, virtual memory), and the input/output model of a family of implementations of the ISA.

Krste Asanović at the University of California, Berkeley, had a research requirement for an open-source computer system, and in 2010 he decided to develop and publish one in a "short, three-month project over the summer" with several of his graduate students. The plan was to aid both academic and industrial users.[12] David Patterson at Berkeley joined the collaboration as he was the originator of the Berkeley RISC,[18] and the RISC-V is the eponymous fifth generation of his long series of cooperative RISC-based research projects at the University of California, Berkeley (RISC-I and RISC-II published in 1981 by Patterson, who refers[21] to the SOAR architecture[22] from 1984 as "RISC-III" and the SPUR architecture[23] from 1988 as "RISC-IV"). At this stage, students provided initial software, simulations, and CPU designs.[24]

2017 ACM Turing Award

"Hennessy and Patterson created a systematic and quantitative approach to designing faster, lower power, and **reduced instruction set computer (RISC)** microprocessors."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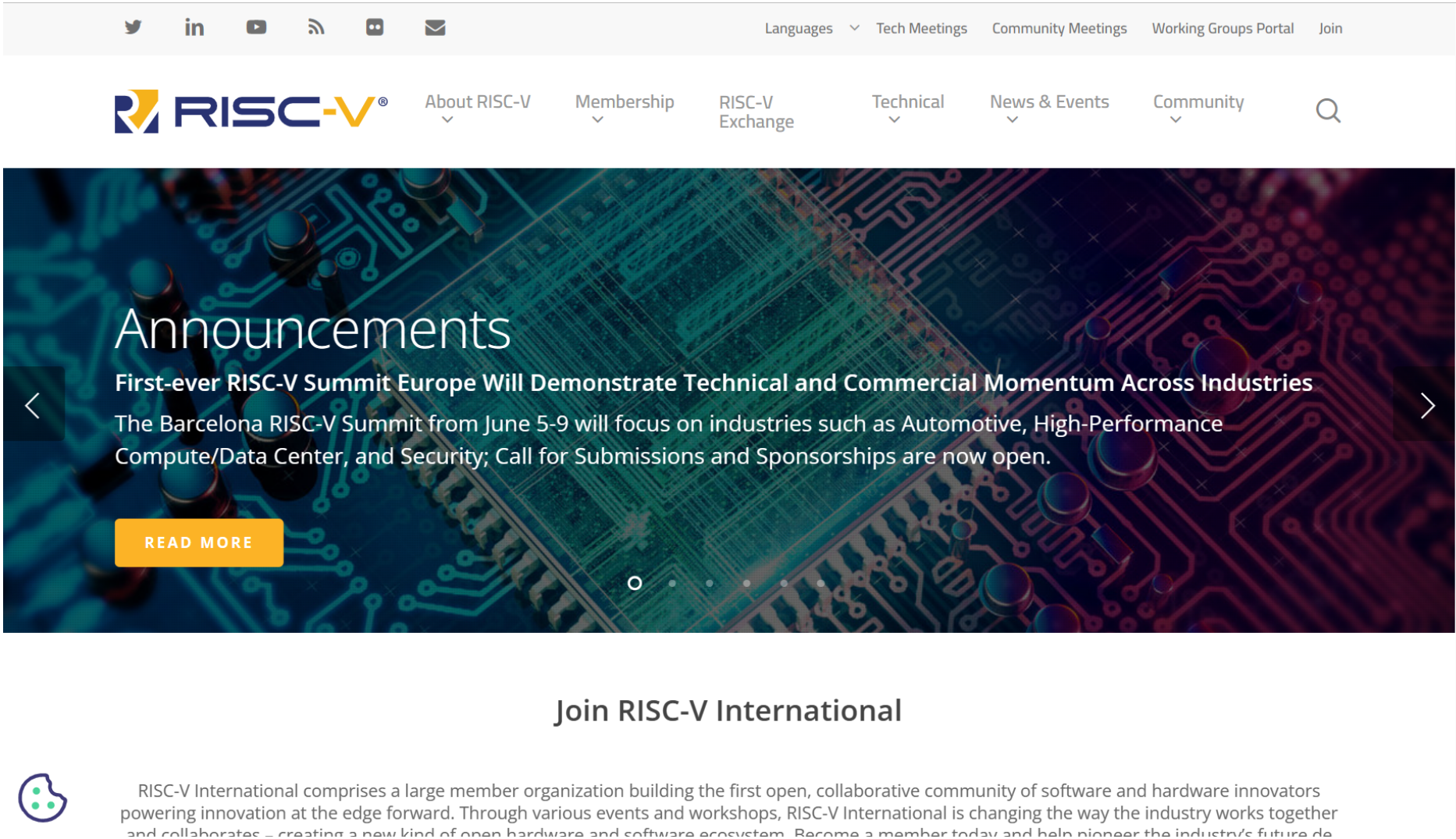
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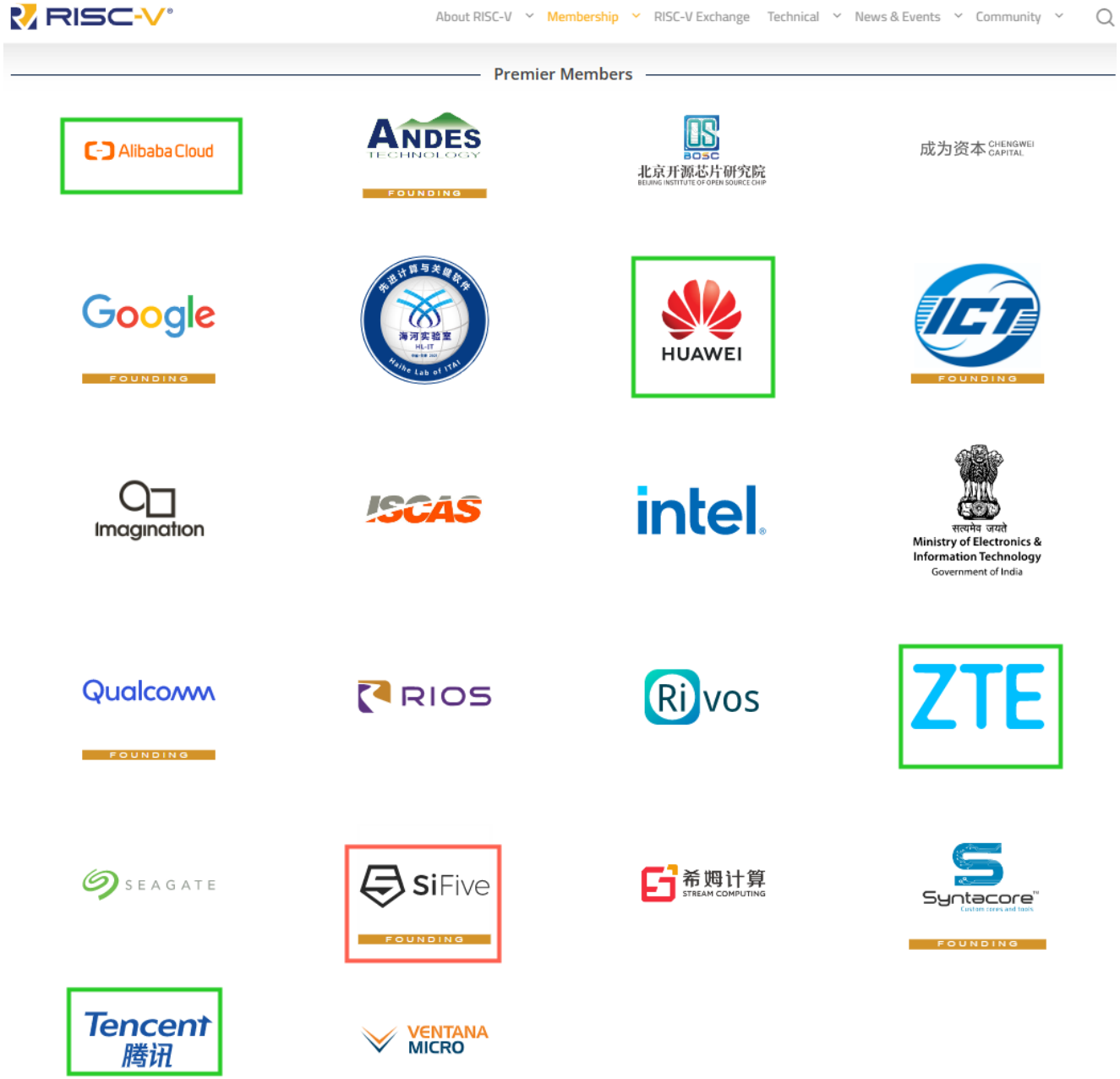
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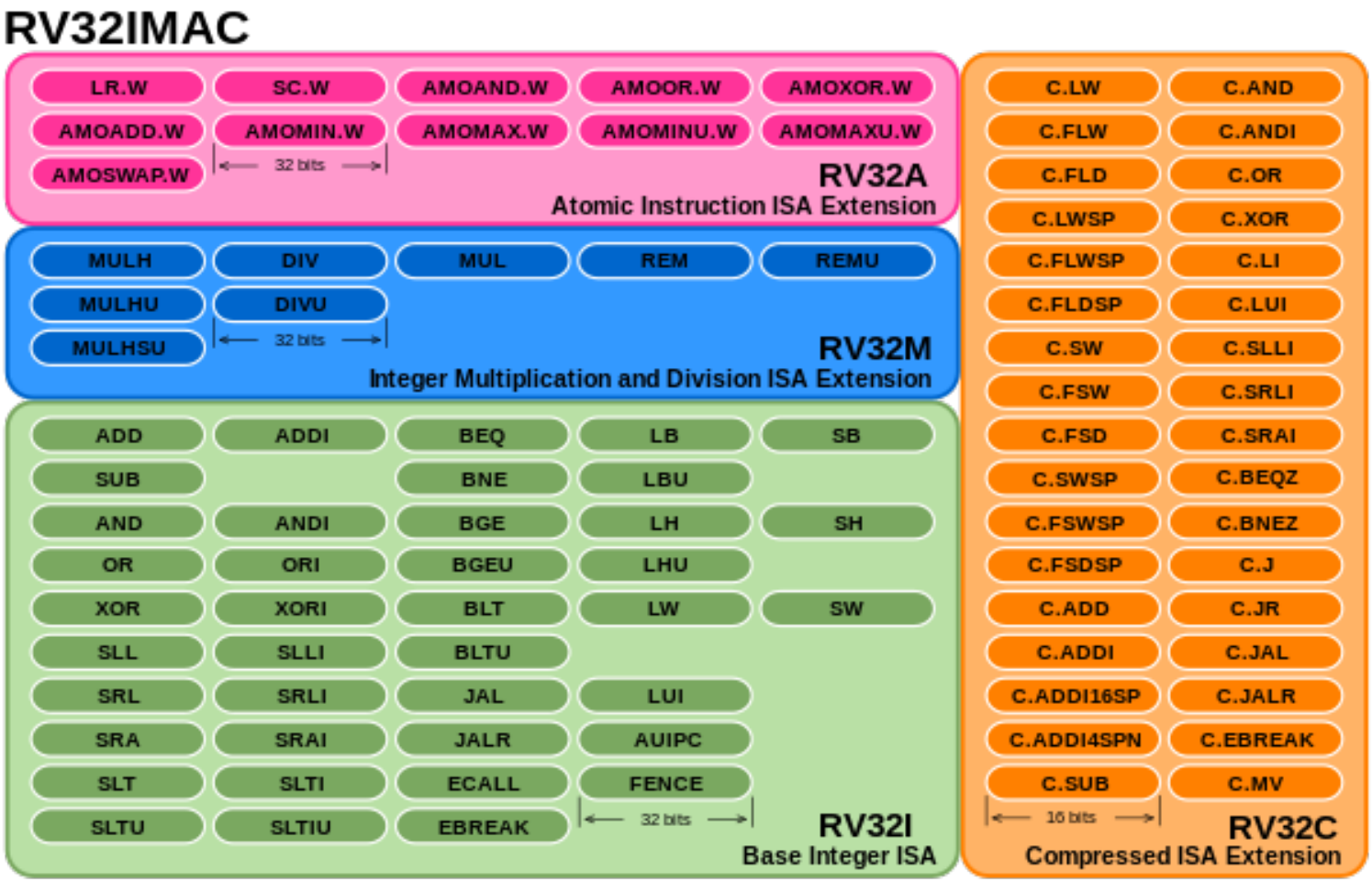
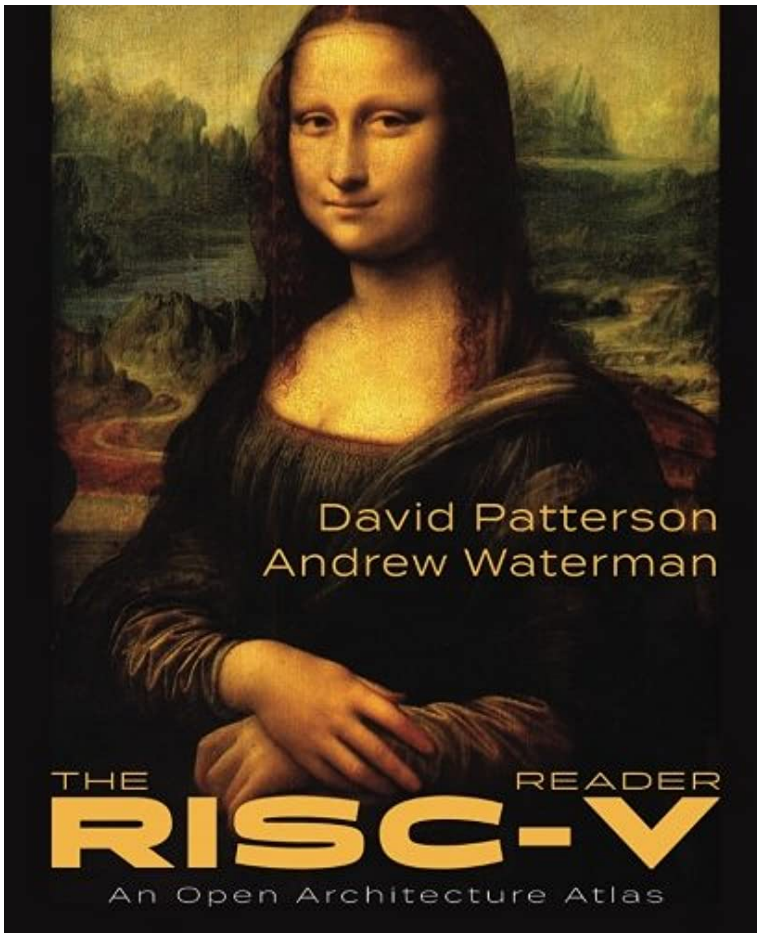
菜单 (**模块式**; RISC-V)


RV32IMAC
LR.W
SC.W
AMOAND.W
AMOOR.W
AMOXOR.W
AMOADD.W
AMOMIN.W
AMOMAX.W
AMOMINU.W
AMOMAXU.W
AMOSWAP.W
32 bits
RV32A
Atomic Instruction ISA Extension
MULH
DIV
MUL
REM
REMU
MULHU
DIVU
MULHSU
32 bits
RV32M
Integer Multiplication and Division ISA Extension
ADD
ADDI
BEQ
LB
SB
SUB
BNE
LBU
AND
ANDI
BGE
LH
SH
OR
ORI
BGEU
LHU
XOR
XORI
BLT
LW
SW
SLL
SLLI
BLTU
SRL
SRLI
JAL
LUI
SRA
SRAI
JALR
AUIPC
SLT
SLTI
ECALL
FENCE
SLTU
SLTIU
EBREAK
32 bits
RV32I
Base Integer ISA
C.LW
C.AND
C.FLW
C.ANDI
C.FLD
C.OR
C.LWSP
C.XOR
C.FLWSP
C.LI
C.FLDSP
C.LUI
C.SW
C.SLLI
C.FSW
C.SRLI
C.FSD
C.SRAI
C.SWSP
C.BEQZ
C.FSWSP
C.BNEZ
C.FSDSP
C.J
C.ADD
C.JR
C.ADDI
C.JAL
C.ADDI16SP
C.JALR
C.ADDI4SPN
C.EBREAK
C.SUB
C.MV
16 bits
RV32C
Compressed ISA Extension

2019 年国际芯片大会

“RISC-V 很可能发展成为世界主流 CPU 之一, 在 CPU 领域形成 Intel、ARM、RISC-V 三分天下的格局。” — 中国工程院院士　倪光南

大道至简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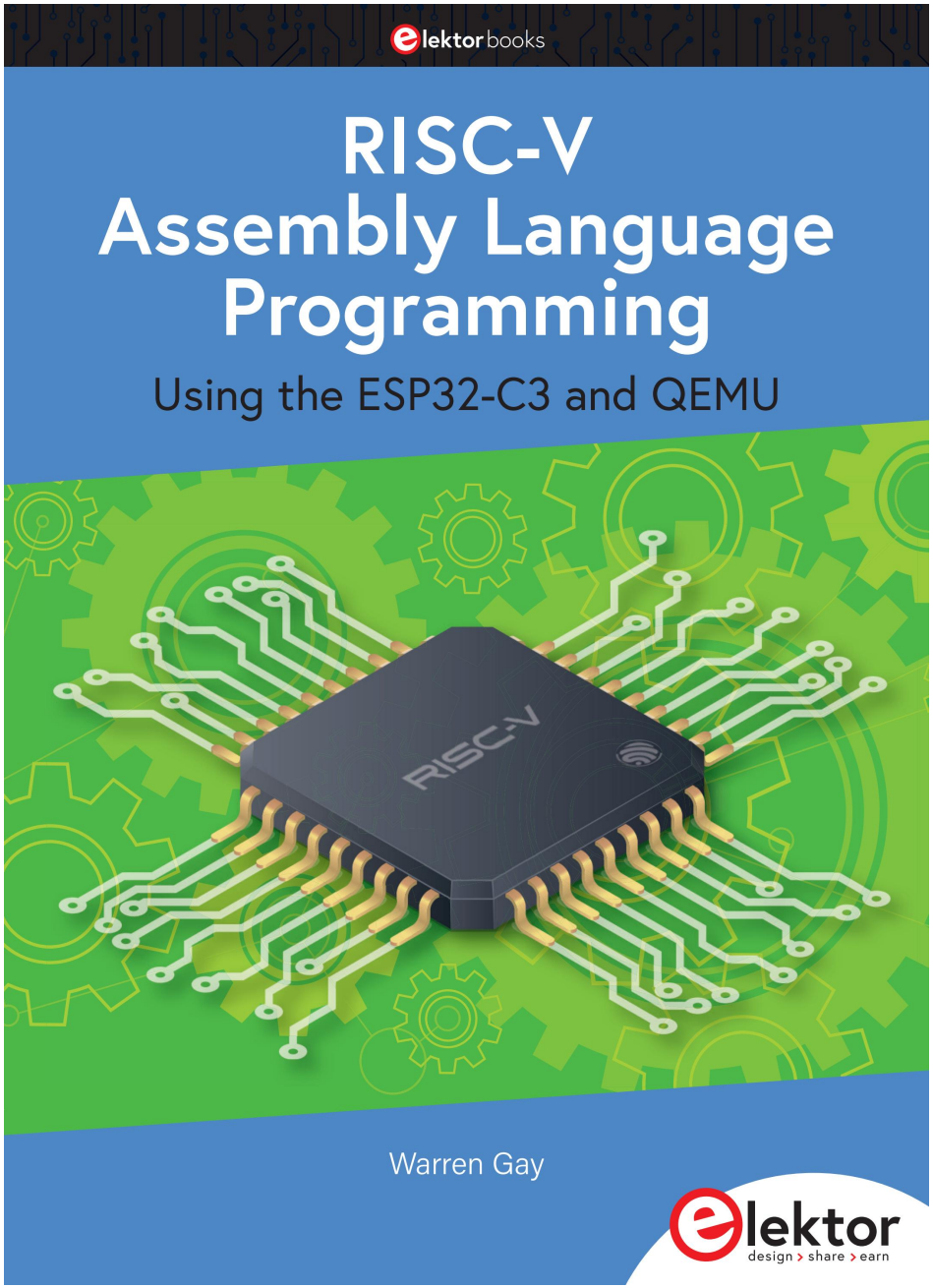
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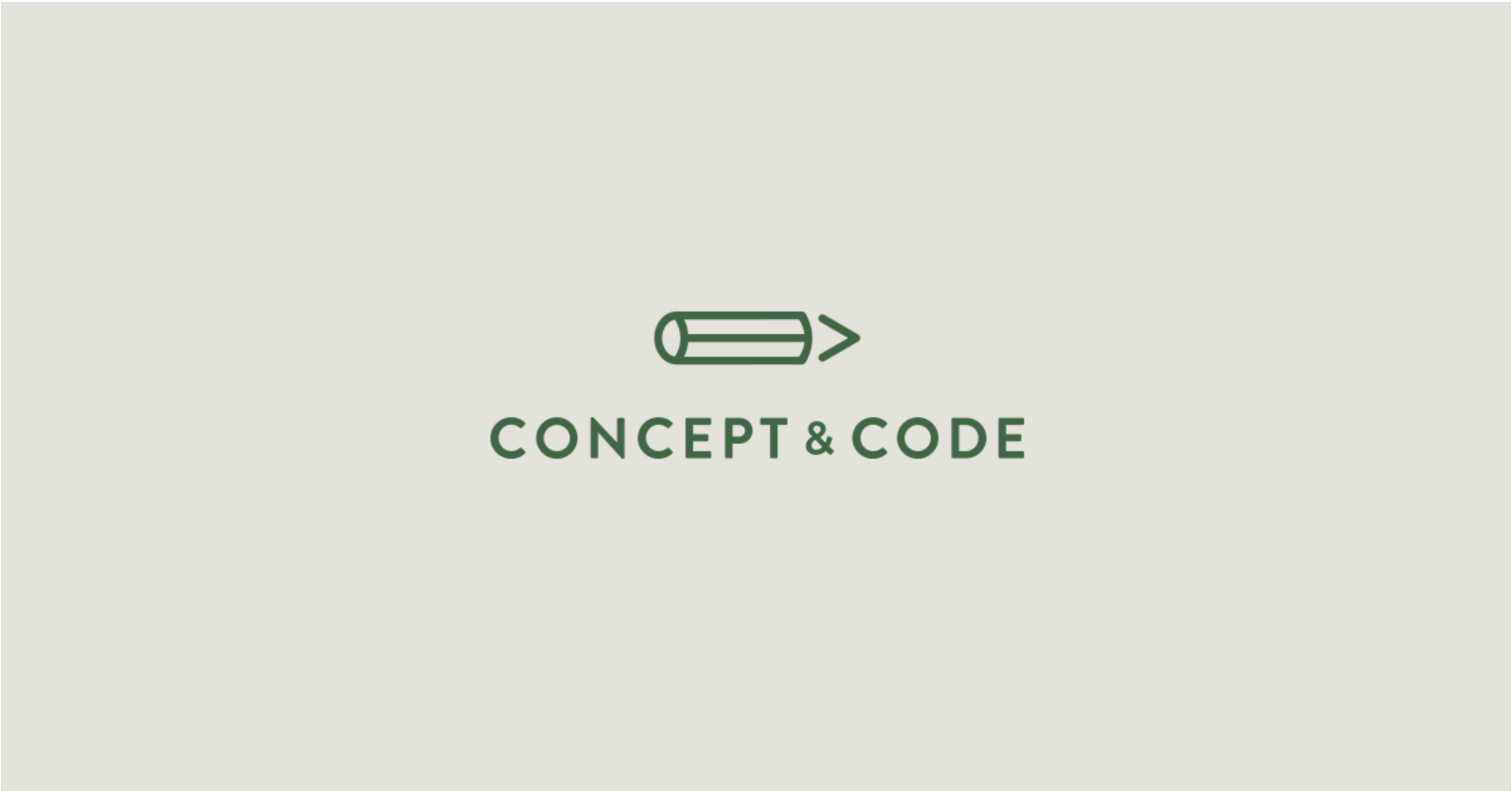
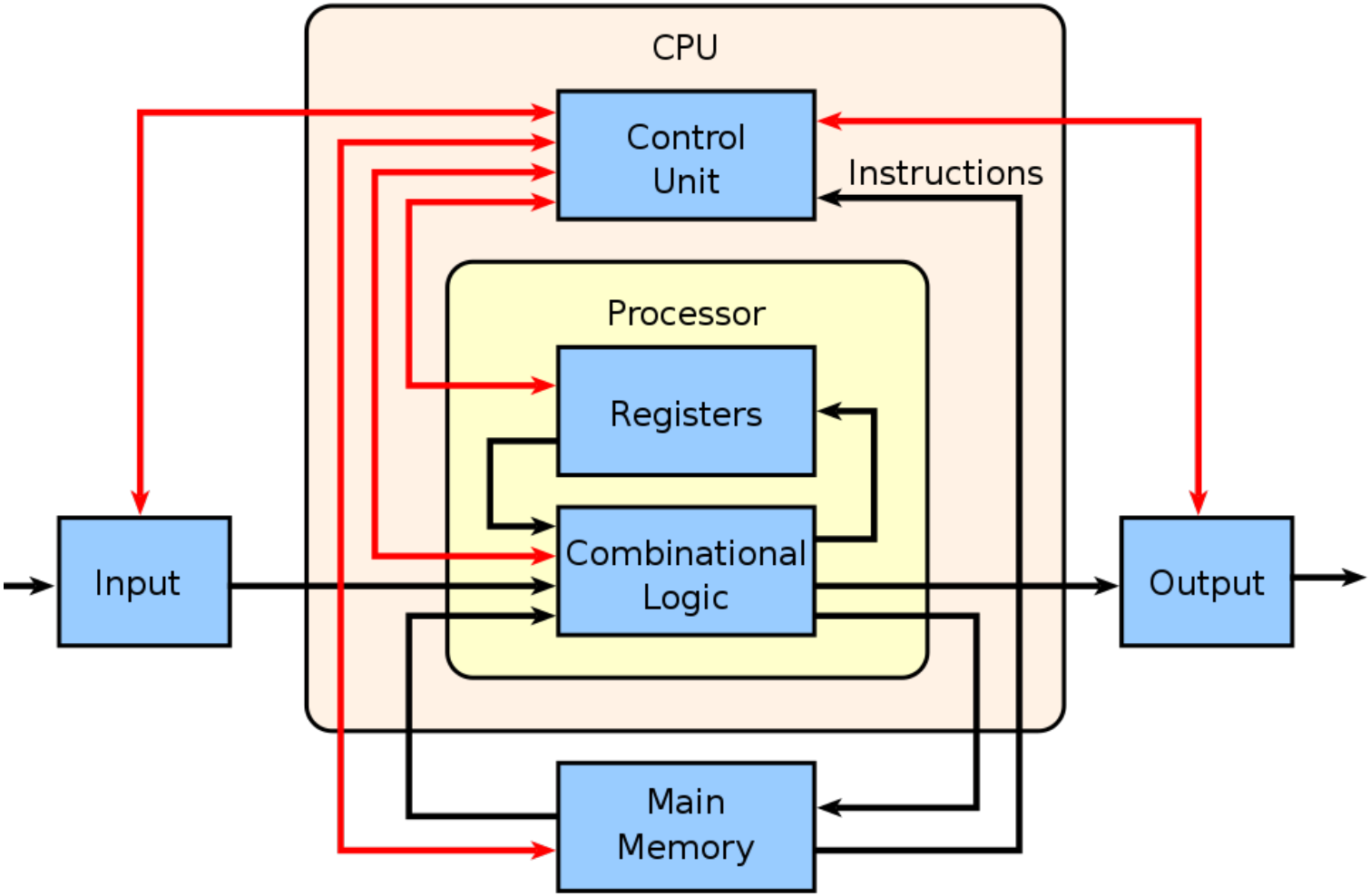
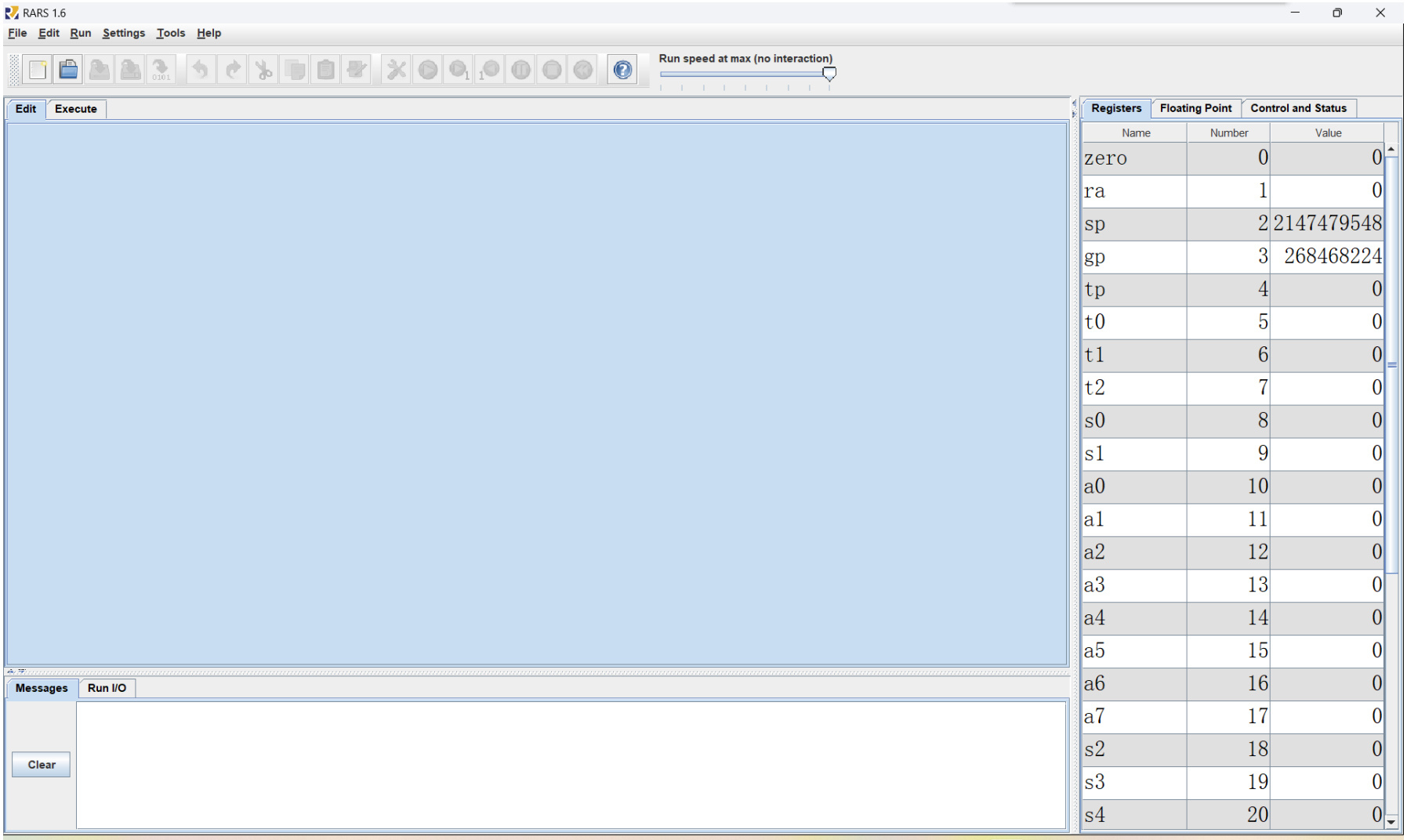

CONCEPT & CODE



Registers (zero, pc)　Memory (Data, Instructions)　I/O

RARS: RISC-V Assembler and Runtime Simulator



https://github.com/TheThirdOne/rars

add.asm

add.asm

addi.asm

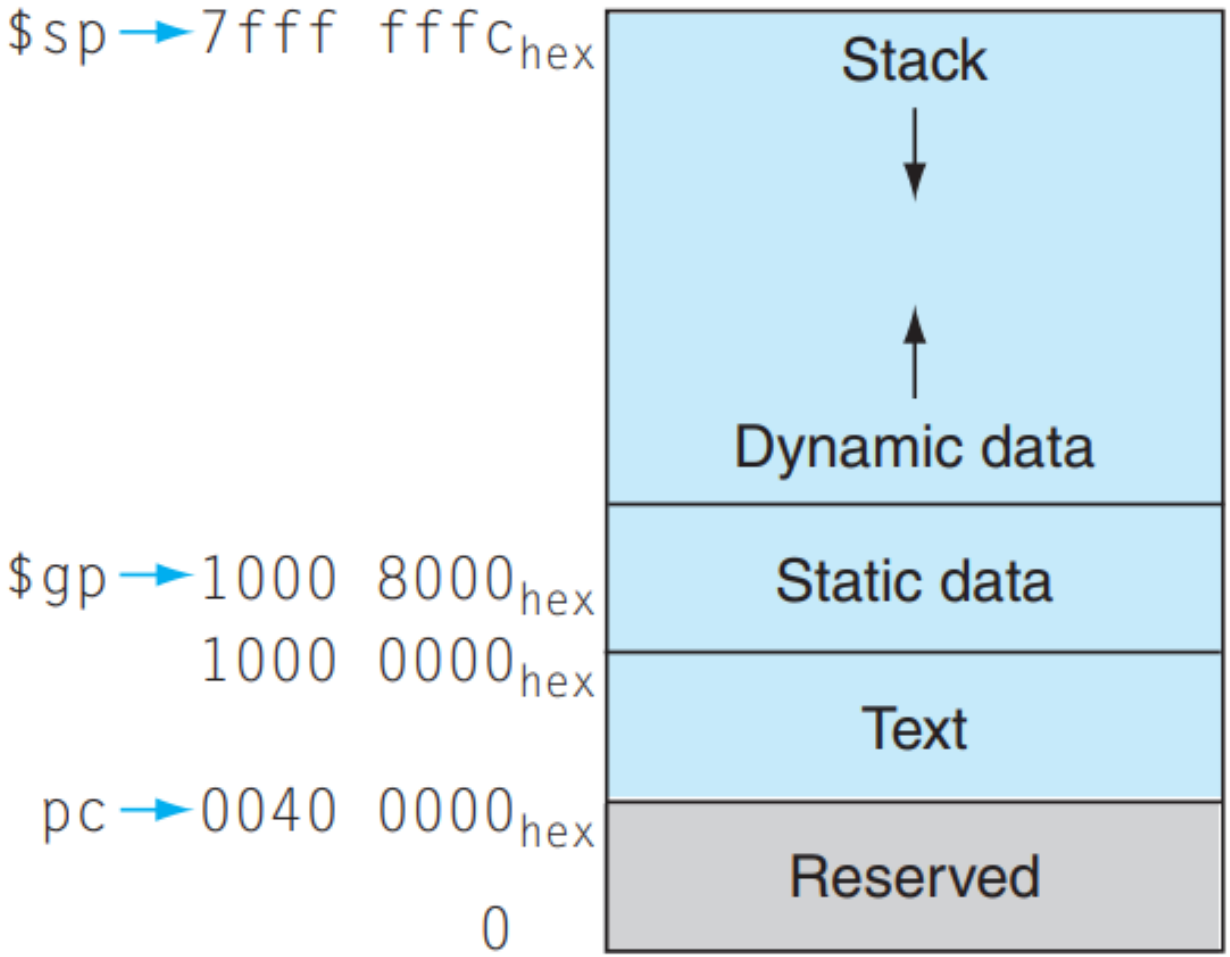
add.asm

addi.asm

add-sub.asm

ecall.asm

data.asm


$sp → 7fff fffc hex
Stack
Dynamic data
$gp → 1000 8000 hex
Static data
1000 0000 hex
Text
pc → 0040 0000 hex
Reserved
0

array.asm

branch-max.asm

proc-max.asm

proc-max.asm

控制流 (control-flow) + 数据流 (data-flow)

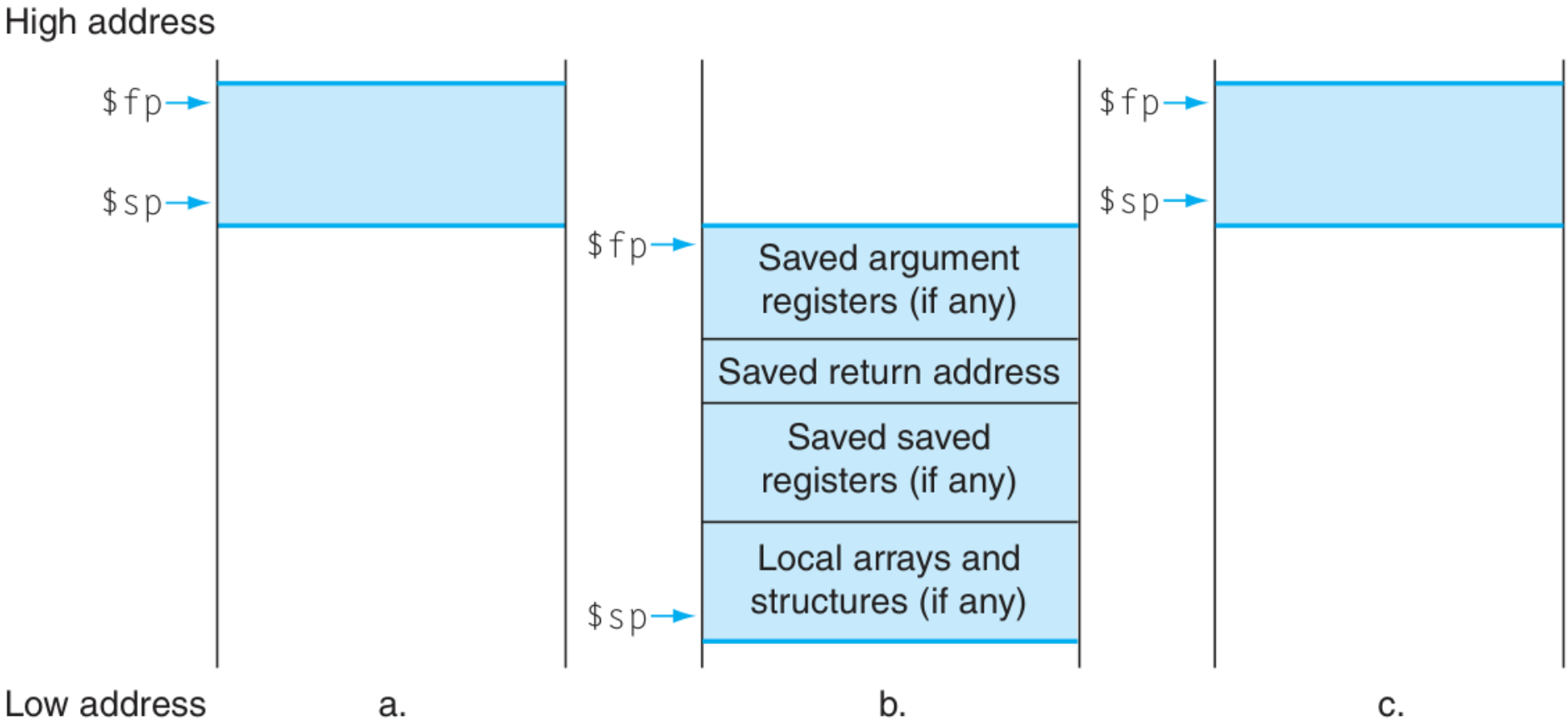
proc-max.asm

proc-fact.asm

proc-fact.asm

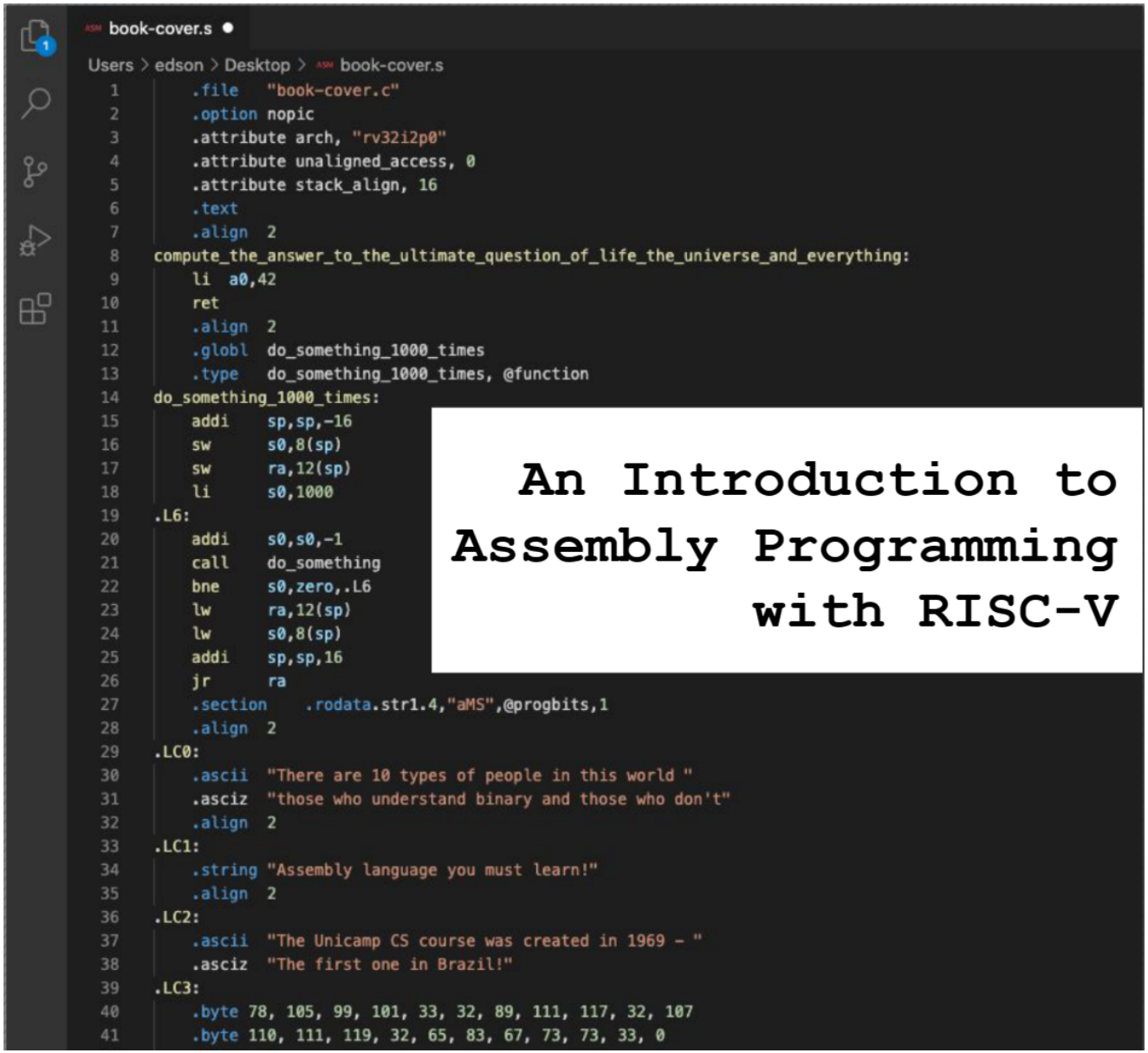
RISC-V 调用约定 (Calling Convention)

Registers	Symbolic names	Description	Saver
x0	zero	Hardwired zero	—
x1	ra	Return address	Caller
x2	sp	Stack pointer	Callee
x3	gp	Global pointer	—
x4	tp	Thread pointer	—
x5-x7	t0-t2	Temporary registers	Caller
x8-x9	s0-s1	Saved registers	Callee
x10-x11	a0-a1	Function arguments and return values	Caller
x12-x17	a2-a7	Function arguments	Caller
x18-x27	s2-s11	Saved registers	Callee
x28-x31	t3-t6	Temporary registers	Caller

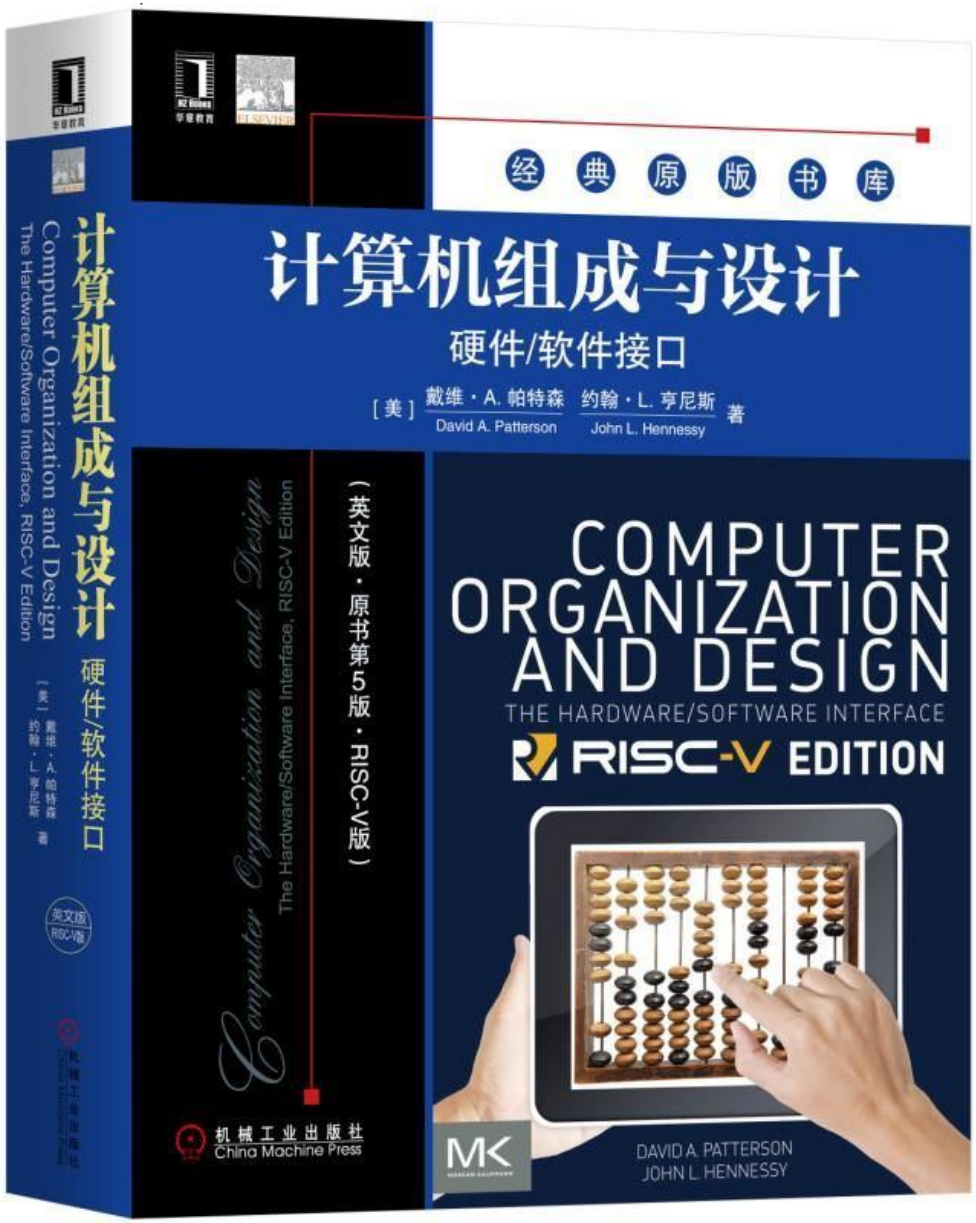

High address
$fp
$sp
$fp
Saved argument registers (if any)
Saved return address
Saved saved registers (if any)
Local arrays and structures (if any)
$sp
$fp
$sp
Low address
a.
b.
c.

bubblesort.asm

bubblesort @ CompilerExplorer



An Introduction to Assembly Programming with RISC-V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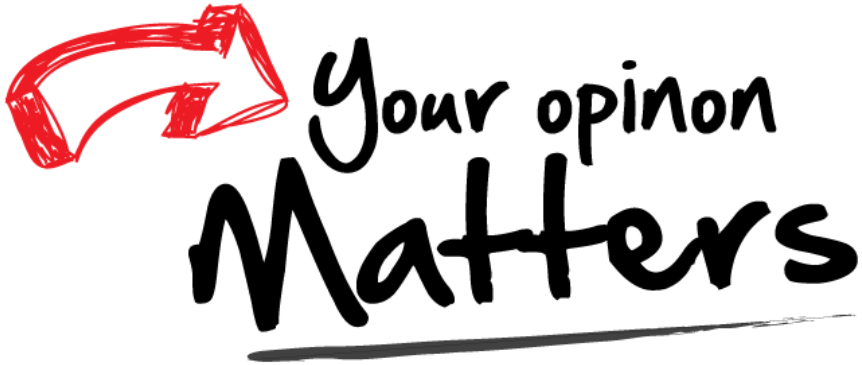
Thank
You!



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