五、目标代码生成
(16. 指令选择)

魏恒峰

hfwei@nju.edu.cn

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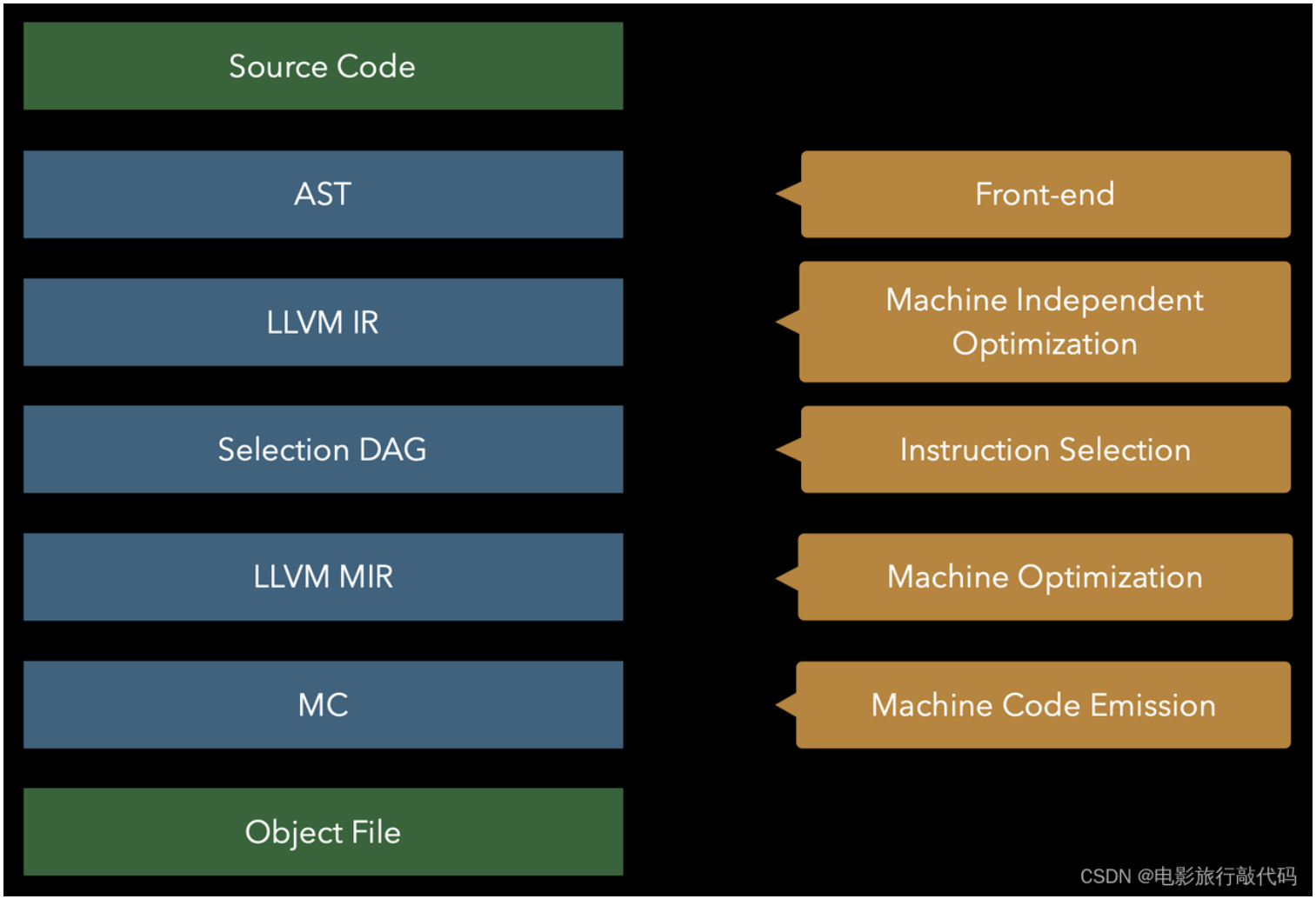
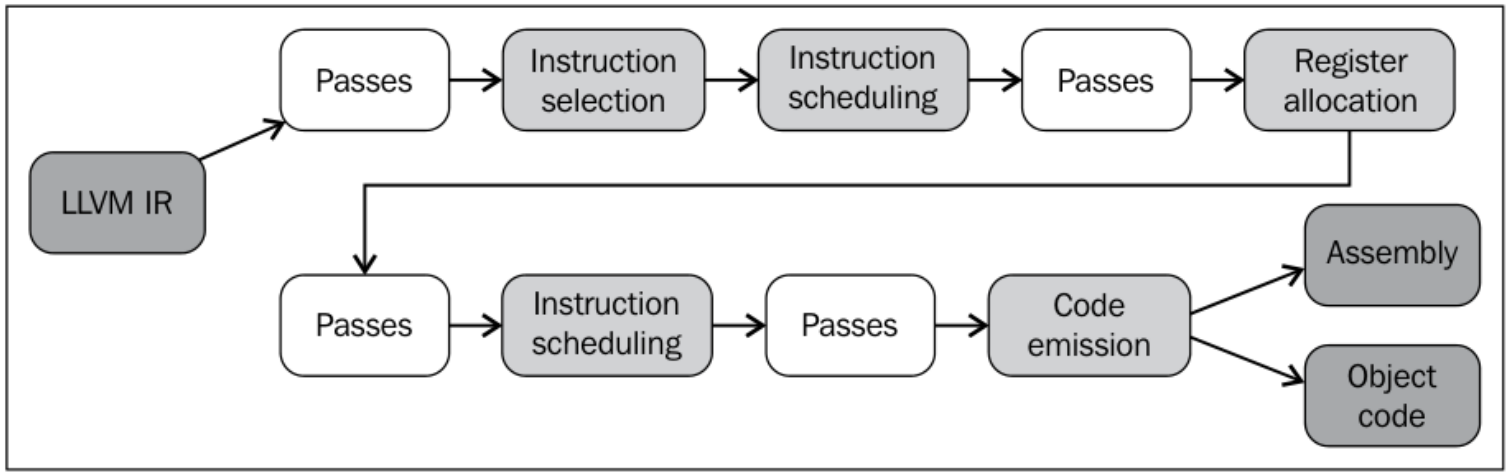
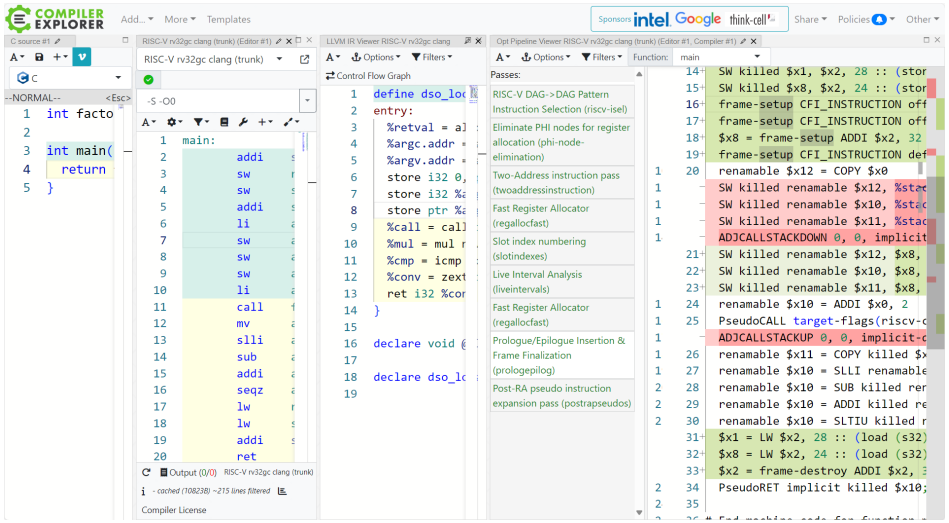

Source Code
AST
LLVM IR
Selection DAG
LLVM MIR
MC
Object File
Front-end
Machine Independent Optimization
Instruction Selection
Machine Optimization
Machine Code Emission
CSDN @电影旅行敲代码

in-memory LLVM IR SelectionDAG MachineInstr MCInst

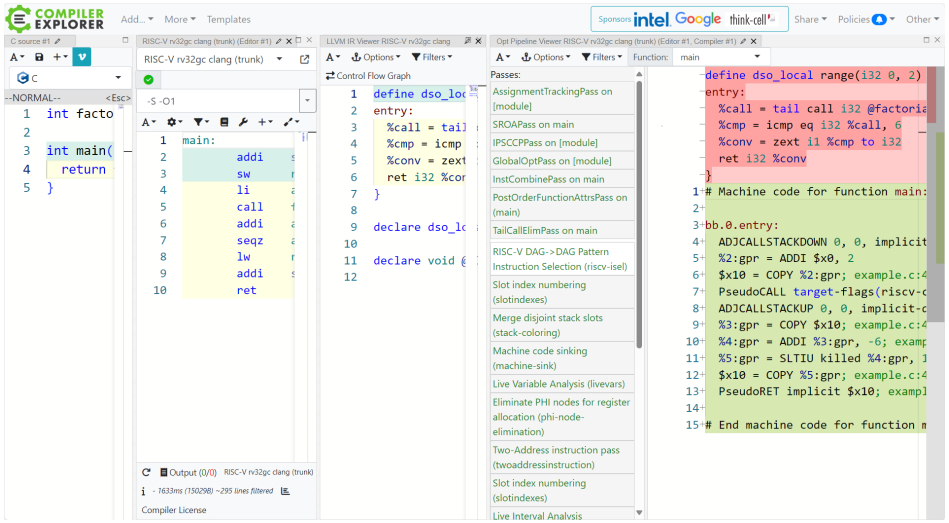


Where is “Prologue/Epilogue Insertion”?

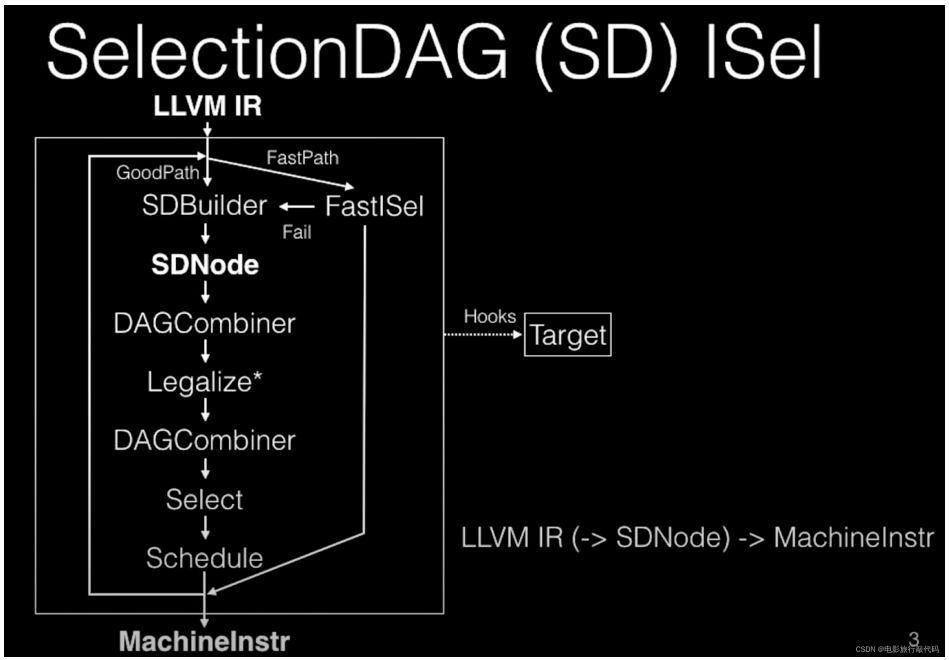
f0-O0 @ Compiler Explorer



f0-O1 @ Compiler Explorer



SDISel　FastISel (per basic block)　GlobalISel (per function)



Instruction Selection (ISel)

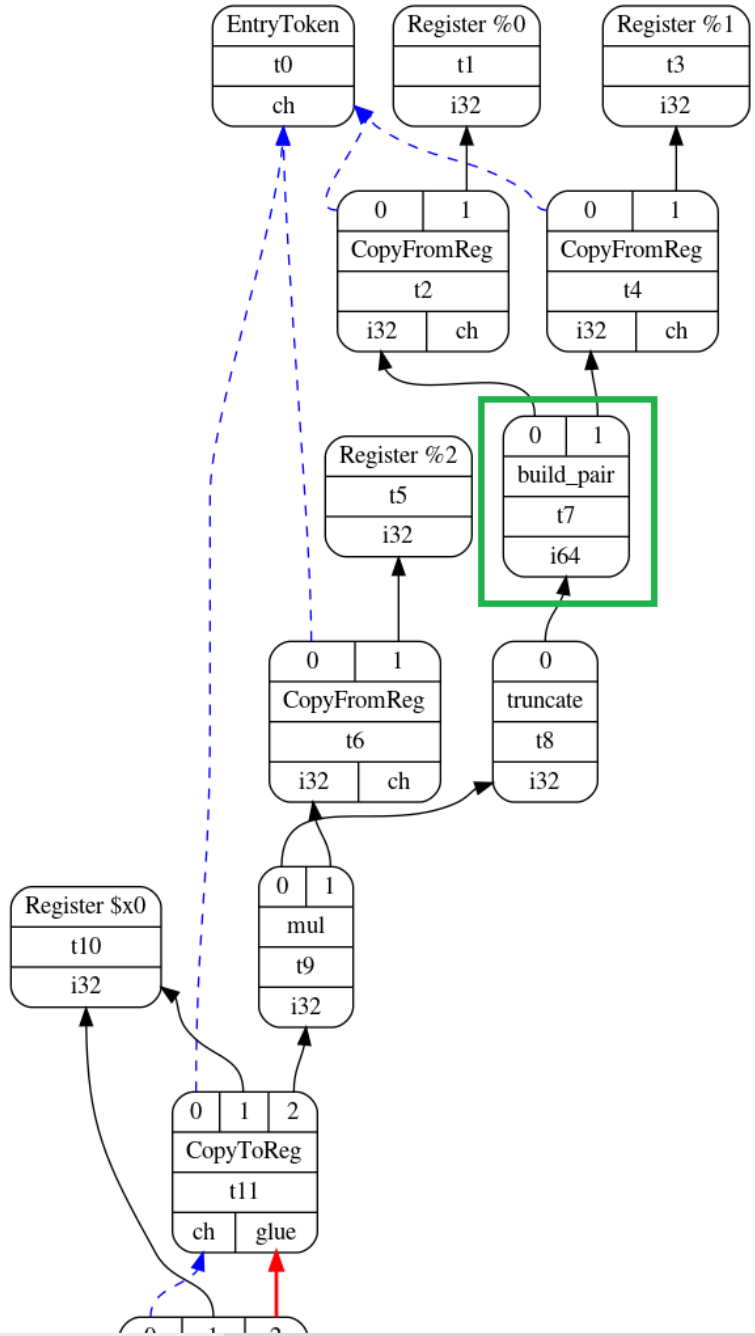
SelectionDAG Select Phase

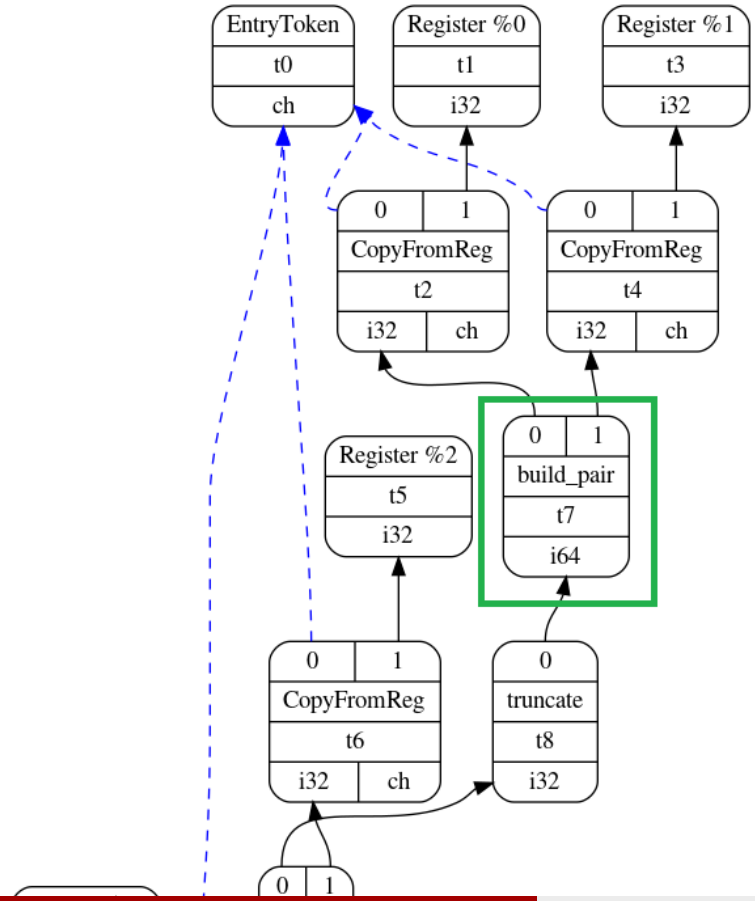
The Select phase is the bulk of the target-specific code for instruction selection. This phase takes a legal SelectionDAG as input, pattern matches the instructions supported by the target to this DAG, and produces a new DAG of target code. For example, consider the following LLVM fragment:

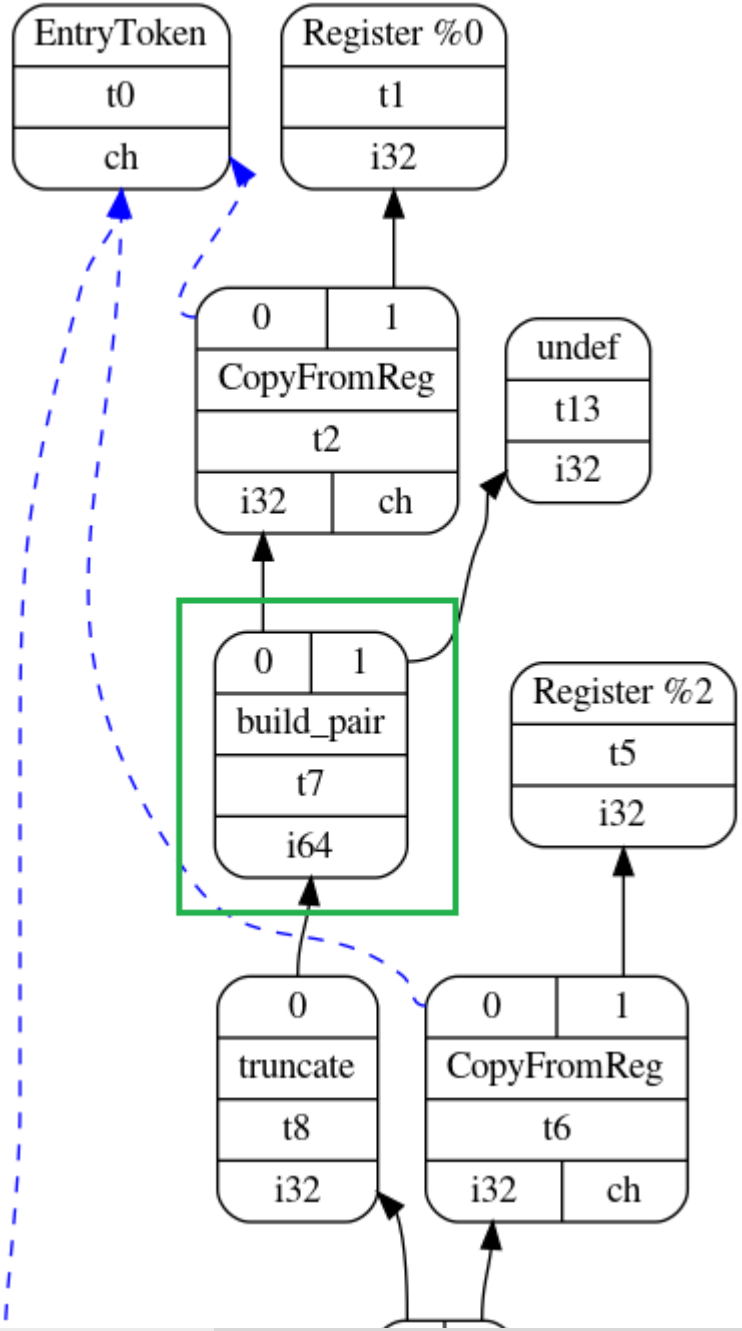
```c
unsigned int MUL(unsigned long long int x, unsigned int y)
{
    return x * y;
}
```

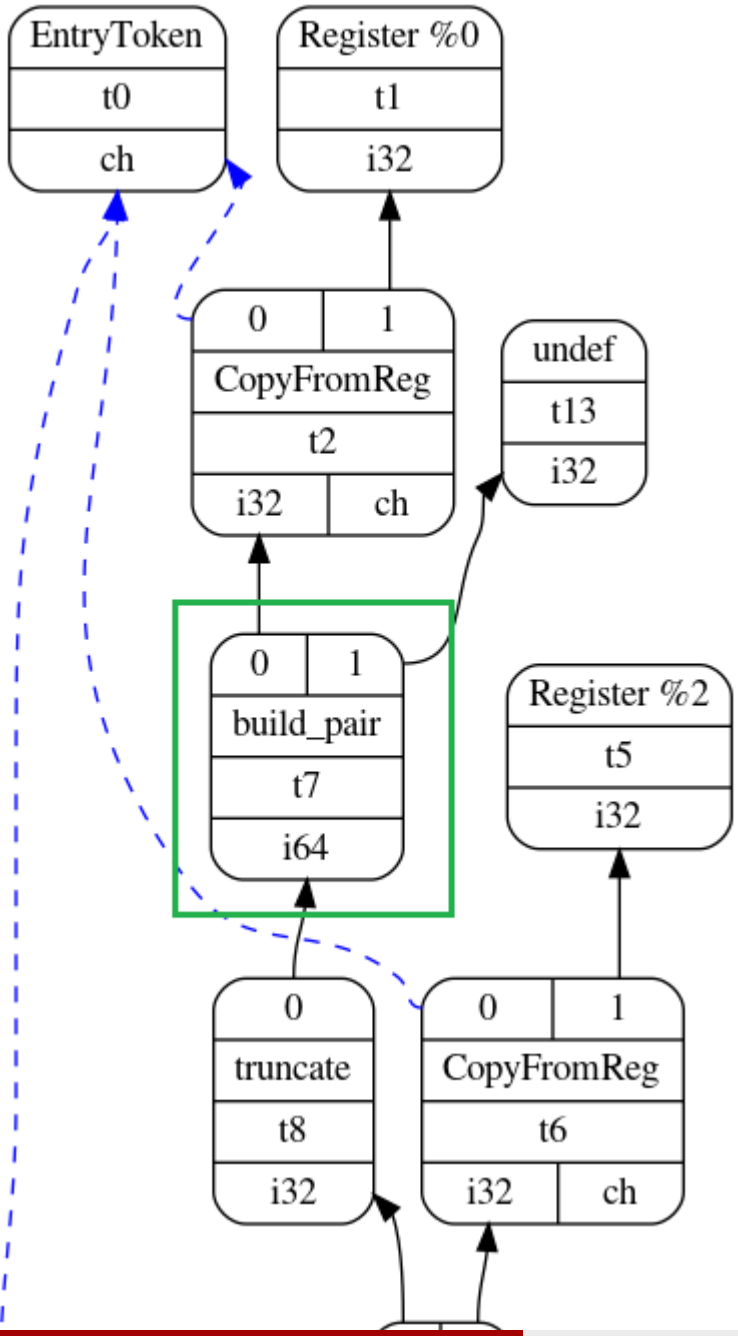
```llvm
define dso_local i32 @MUL(i64 %x, i32 %y) local_unnamed_addr #0 {
entry:
  %0 = trunc i64 %x to i32
  %conv1 = mul i32 %0, %y
  ret i32 %conv1
}
```

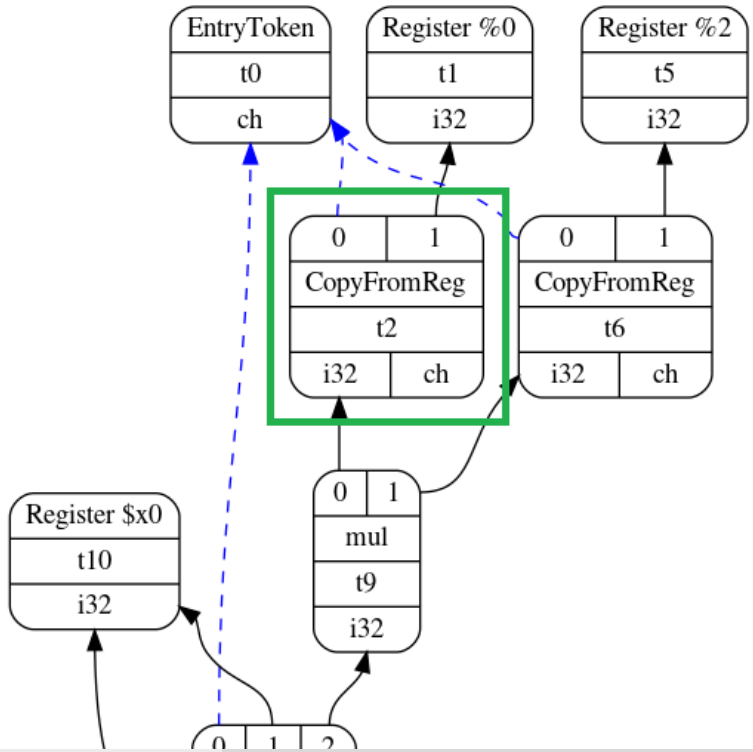
```
define dso_local i32 @MUL(i64 %x, i32 %y) local_unnamed_addr #0 {
entry:
  %0 = trunc i64 %x to i32
  %conv1 = mul i32 %0, %y
  ret i32 %conv1
}
```

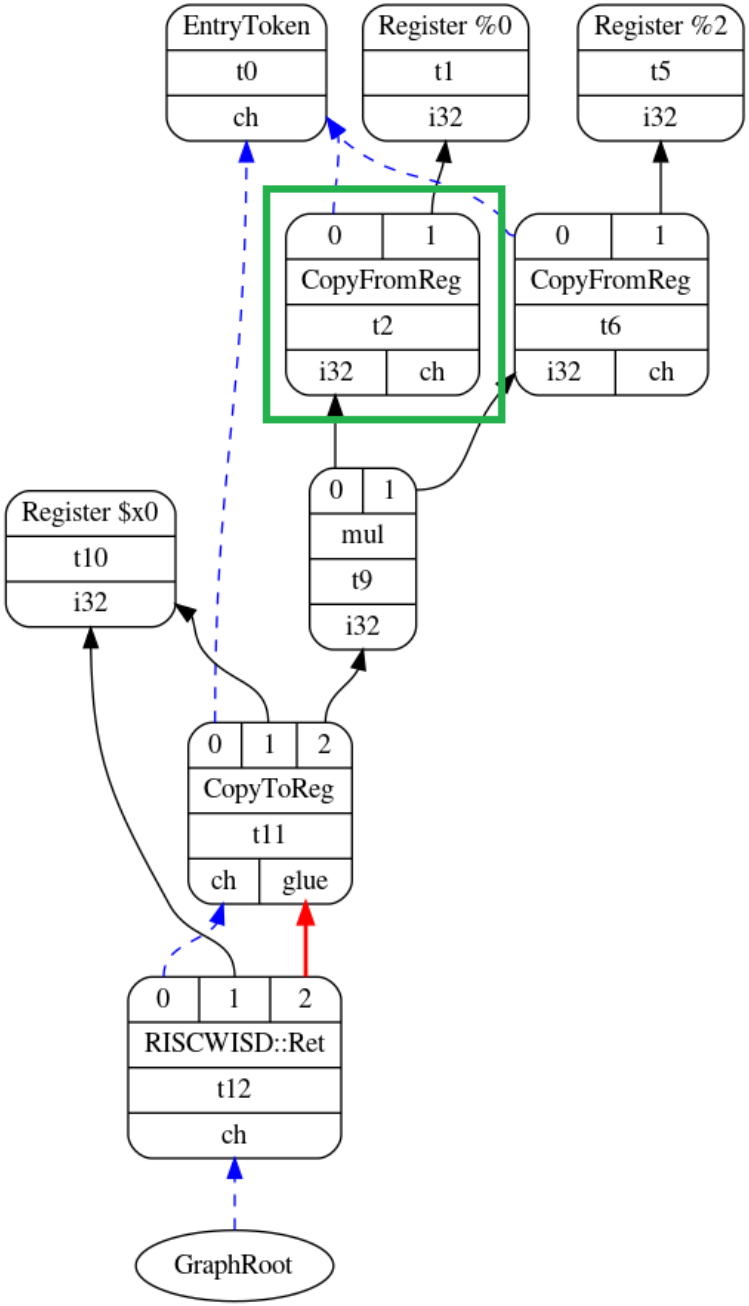



EntryToken
t0
ch
Register %0
t1
i32
Register %1
t3
i32
0
1
CopyFromReg
t2
i32
ch
0
1
CopyFromReg
t4
i32
ch
Register %2
t5
i32
0
1
build_pair
t7
i64
0
truncate
t8
i32
0
1
CopyFromReg
t6
i32
ch
0
1

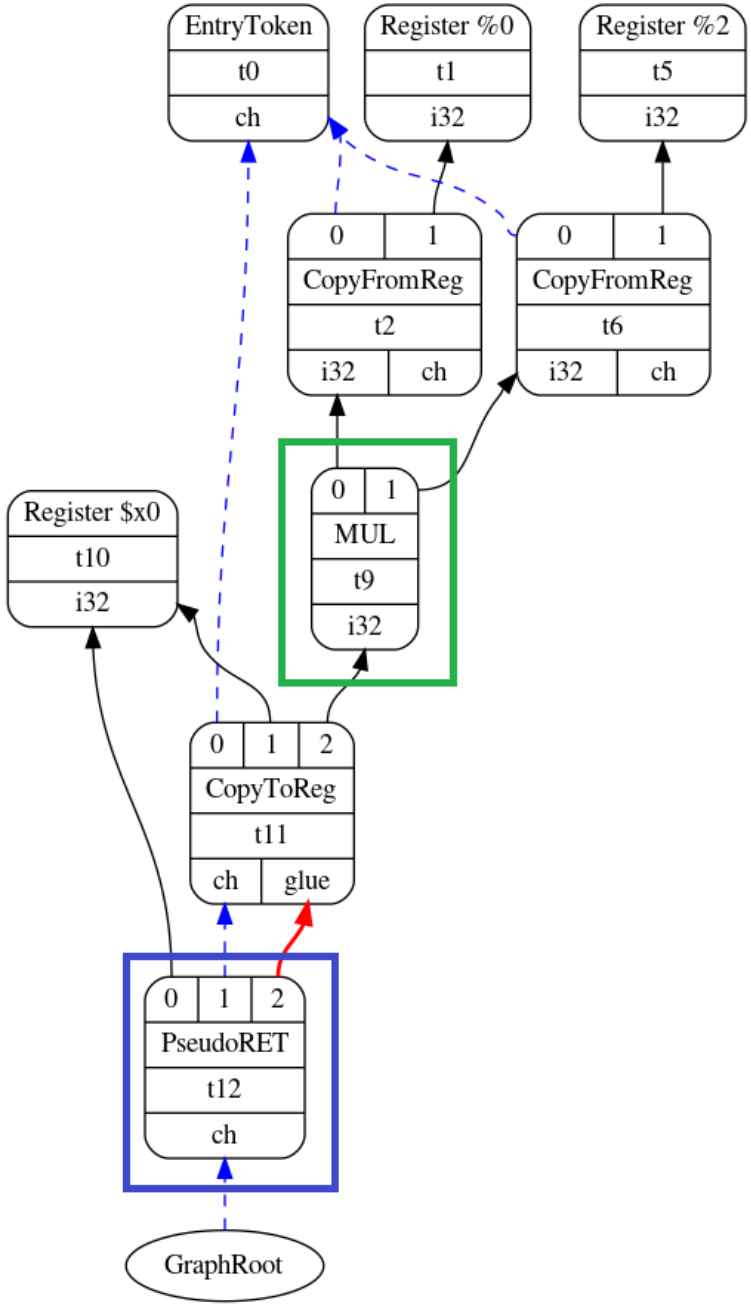

EntryToken
t0
ch
Register %0
t1
i32
0
1
CopyFromReg
t2
i32
ch
undef
t13
i32
0
1
build_pair
t7
i64
Register %2
t5
i32
0
truncate
t8
i32
0
1
CopyFromReg
t6
i32
ch


EntryToken
t0
ch
Register %0
t1
i32
0
1
CopyFromReg
t2
i32
ch
undef
t13
i32
0
1
build_pair
t7
i64
Register %2
t5
i32
0
truncate
t8
i32
0
1
CopyFromReg
t6
i32
ch

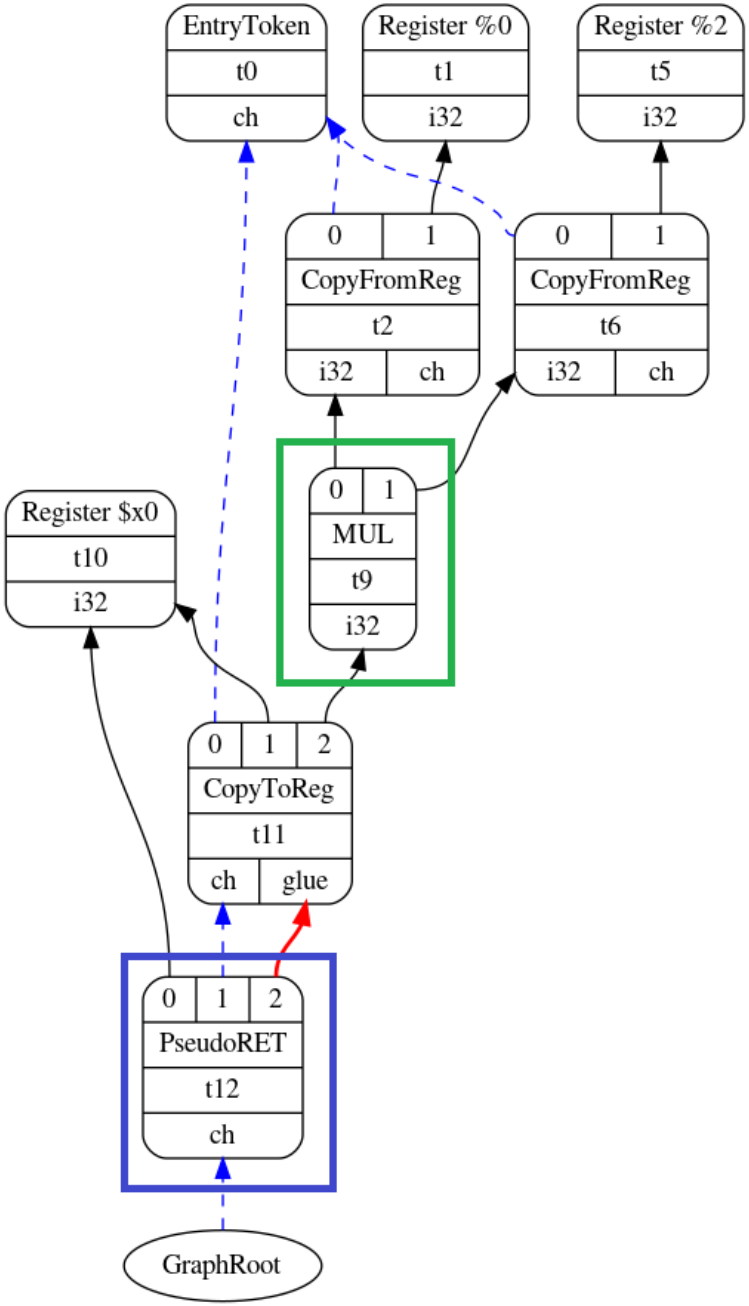

EntryToken
t0
ch
Register %0
t1
i32
Register %2
t5
i32
0
1
CopyFromReg
t2
i32
ch
0
1
CopyFromReg
t6
i32
ch
Register $x0
t10
i32
0
1
mul
t9
i32



dag-combine2 input for MUL:entry



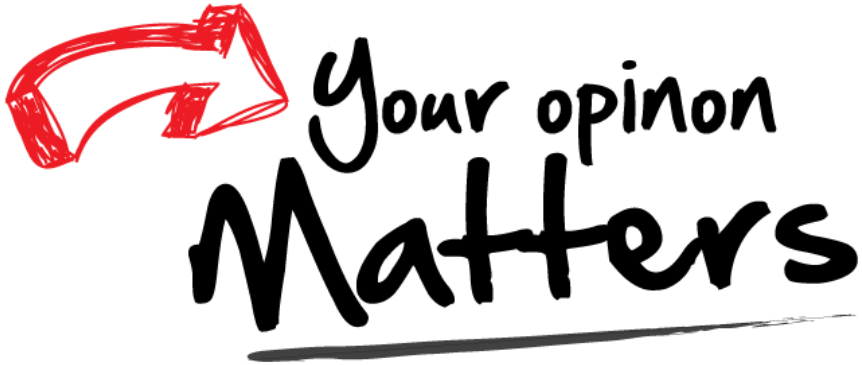
scheduler input for MUL:entry



scheduler input for MUL:entry

```
bb.0.entry:
  liveins: $x0, $x2
  %2:gpr = COPY $x2
  %0:gpr = COPY $x0
  %3:gpr = MUL %0:gpr, %2:gpr
  $x0 = COPY %3:gpr
  PseudoRET implicit $x0
```


Thank
You!



Office 926

hfwei@nju.edu.cn