

五、目标代码生成

(1. RISC-V 概述)

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2023 年 06 月 02 日



WELCOME!

A decorative banner at the bottom of the slide featuring the word "WELCOME!" in large, bold, white letters. The letters are partially obscured by a burst of colorful confetti in shades of blue, yellow, red, and green.



RISC: Reduced Instruction Set Computer (精简指令集计算机)



V: Five

CISC: Complex Instruction Set Computer (复杂指令集计算机)



RISC: Each instruction performs only one function.

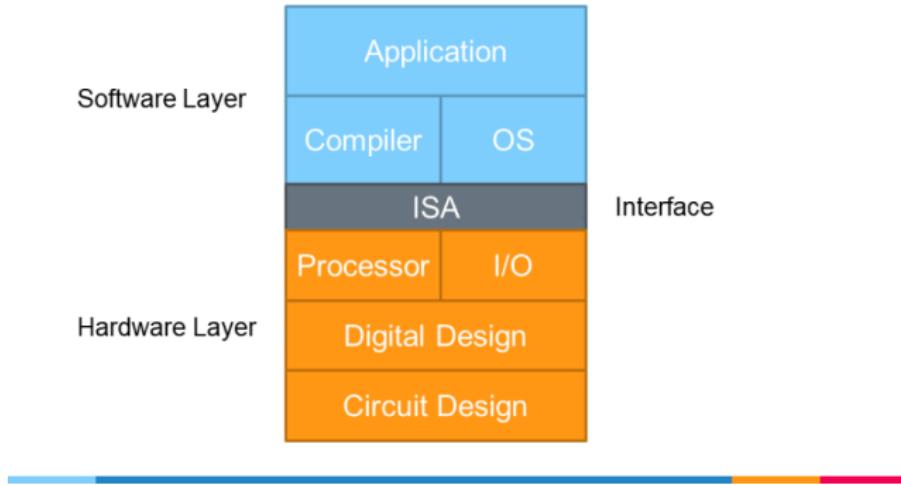
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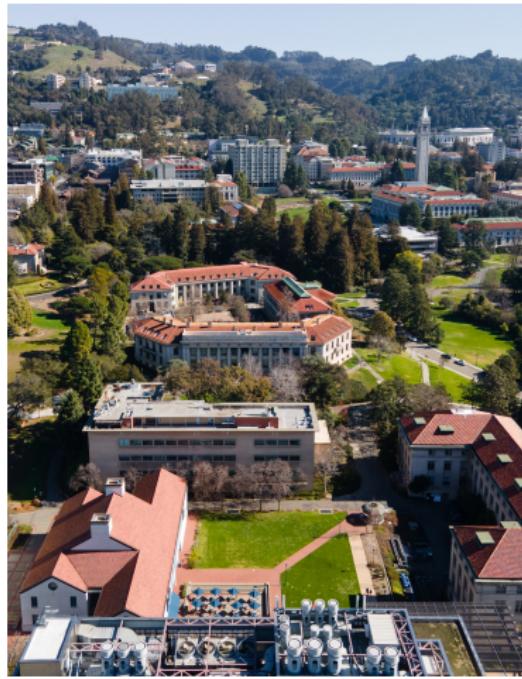
CISC:



RISC:

ISA as the Software/Hardware Interface



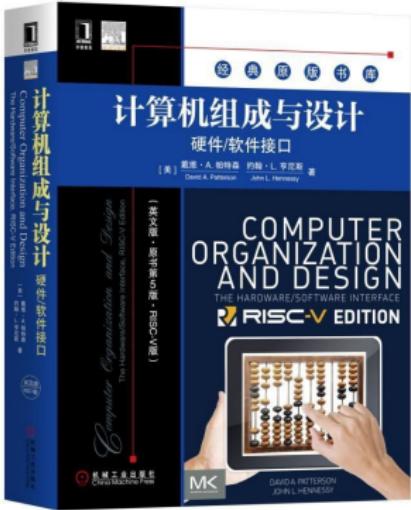


David Andrew Patterson (1947 ~)

2017 ACM Turing Award



“Hennessy and Patterson created a systematic and quantitative approach to designing faster, lower power, and **reduced instruction set computer (RISC)** microprocessors.”



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Announcements

First-ever RISC-V Summit Europe Will Demonstrate Technical and Commercial Momentum Across Industries

The Barcelona RISC-V Summit from June 5-9 will focus on industries such as Automotive, High-Performance Compute/Data Center, and Security; Call for Submissions and Sponsorships are now open.

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Join RISC-V International



RISC-V International comprises a large member organization building the first open, collaborative community of software and hardware innovators powering innovation at the edge forward. Through various events and workshops, RISC-V International is changing the way the industry works together and collaborates – creating a new kind of open hardware and software ecosystem. Become a member today and help pioneer the industry's future!

Premier Members



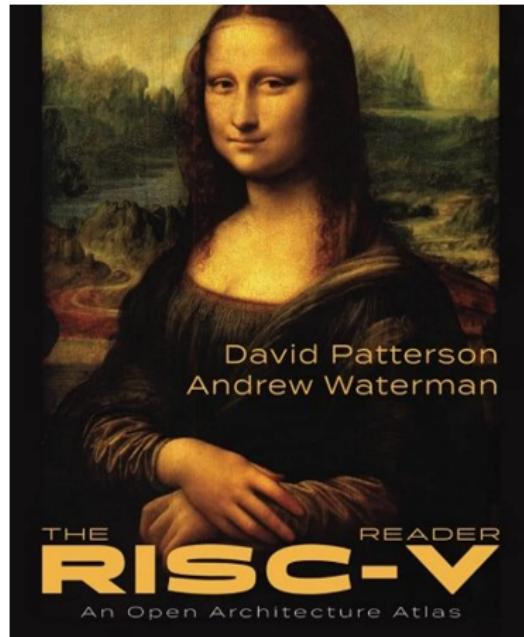
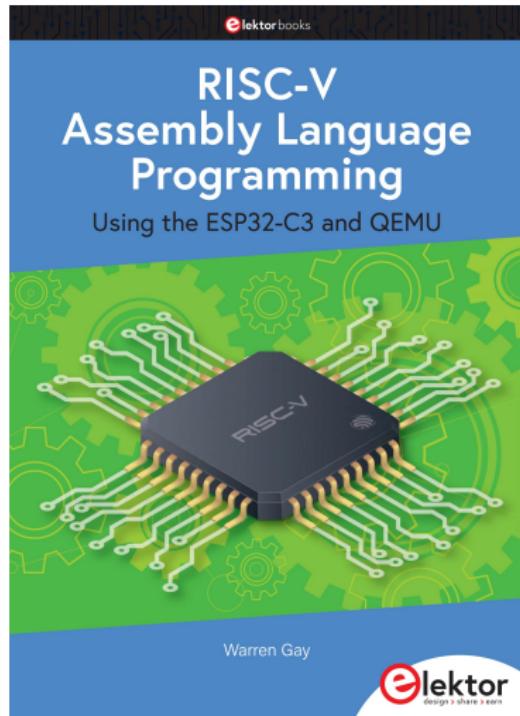
成为资本 CHENGING CAPITAL



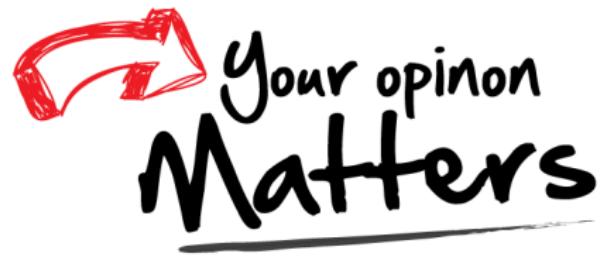
2019 年国际芯片大会



“RISC-V 很可能发展成为世界主流 CPU 之一，在 CPU 领域形成 Intel、ARM、RISC-V 三分天下的格局。” — 中国工程院院士 倪光南



Thank You!



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