

五、目标代码生成

(1. RISC-V 概述)

魏恒峰

hfwei@nju.edu.cn

2023 年 06 月 02 日

WELCOME!

RISC: Reduced Instruction Set Computer (精简指令集计算机)



V: Five

CISC: Complex Instruction Set Computer (复杂指令集计算机)

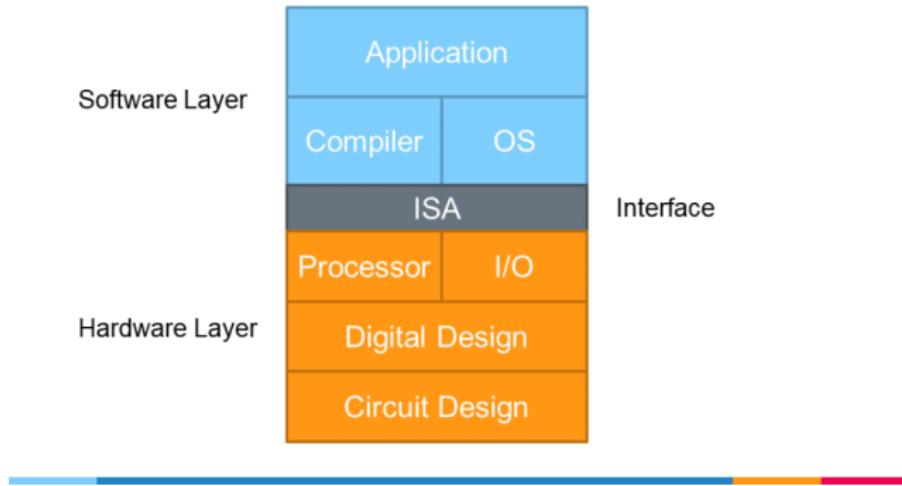


RISC: Each instruction performs only one function.

CISC: SUBL val, %eax ; %eax <- %eax - val)



ISA (Instruction Set Architecture) as the Software/Hardware Interface



2017 ACM Turing Award



“Hennessy and Patterson created a systematic and quantitative approach to designing faster, lower power, and **reduced instruction set computer (RISC)** microprocessors.”



[About RISC-V](#)[Membership](#)[RISC-V Exchange](#)[Technical](#)[News & Events](#)[Community](#)

Announcements

First-ever RISC-V Summit Europe Will Demonstrate Technical and Commercial Momentum Across Industries

The Barcelona RISC-V Summit from June 5-9 will focus on industries such as Automotive, High-Performance Compute/Data Center, and Security; Call for Submissions and Sponsorships are now open.

[READ MORE](#)

Join RISC-V International



RISC-V International comprises a large member organization building the first open, collaborative community of software and hardware innovators powering innovation at the edge forward. Through various events and workshops, RISC-V International is changing the way the industry works together and collaborates – creating a new kind of open hardware and software ecosystem. Become a member today and help pioneer the industry's future!

Premier Members



成为资本 CHENGJIU CAPITAL



2019 年国际芯片大会



“RISC-V 很可能发展成为世界主流 CPU 之一，在 CPU 领域形成 Intel、ARM、RISC-V 三分天下的格局。” — 中国工程院院士 倪光南



新长征路上的摇滚

“万里长征第一步 ...”

RISC-V Assembly Language Programming

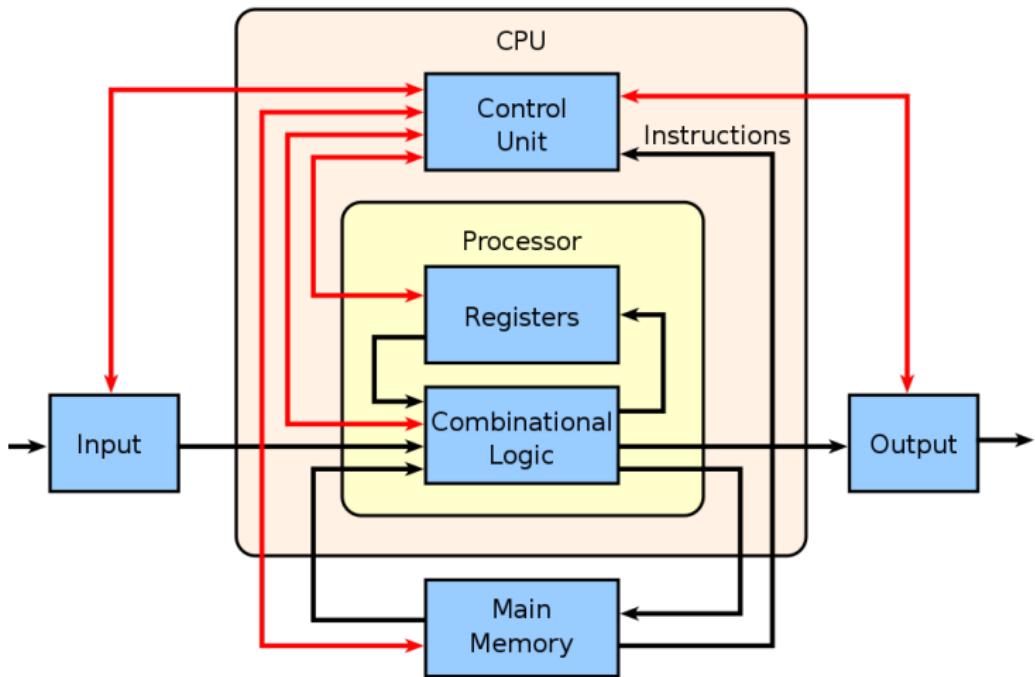
Using the ESP32-C3 and QEMU



Warren Gay



CONCEPT & CODE



Registers (zero, pc)

Memory (Data, Instructions)

I/O

add.asm

addi.asm

add-sub.asm

ecall.asm

data.asm

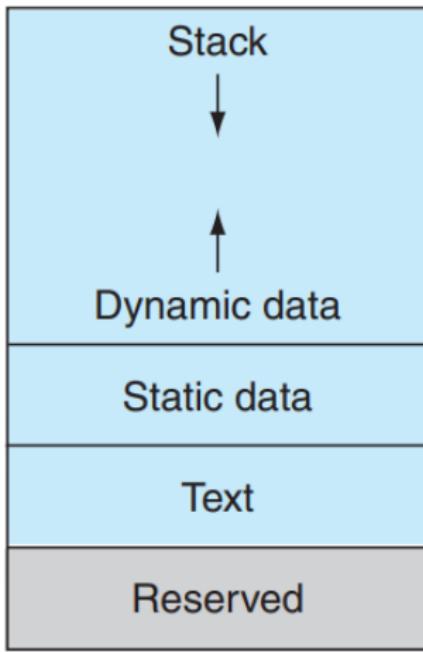
\$sp → 7fff fffc_{hex}

\$gp → 1000 8000_{hex}

1000 0000_{hex}

pc → 0040 0000_{hex}

0



array.asm

array-index-bit.asm

branch-max.asm

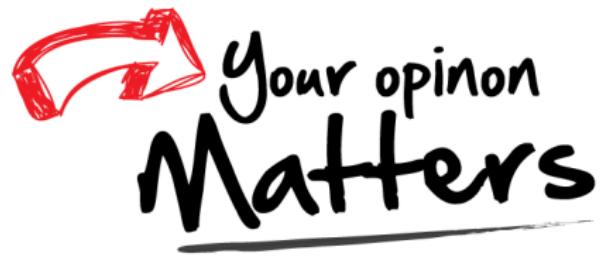
proc-max.asm

Registers	Symbolic names	Description
x0	zero	Hardwired zero
x1	ra	Return address
x2	sp	Stack pointer
x3	gp	Global pointer
x4	tp	Thread pointer
x5-x7	t0-t2	Temporary registers
x8-x9	s0-s1	Saved registers
x10-x11	a0-a1	Function arguments and return values
x12-x17	a2-a7	Function arguments
x18-x27	s2-s11	Saved registers
x28-x31	t3-t6	Temporary registers

proc-fact.asm

bubblesort.asm

Thank You!



Office 926

hfwei@nju.edu.cn