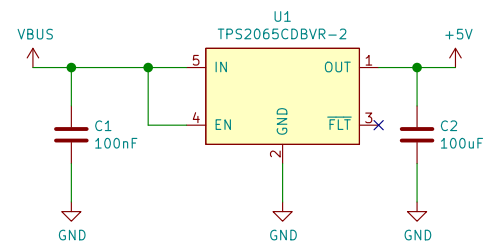
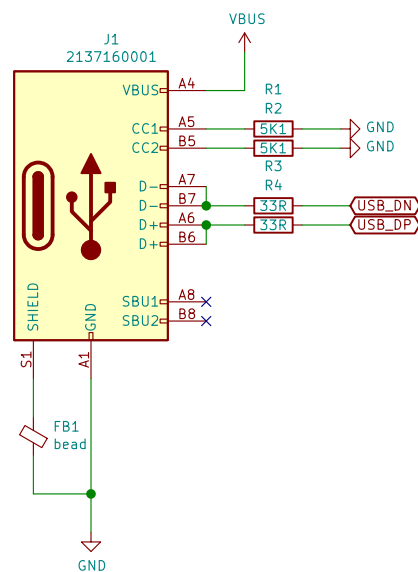


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B	<div>Sheet: Power</div> <div>File: Power/file606F3C8C.sch</div>		<div>Sheet: Pin_header</div> <div>File: Header/file608CB110.sch</div>			
C	<div>Sheet: MCU</div> <div>File: M480/file606F3CD8.sch</div>		<div>H1</div> <div>MountingHole</div>	<div>H3</div> <div>MountingHole</div>		
D			<div>H2</div> <div>MountingHole</div>	<div>H4</div> <div>MountingHole</div>	<div>danchouzhou@gmail.com</div> <div>Copyright © Danny Chou, all rights reserved.</div> <div>DANCHOUZHOU</div> <div>Sheet: /</div> <div>File: NuDAC.sch</div> <div>Title: NuDAC</div> <div>Size: A4</div> <div>Date: 2021-06-02</div> <div>KiCad E.D.A. kicad (5.1.9)-1</div> <div>Rev: 1.0.0</div> <div>Id: 1/6</div>	
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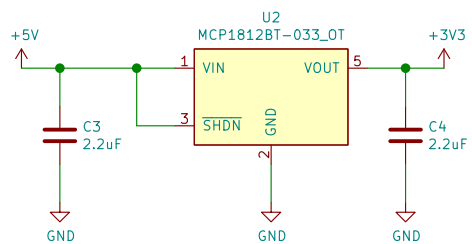
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Size: A4 Date: 2021-06-02

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Sheet: /Power/  
File: file606F3C8C.sch

**Title: NuDAC**

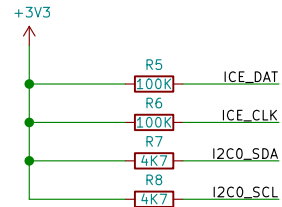
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KiCad E.D.A. kicad (5.1.9)-1

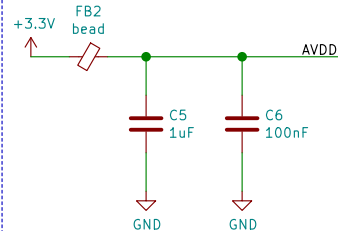
**Rev: 1.0.0**

Id: 3/6

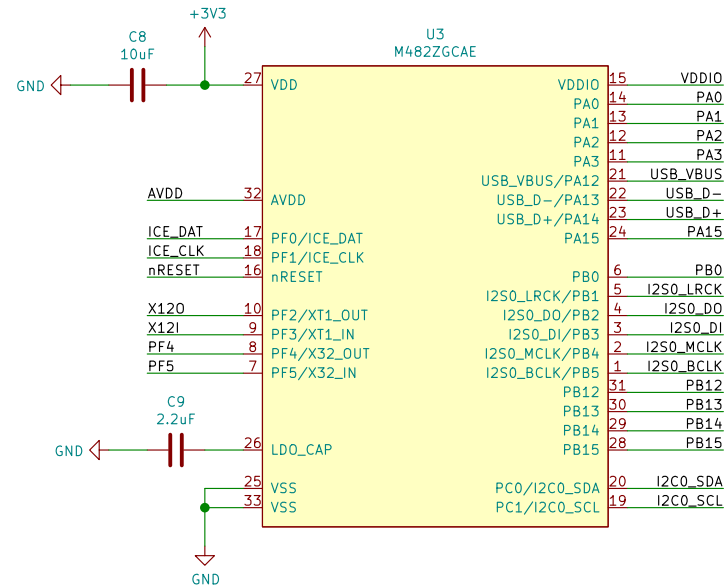
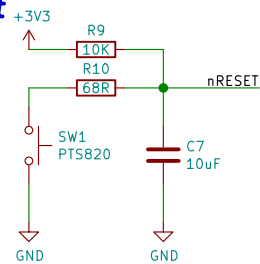
## Pull-up resistor



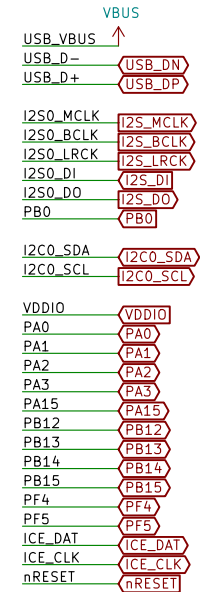
## AVDD



## Reset



## Off page connection



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Sheet: /MCU/  
File: file606F3CD8.sch

**Title: NuDAC**

Size: A4 Date: 2021-06-02

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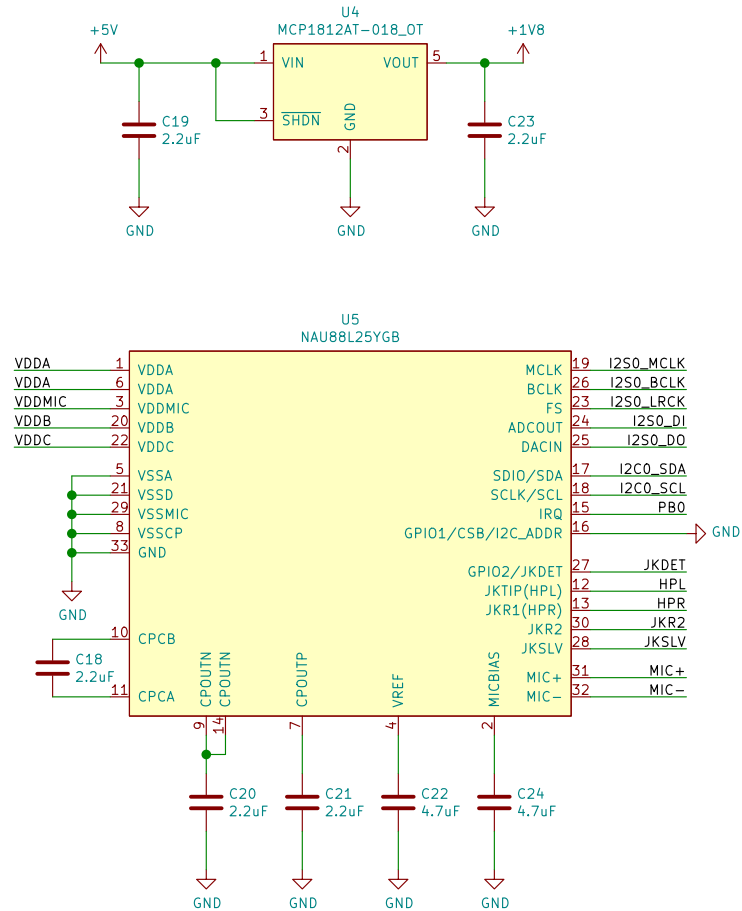
**Rev: 1.0.0**

Id: 4/6

## Bulk and filter

The diagrams illustrate the bulk and filter capacitor placement for various power rails:

- VDDA:** +1V8 source, FB3 bead, bulk capacitor C10 (4.7uF) to GND, filter capacitor C14 (100nF) to GND.
- VDDC:** +1V8 source, FB4 bead, bulk capacitor C11 (4.7uF) to GND, filter capacitor C15 (100nF) to GND.
- VDDMIC:** +3V3 source, FB5 bead, bulk capacitor C12 (4.7uF) to GND, filter capacitor C16 (100nF) to GND.
- VDDDB:** +3V3 source, FB6 bead, bulk capacitor C13 (4.7uF) to GND, filter capacitor C17 (100nF) to GND.



## Off page connection

The diagram illustrates off-page connections for various signals. On the left, the signals are listed: I2S0\_MCLK, I2S0\_BCLK, I2S0\_LRCK, I2S0\_DI, I2S0\_DO, PB0, I2C0\_SDA, and I2C0\_SCL. On the right, there are two red rectangular boxes. The top box contains the labels I2S\_MCLK, I2S\_BCLK, and I2S\_LRCK. The bottom box contains the labels I2S\_DI, I2S\_DO, and PB0. Green lines connect the signals on the left to their corresponding labels in the boxes on the right. Specifically, I2S0\_MCLK connects to I2S\_MCLK, I2S0\_BCLK to I2S\_BCLK, I2S0\_LRCK to I2S\_LRCK, I2S0\_DI to I2S\_DI, I2S0\_DO to I2S\_DO, and PB0 to PB0. The I2C0\_SDA and I2C0\_SCL signals on the left do not have corresponding connections shown on the right.

I2S0_MCLK	I2S_MCLK
I2S0_BCLK	I2S_BCLK
I2S0_LRCK	I2S_LRCK
I2S0_DI	I2S_DI
I2S0_DO	I2S_DO
PB0	PB0
I2C0_SDA	I2C0_SDA
I2C0_SCL	I2C0_SCL

# Phone jack

Thanks for Singatron Co. provide the sample.

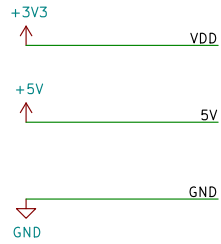
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Title: NuDAC

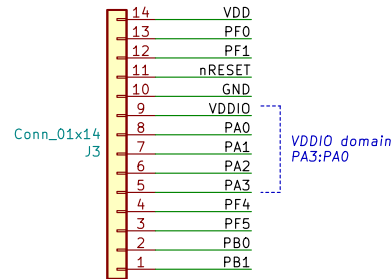
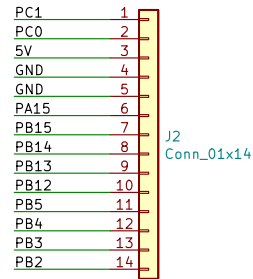
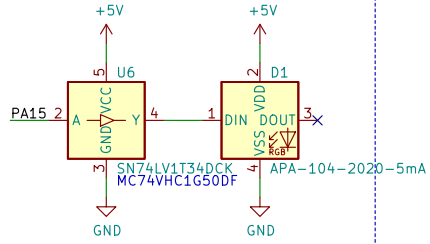
Rev: 1.0.0

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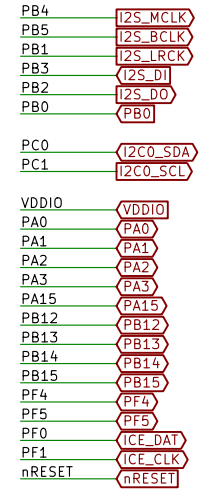
## Power



## RGB LED



## Off page connection



## VDDIO selection



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Sheet: /Pin header/  
File: file608CB110.sch

**Title: NuDAC**

Size: A4 Date: 2021-06-02

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**Rev: 1.0.0**

Id: 6/6