Hardware Specifications:

8-Bit Bus:

- 8 lines each being specific to one bit.
- Only 2 system blocks should be sending and receiving data at one time to prevent bus contention.
- When a module is sending data to the bus, all other outputs should be floating (use three-state buffers: 1, 0, or floating (disconnected)).

Clock:

- Square wave generated from 555 timer IC.
- 1000 mHz.
- 50 duty cycle.

Program Counter (PC):

- 4-bit counter that counts from 0000 to 1111, each going up by a binary bit.
- Sends the next memory location to the MAR.
- Increments after each instruction cycle.

Control bits:

- Program Counter Increment (ICR): Advances the program counter on the subsequent clock cycle.
- Program Counter Out (PO): Outputs the current program counter value onto the bus, disconnecting when CO is low.

Memory Address Register (MAR):

- 4-bit buffer register.
- Takes the memory location nibble from the PC (by bus) and sends it to the RAM through the address selector.

Control Bits:

- Memory Address In (MI): Stores the current bus values into the MAR that came from the program counter.

Input Unit:

- Control Panel used by the operator.
- 4 switches for clear and start.
- 2 switches for RAM.
- 1 switch for address selector.
- 4 switches for address.
- 8 switches for data.

Address Selector:

- RUN state when the microprocessor is running, it will give RAM memory location from the MAR.
- PROG state when the operator is programming, it will give RAM memory location from the operator.

Random Access Memory (RAM):

- RAM size 16x8 (16 memory locations each storing 1 byte).

Control Bits:

- RAM Out (RO): Outputs the selected RAM byte onto the bus, disconnecting when RO is low.

Accumulator A:

- 8-bit buffer register.
- Used as A byte within the adder-subtractor.
- Used to store the output of the adder-subtractor (hence the name accumulator).

Control Bits:

- Accumulator In (AI): Stores bus input into the accumulator.
- Accumulator Out (AO): Outputs the accumulator's contents onto the bus.

Register TMP:

- 8-bit buffer register.
- Used as the temporary register for the adder-subtractor.
- Not a general register.
- Used as B byte within the adder-subtractor.

Control Bits:

- Register TMP In (TI): Stores bus input into the TMP Register.

Register B:

- 8-bit buffer register.
- Used as a general register.

Control Bits:

- Register B In (BI): Stores bus input into the accumulator.
- Register B Out (BO): Outputs register B's contents onto the bus.

Register C:

- 8-bit buffer register
- Used as a general register

Control Bits:

- Register C In (CI): Stores bus input into the C Register.

- Register C Out (CO): Outputs register C's contents onto the bus.

Arithmetic and Logic Unit (ALU):

- Performs 8-bit binary addition and subtraction through inputs A and B.

Control Bits:

- Subtraction Select (SU): Activates subtraction mode when high.
- ALU Out (OO): Outputs the ALU result onto the bus, disconnecting when OO is low.

Output Register:

- Also known as output port.
- 8-bit buffer register.
- Stores the results from the accumulator through the bus to display when requested.
- Can be connected to any display module (ideally with light emitting diodes (LEDs) because of how simple this microprocessor is).

Control Bits:

- Output Register In (OI): Stores bus contents into the output register.

Instruction Register (IR):

- Stores the 8-bit instruction from the RAM.
- This 8-bit data is split into two nibbles (nibble is half a byte; 4 bits).
- The upper nibble (I7, I6, I5, I4) goes into the controller-sequencer.
- The lower nibble is sent to the bus (I3, I2, I1, I0).

Control Bits:

- Instruction Register In (II): Stores bus contents into the Instruction Register.
- Instruction Register Out (IO): Outputs the lower nibble onto the bus.
- Note: The upper nibble (op code) is sent to the controller sequencer instantaneously, not dependent on the IO micro-instruction.

Controller-Sequencer:

- Generates control signals on each T state, coordinating processor operations.
- Control Bits (ICR RO AI AO OO SU TI BO BO CI CO OI MI RO II IO)
- Determines subsequent actions of all processor blocks on the next positive CLK edge. Additionally, it emits a HLT (halt) signal to cease computing by halting the main clock.