UNIVERSITY OF TEHRAN

Report for Computer Assignment 5

State Machine Coding, Pre- and Post-Synthesis

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Danial Saeedi

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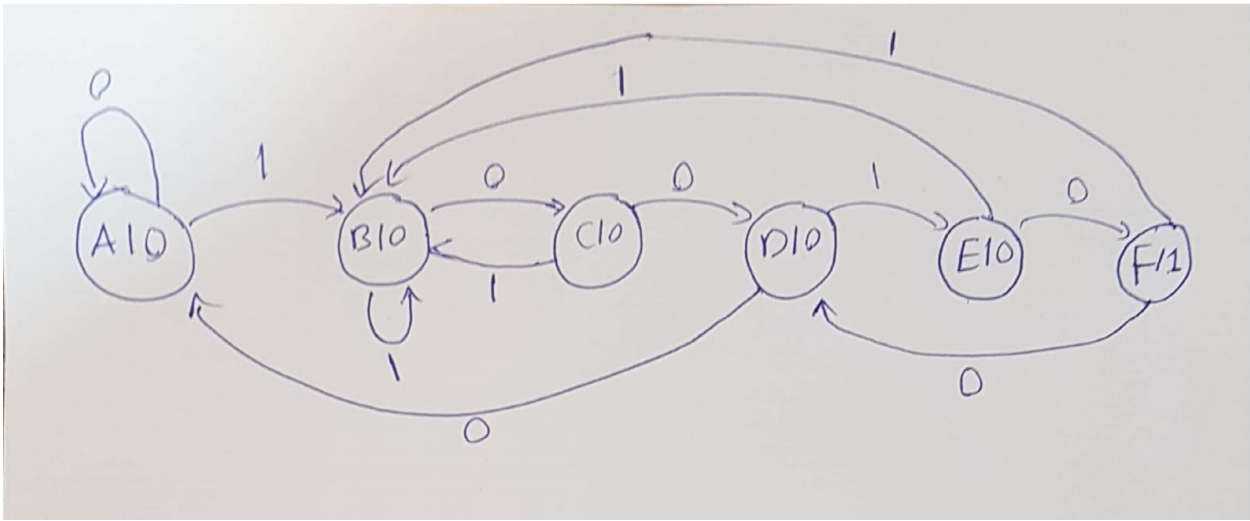
Problem a: 10010 detector

Moore State Diagram



Verilog Code

```verilog
`timescale 1ns/1ns
module moore10010(input clk,rst,j, output w);
    reg [2:0] ns,ps;
    parameter [2:0] A = 3'b0,B = 3'b001,C = 3'b010,D = 3'b011,E = 3'b100,F = 3'b101;
    //Combinational
    always @(ps,j) begin
        ns = A;
        case(ps)
            A : ns = j ? B : A;
            B : ns = j ? B : C;
            C : ns = j ? B : D;
            D : ns = j ? E : A;
            E : ns = j ? B : F;
            F : ns = j ? B : D;
            default: ns = A;
        endcase
    end

    assign w = (ps == F) ? 1'b1 : 1'b0;

    //Sequential
    always @(posedge clk,posedge rst) begin
        if(rst)
            ps <= A;
        else
            ps <= ns;
    end
endmodule
```

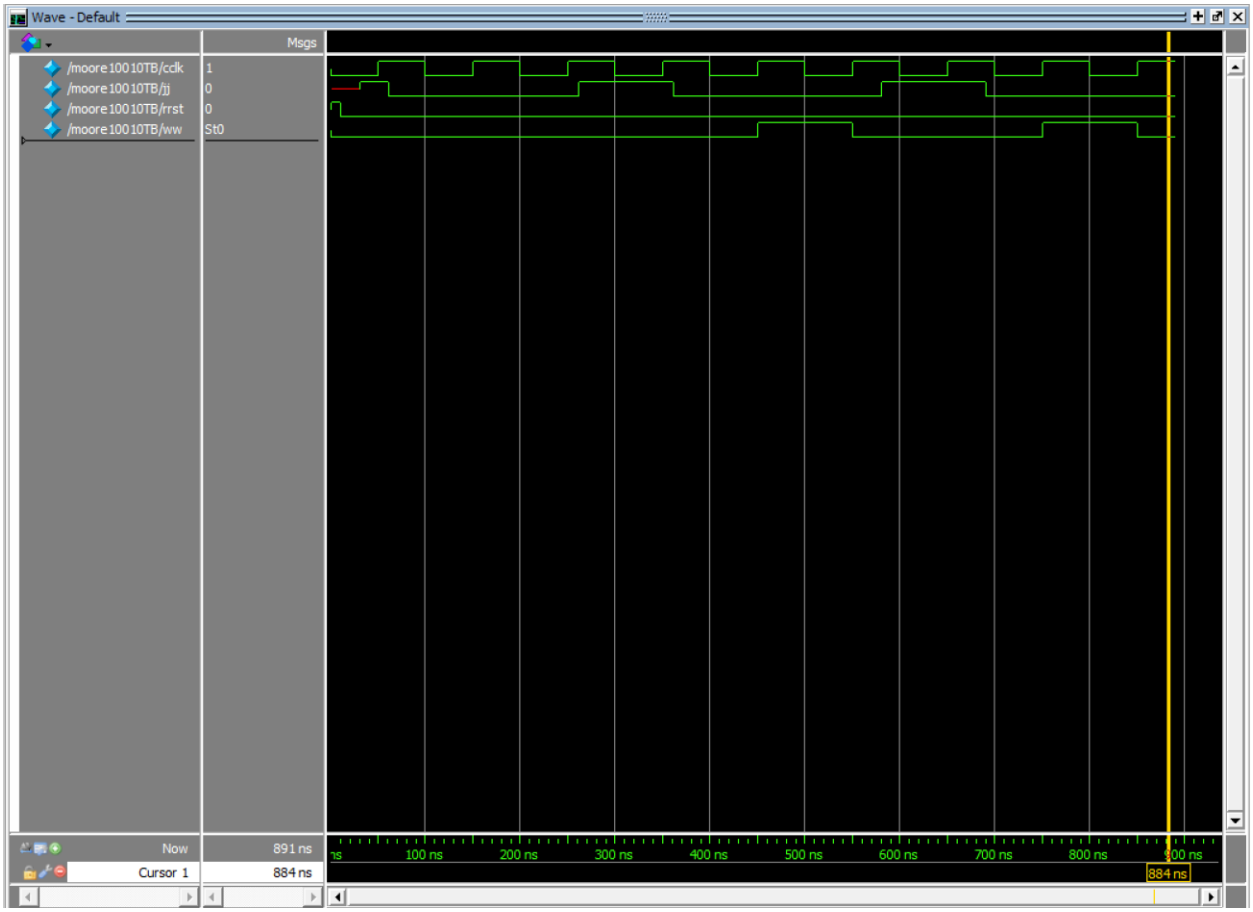
`

Part i.

Testbench

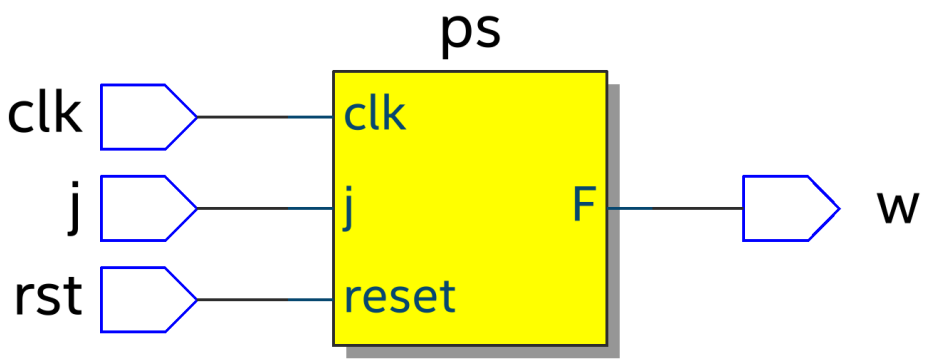
```
1  `timescale 1ns/1ns
2  module moore10010TB();
3      reg cclk = 0,jj,rrst;
4      wire ww;
5      moore10010 CUT1(cclk,rrst,jj,ww);
6      always #50 cclk = ~cclk;
7      initial begin
8          #1 rrst = 1;
9          #10 rrst = 0;
10         #20 jj = 1;
11         #30 jj = 0;
12         #200 jj = 1;
13         #100 jj = 0;
14         #110 jj = 0;
15         #110 jj = 1;
16         #110 jj = 0;
17
18         #200 $stop;
19     end
20 endmodule
```

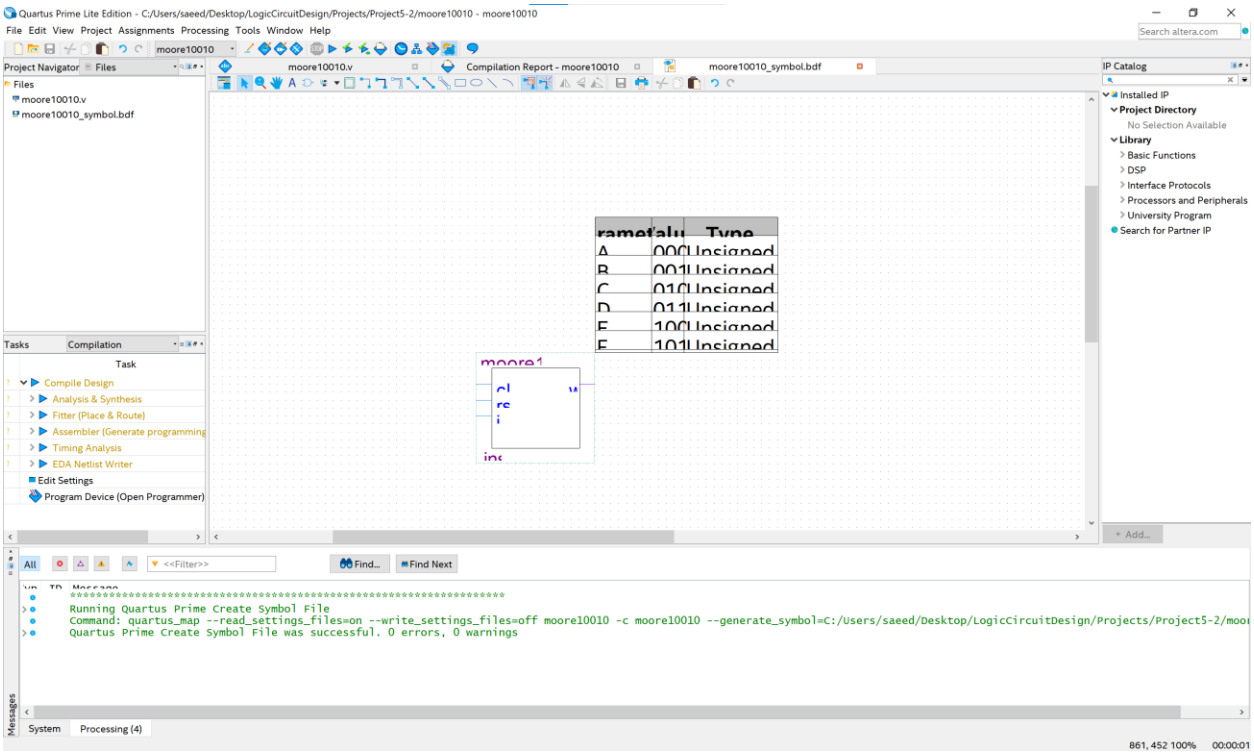
Simulation Result



`

Part ii.


ps
clk
j
rst
clk
j
reset
F
w


Quartus Prime Lite Edition - C:/Users/saeed/Desktop/LogicCircuitDesign/Projects/Project5-2/moore10010 - moore10010
File Edit View Project Assignments Processing Tools Window Help
moore10010.v
Compilation Report - moore10010
moore10010_symbol.bdf
Project Navigator
Files
moore10010.v
moore10010_symbol.bdf
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Running Quartus Prime Create Symbol File
Command: quartus_map --read_settings_files=on --write_settings_files=off moore10010 -c moore10010 --generate_symbol=C:/Users/saeed/Desktop/LogicCircuitDesign/Projects/Project5-2/moo
Quartus Prime Create Symbol File was successful. 0 errors, 0 warnings
System
Processing (4)

`

Flow Summary

<<Filter>>

Flow Status	Successful - Fri Jun 11 13:25:04 2021
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	moore10010
Top-level Entity Name	moore10010
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	5 / 14,400 (< 1 %)
Total registers	5
Total pins	4 / 81 (5 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

`

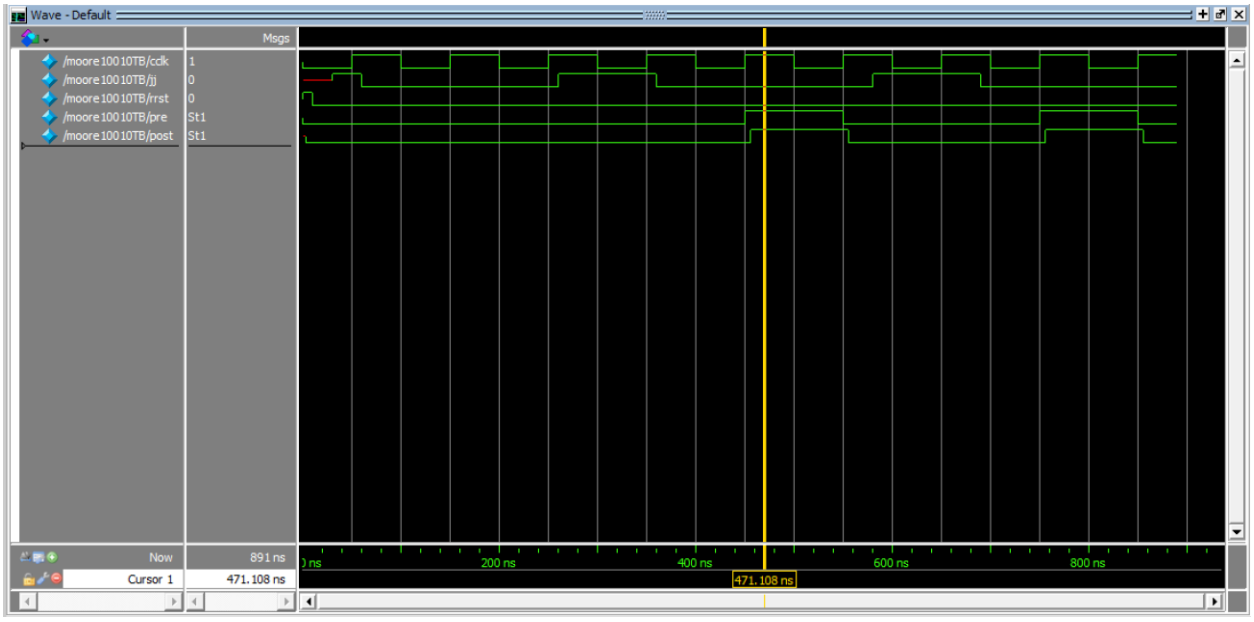
Part iii.

Testbench

```
`timescale 1ps/1ps
module moore10010TB();
    reg cclk = 0,jj,rrst;
    wire pre;
    wire post;
    moore10010 CUT1(cclk,rrst,jj,pre);
    moore10010_synth CUT2(cclk,rrst,jj,post);
    always #50 cclk = ~cclk;
    initial begin
        #1 rrst = 1;
        #10 rrst = 0;
        #20 jj = 1;
        #30 jj = 0;
        #200 jj = 1;
        #100 jj = 0;
        #110 jj = 0;
        #110 jj = 1;
        #110 jj = 0;

        #200 $stop;
    end
endmodule
```

Simulation Result



As you can see, the waveform of pre and post synthesis are the same.

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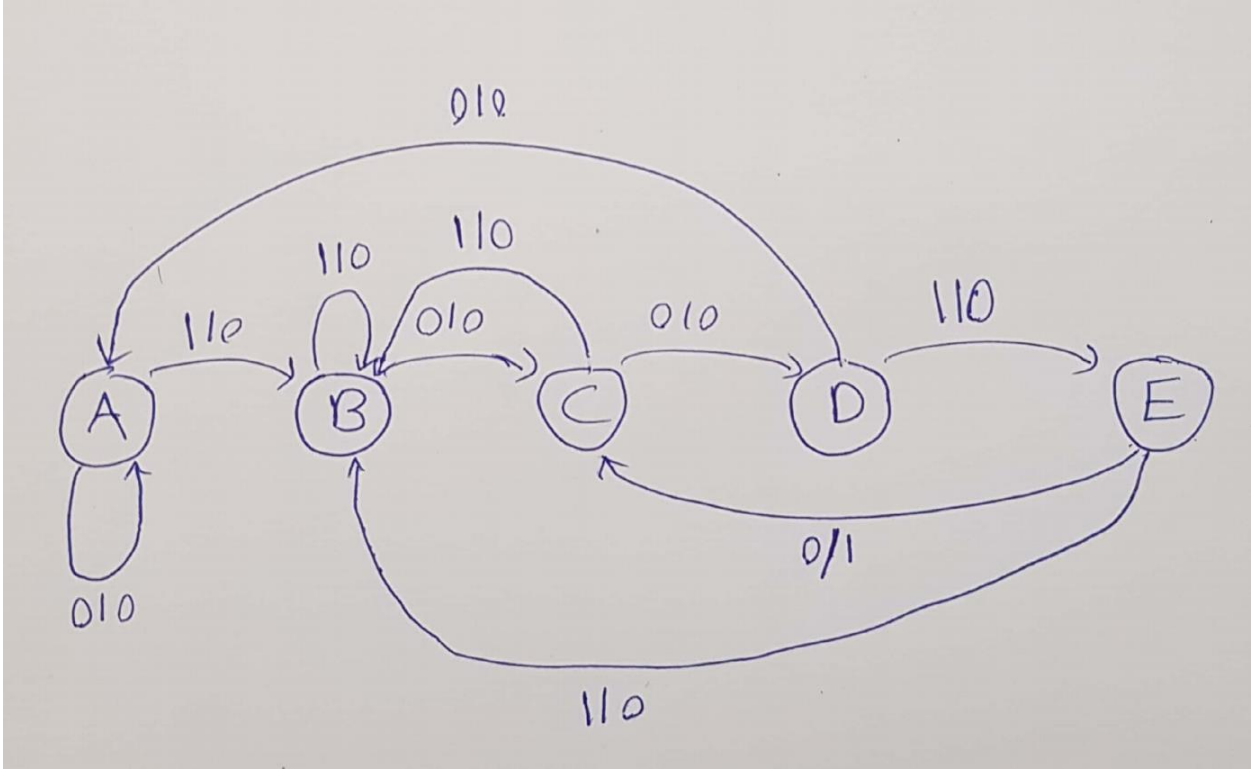
Problem b: 10010 detector

Mealy State Diagram



Verilog Code

```verilog
`timescale 1ps/1ps
module mealy10010(input clk,rst,j, output w);
    reg [2:0] ns,ps;
    parameter [2:0] A = 3'b0,B = 3'b001,C = 3'b010,D = 3'b011,E = 3'b100;

    //Combinational
    always @(ps,j) begin
        ns = A;
        case(ps)
            A : ns = j ? B : A;
            B : ns = j ? B : C;
            C : ns = j ? B : D;
            D : ns = j ? A : E;
            E : ns = j ? B : C;
            default: ns = A;
        endcase
    end

    assign w = (ps == E) ? ~j : 1'b0;

    //Sequential
    always @(posedge clk,posedge rst) begin
        if(rst)
            ps <= A;
        else
            ps <= ns;
    end
endmodule
```

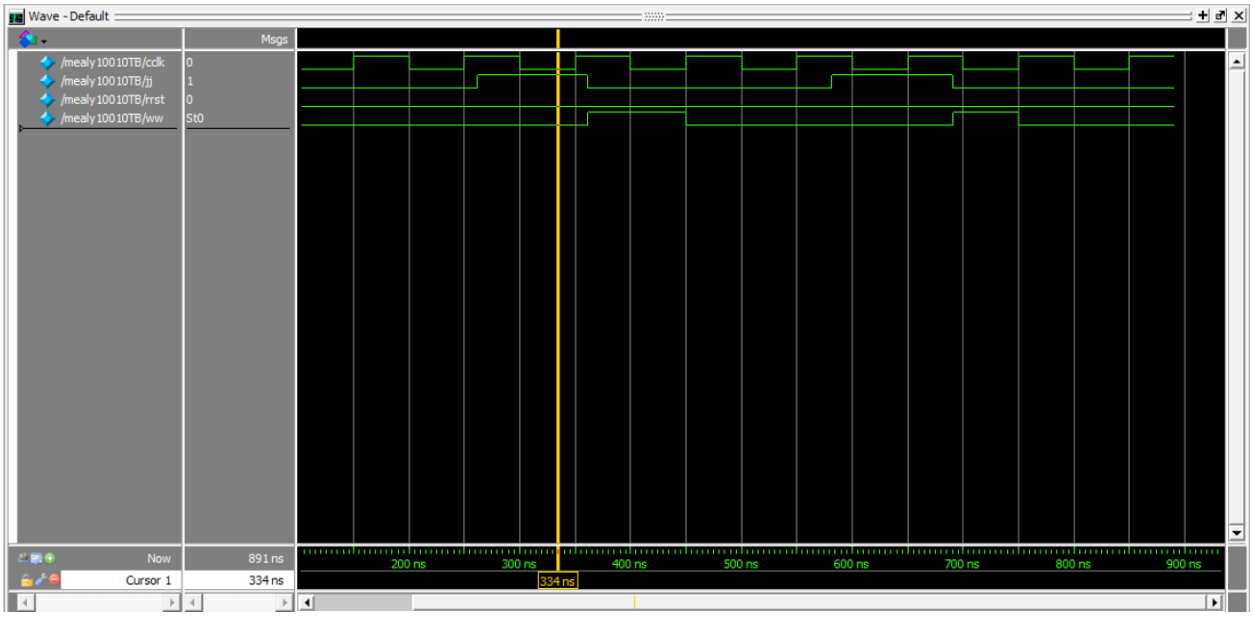
`

Part i.

Testbench

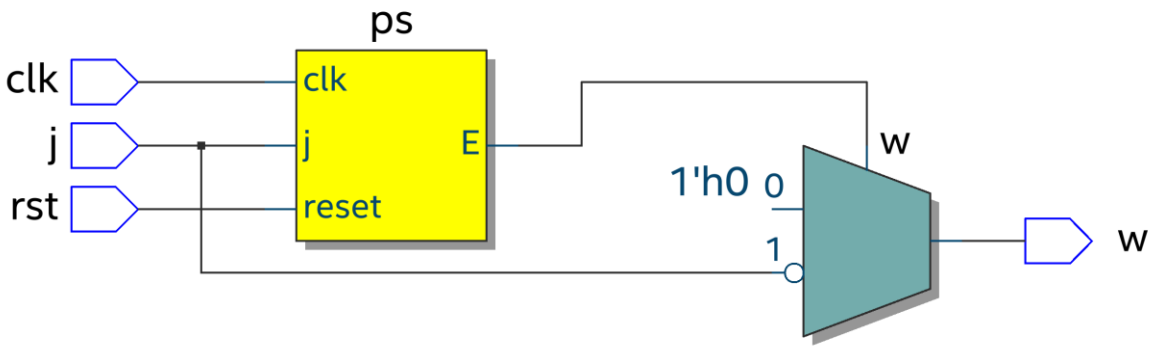
```
1  `timescale 1ns/1ns
2  module mealy10010TB();
3      reg cclk = 0,jj,rrst;
4      wire ww;
5      mealy10010 CUT1(cclk,rrst,jj,ww);
6      always #50 cclk = ~cclk;
7      initial begin
8          #1 rrst = 1;
9          #10 rrst = 0;
10         #20 jj = 1;
11         #30 jj = 0;
12         #200 jj = 1;
13         #100 jj = 0;
14         #110 jj = 0;
15         #110 jj = 1;
16         #110 jj = 0;
17
18         #200 $stop;
19     end
20 endmodule
```

Simulation Result



`

Part ii.



Flow Summary	
<<Filter>>	
Flow Status	Successful - Fri Jun 11 16:54:25 2021
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
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Top-level Entity Name	mealy10010
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	5 / 14,400 (< 1 %)
Total registers	4
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Total virtual pins	0
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Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

`

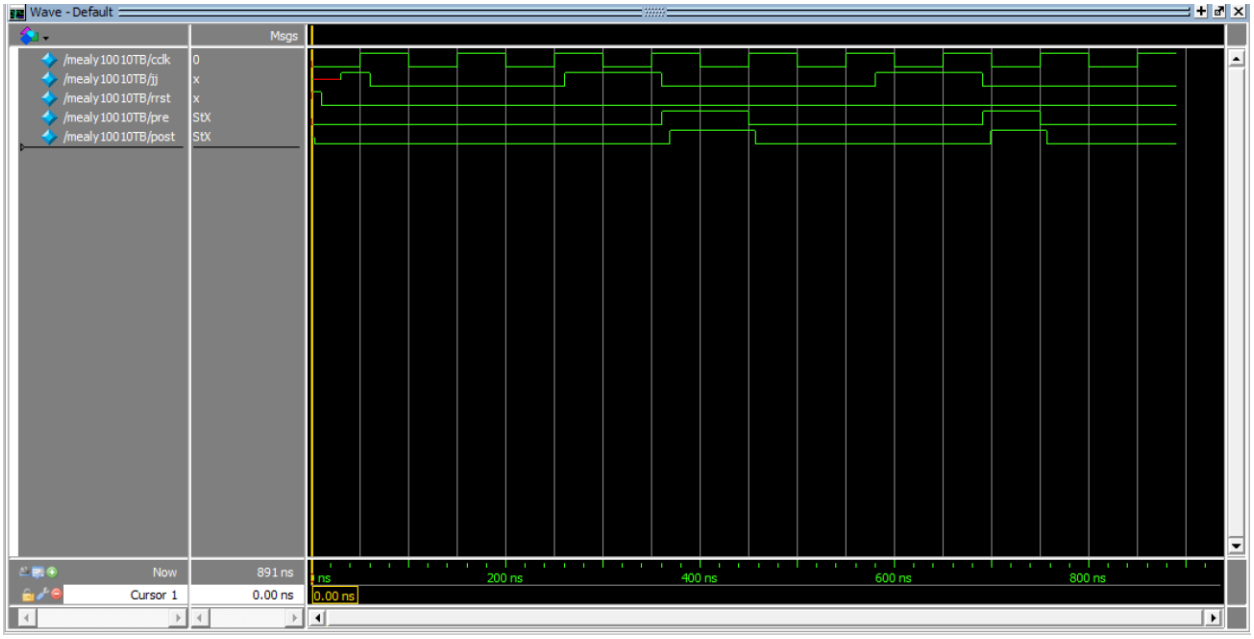
Part iii.

Testbench

```
`timescale 1 ns/ 1 ps
module mealy10010TB();
    reg cclk = 0,jj,rrst;
    wire pre;
    wire post;
    mealy10010_pre CUT1(cclk,rrst,jj,pre);
    mealy10010 CUT2(cclk,rrst,jj,post);
    always #50 cclk = ~cclk;
    initial begin
        #1 rrst = 1;
        #10 rrst = 0;
        #20 jj = 1;
        #30 jj = 0;
        #200 jj = 1;
        #100 jj = 0;
        #110 jj = 0;
        #110 jj = 1;
        #110 jj = 0;

        #200 $stop;
    end
endmodule
```

Simulation Result



As you can see, the waveform of pre and post synthesis are the same.

`

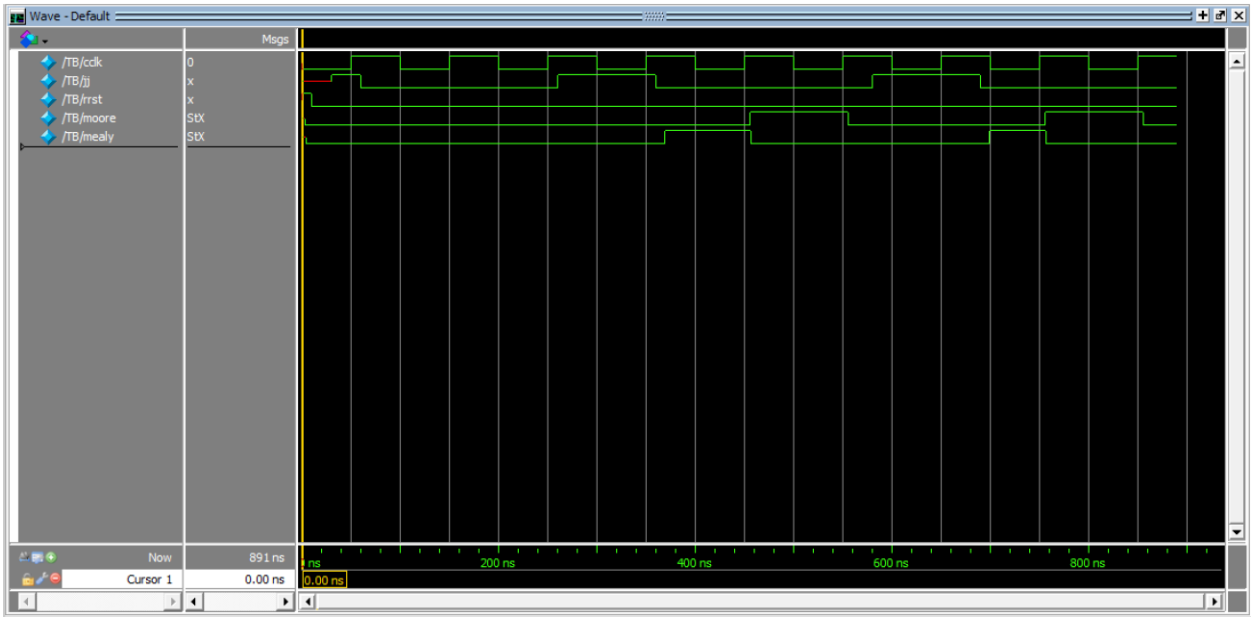
Problem C: Compare Moore and Mealy Machine

Testbench

TB.v

```
1  `include "../simulation/modelsim/moore10010.vo"
2  `include "../mealy/simulation/modelsim/mealy10010.vo"
3  `timescale 1 ns/ 1 ps
4  module TB();
5      reg cclk = 0,jj,rrst;
6      wire moore;
7      wire mealy;
8      moore10010 CUT1(cclk,rrst,jj,moore);
9      mealy10010 CUT2(cclk,rrst,jj,mealy);
10     always #50 cclk = ~cclk;
11     initial begin
12         #1 rrst = 1;
13         #10 rrst = 0;
14         #20 jj = 1;
15         #30 jj = 0;
16         #200 jj = 1;
17         #100 jj = 0;
18         #110 jj = 0;
19         #110 jj = 1;
20         #110 jj = 0;
21
22         #200 $stop;
23     end
24 endmodule
```

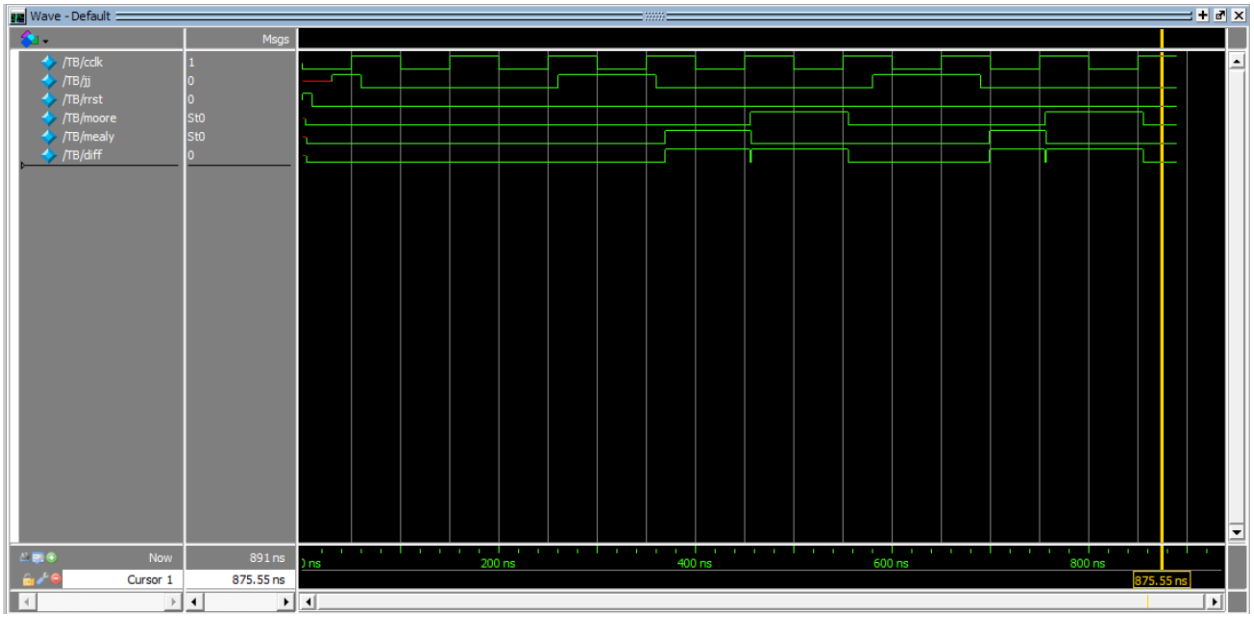
Simulation Result



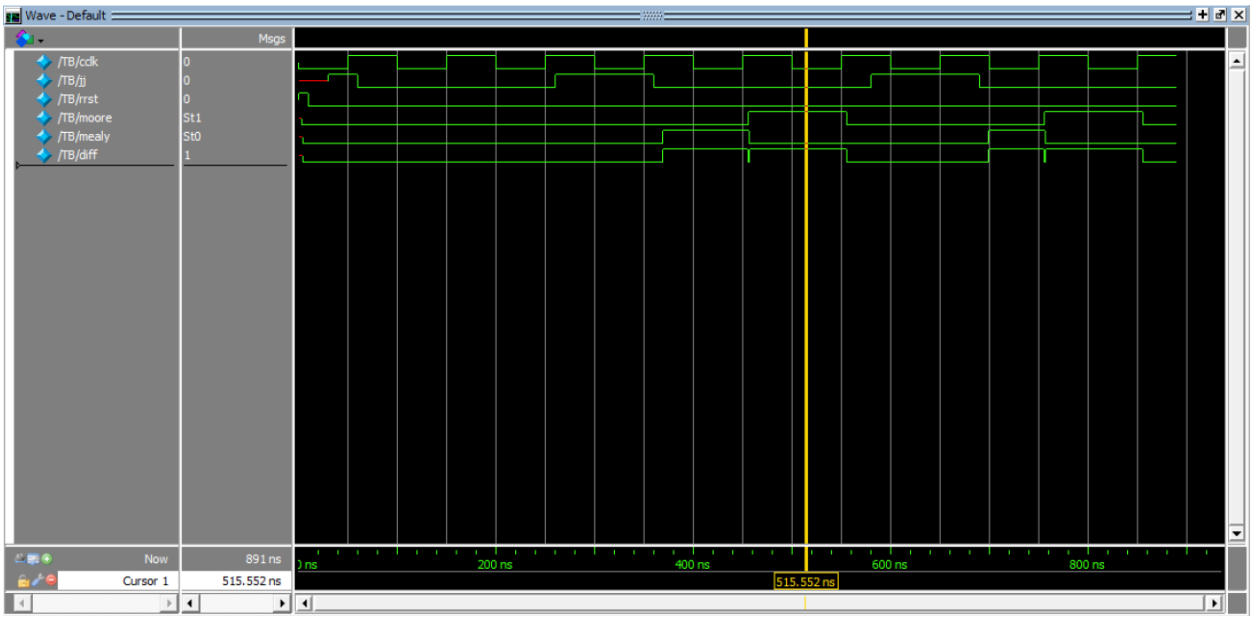
`

Part i.

```
10      reg diff;
11      assign diff = moore ^ mealy;
```



Part ii.

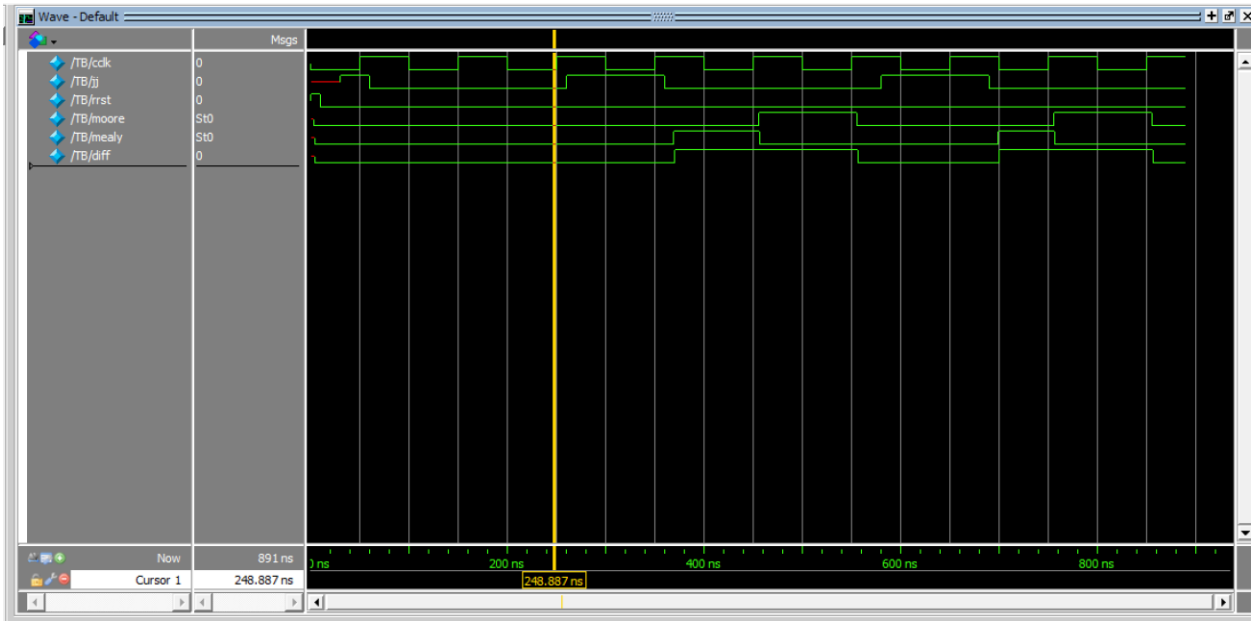


`

Part iii.

By adding delay to diff, the differences are due to changes on the inputs only:

```
11
12      assign #1 diff = moore ^ mealy;
13
```



As you can see there is no glitch anymore.