UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367, ECE 894, Spring 1399-1400

Homework 2

Transistor Switches

Name:	**Date:**
Username:	

1. A 2-input XOR gate output becomes 1 when the inputs are different, i.e., a=0 and b=0, or a=1 and b=0. Another way of saying this is to say that the output of an XOR gate is 0 when its two inputs are the same. Show complex gate structure for an XOR gate (w = a'.b + a'.b). Show switch level structures for the inverters where needed.

2. Given nMOS and pMOS delays as #(3,5,7) and #(5,7,9), show switch level Verilog description of an XOR gate.

3. Given nMOS and pMOS delays as #(3,5,7) and #(5,7,9), calculate worst case delay of an XOR gate as discussed in Problem 1. Show how this gate is represented in Verilog.

4. Given nMOS and pMOS delays as #(3,5,7) and #(5,7,9), calculate worst case delay of a 4-input NOR gate. Show how this gate is represented in Verilog.

5. Two 4-bit numbers A[3:0] and B[3:0] are equal if all their bits are equal. You can build a 4-bit comparator by using gates discussed above. Show gate level structure of this circuit.

6. Write Verilog description of the circuit of Problem 5 using gates developed and described in Problems 3 and 4.

7. Start with a pass-transistor implementation of a 2-to-1 Mux, and develop the following gates:
   a. An AND gate
   b. An OR gate
   c. A NOT gate
   d. An XOR gate

8. Using gates of the above problem, show implementation of the Overflow circuit as discussed in class. Find the number of transistors and the worst case delay of the circuit for nMOS and pMOS delay values of #(3,4,5) and #(5,6,7).

9. Using gates of Problem 7, show a 2-bit comparator whose output becomes 1 when both inputs are equal. Find the number of transistors and the worst case delay of the circuit for nMOS and pMOS delay values of #(3,4,5) and #(5,6,7).