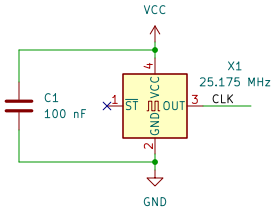
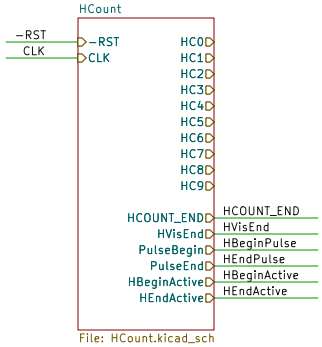
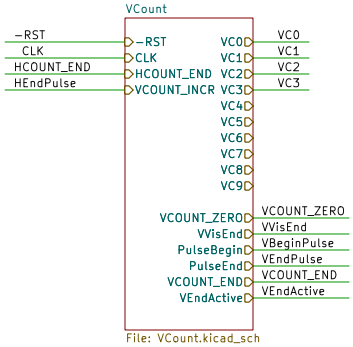
Oscillator module to produce
25.175 MHz VGA dot clock



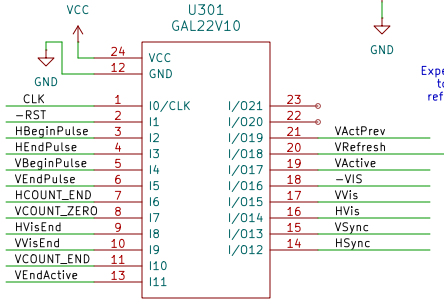
Horizontal count

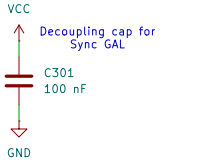


Vertical count



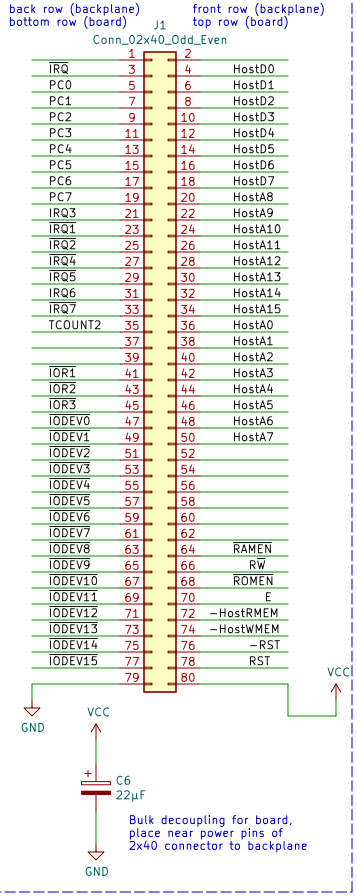
Sync gen and visibility signals:
Logic is in Sync.pld



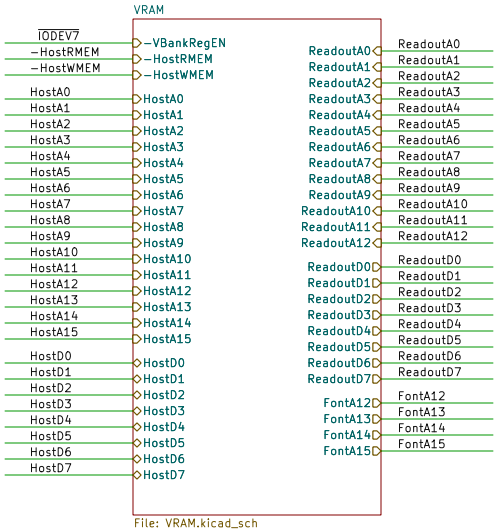


Experimental: place jumper
to generate a vertical
refresh interrupt as IRQ6

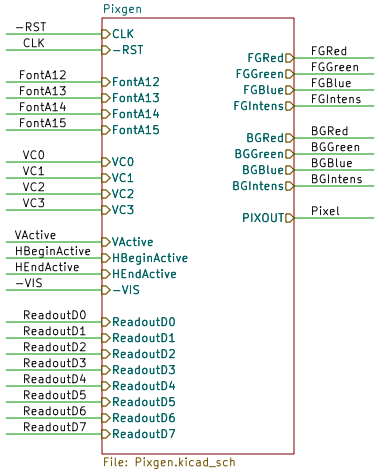
Backplane connector: one per board PCB
(appears here because all backplane signals
exist on this sheet)



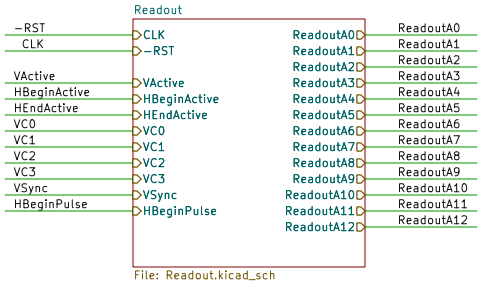
VRAM (video memory for
character and attribute data)



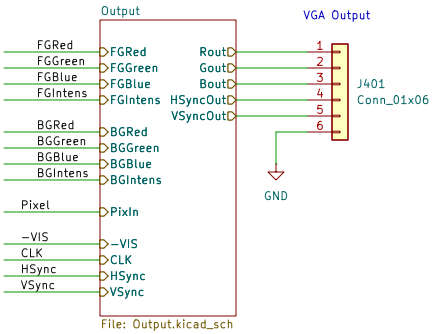
Pixel generation (using data from VRAM,
generate sequence of pixel fg/bg values
along with fg/bg color information
to send to Output module for display)



Readout module (generate addresses
for reading character and attribute
data from VRAM)



Video output
(to VGA monitor)

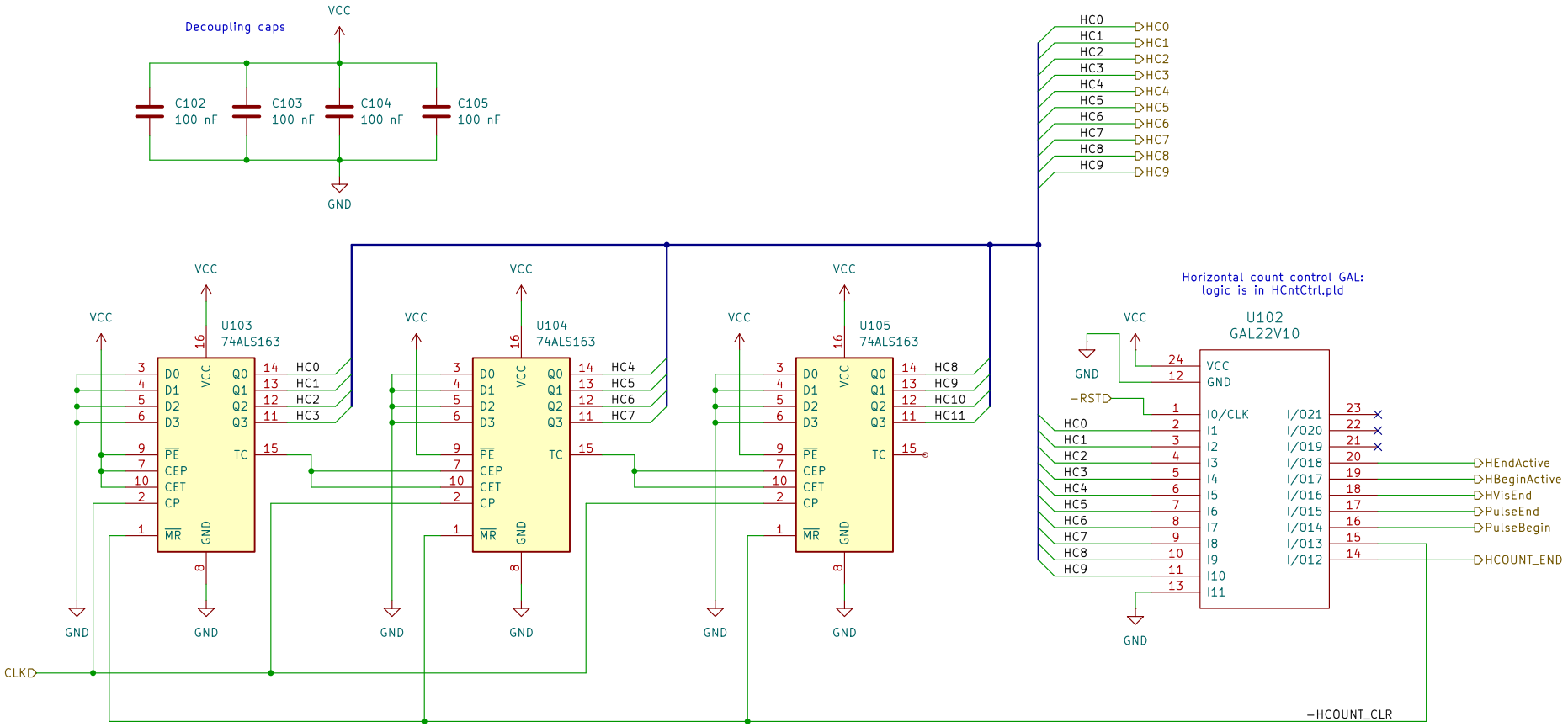


daveho hacks

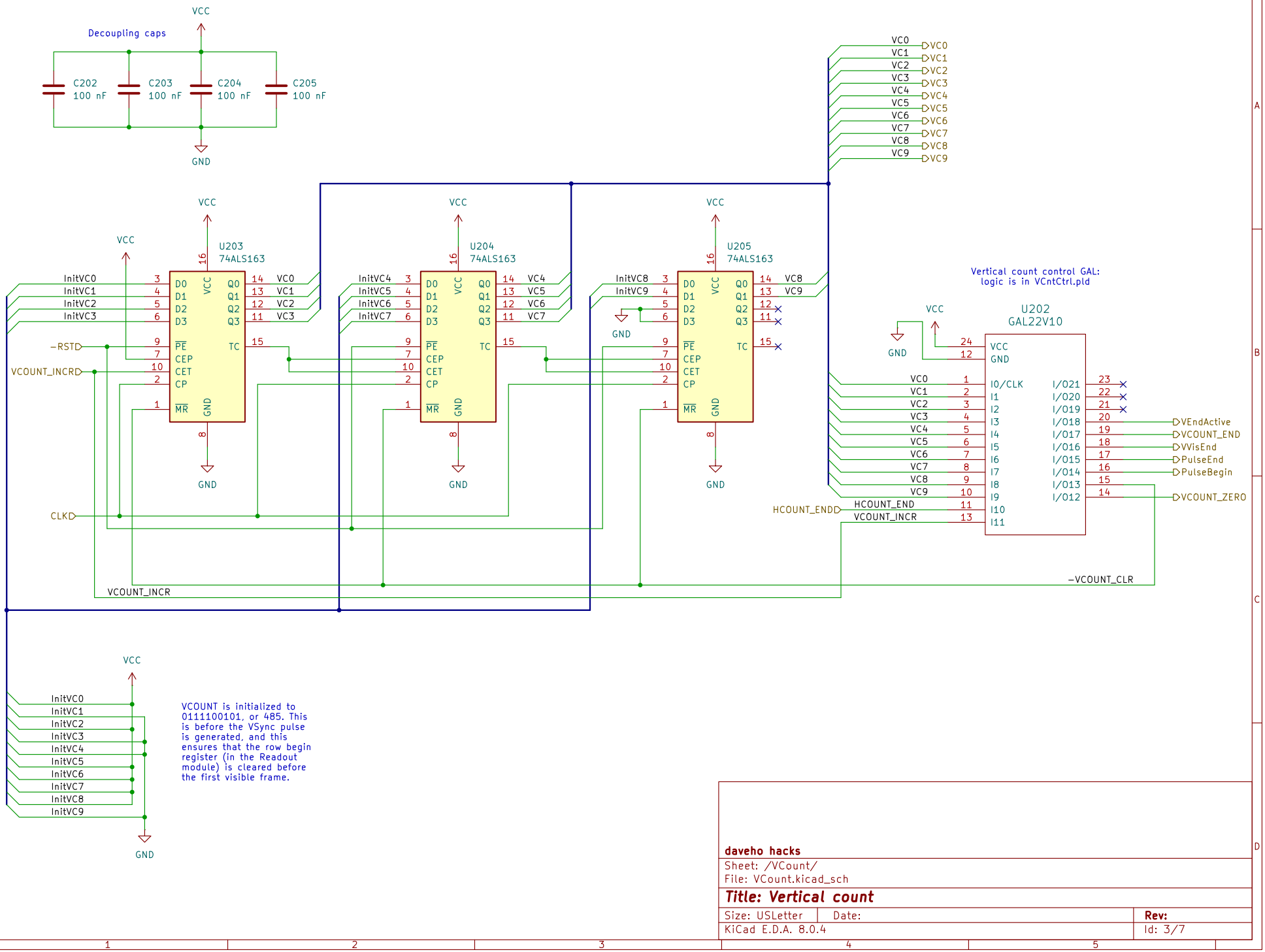
Sheet: /
File: HW_VGA.kicad_sch

Title: Hardware VGA

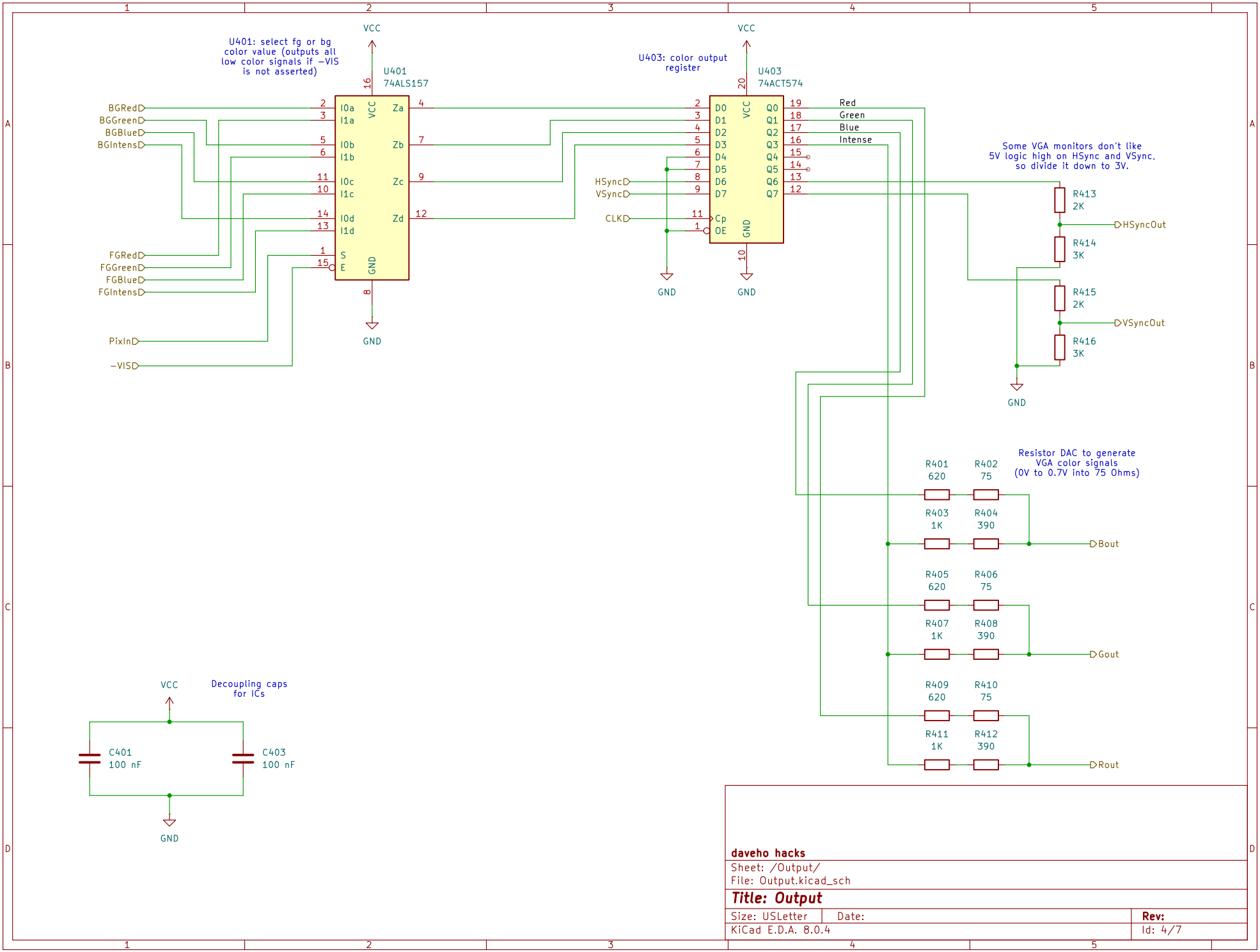
Size: User	Date:	Rev:
KiCad E.D.A. 8.0.4		Id: 1/7

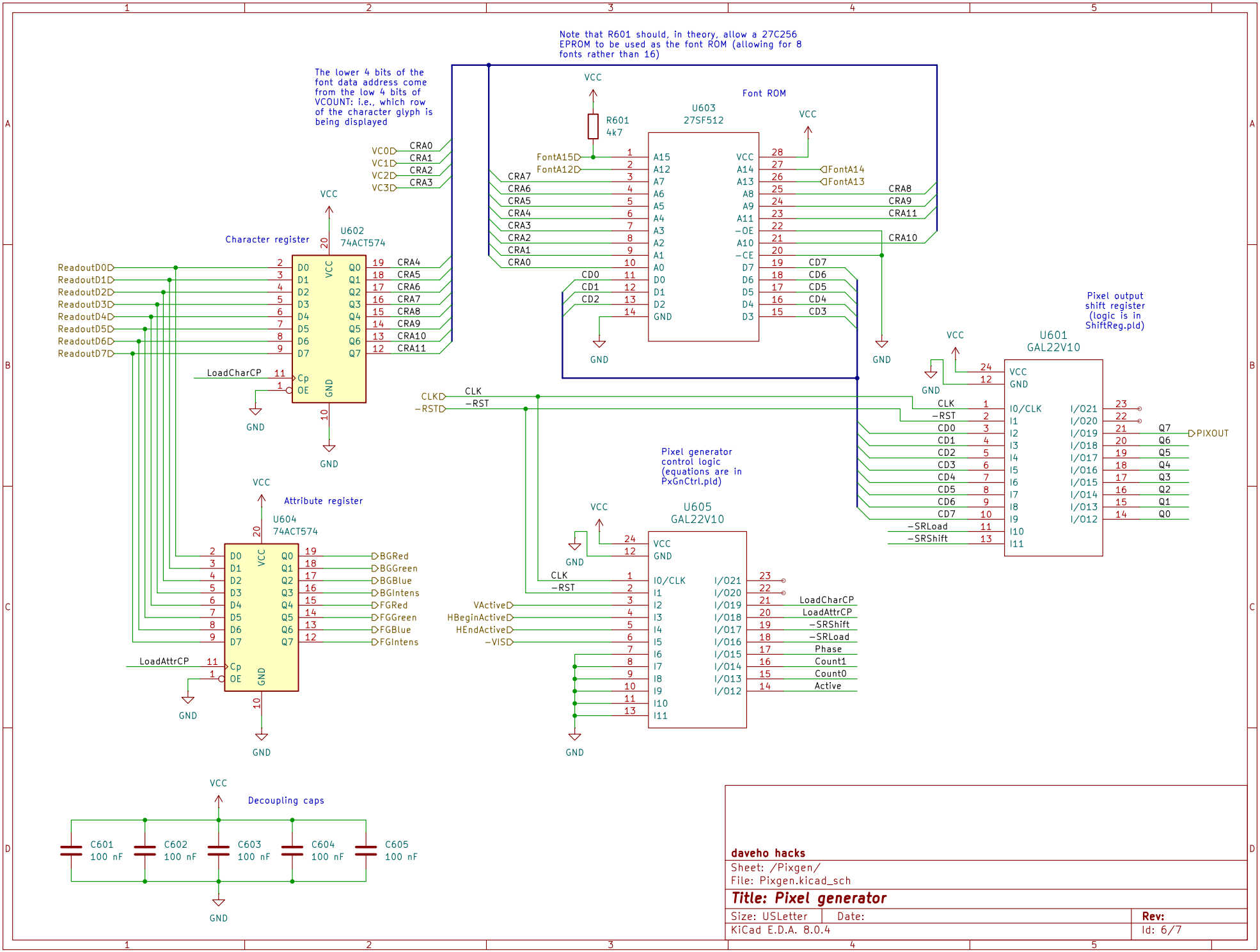


daveho hacks		
Sheet: /HCount/		
File: HCount.kicad_sch		
Title: Horizontal count		
Size: USLetter	Date:	**Rev:**
KiCad E.D.A. 8.0.4		Id: 2/7

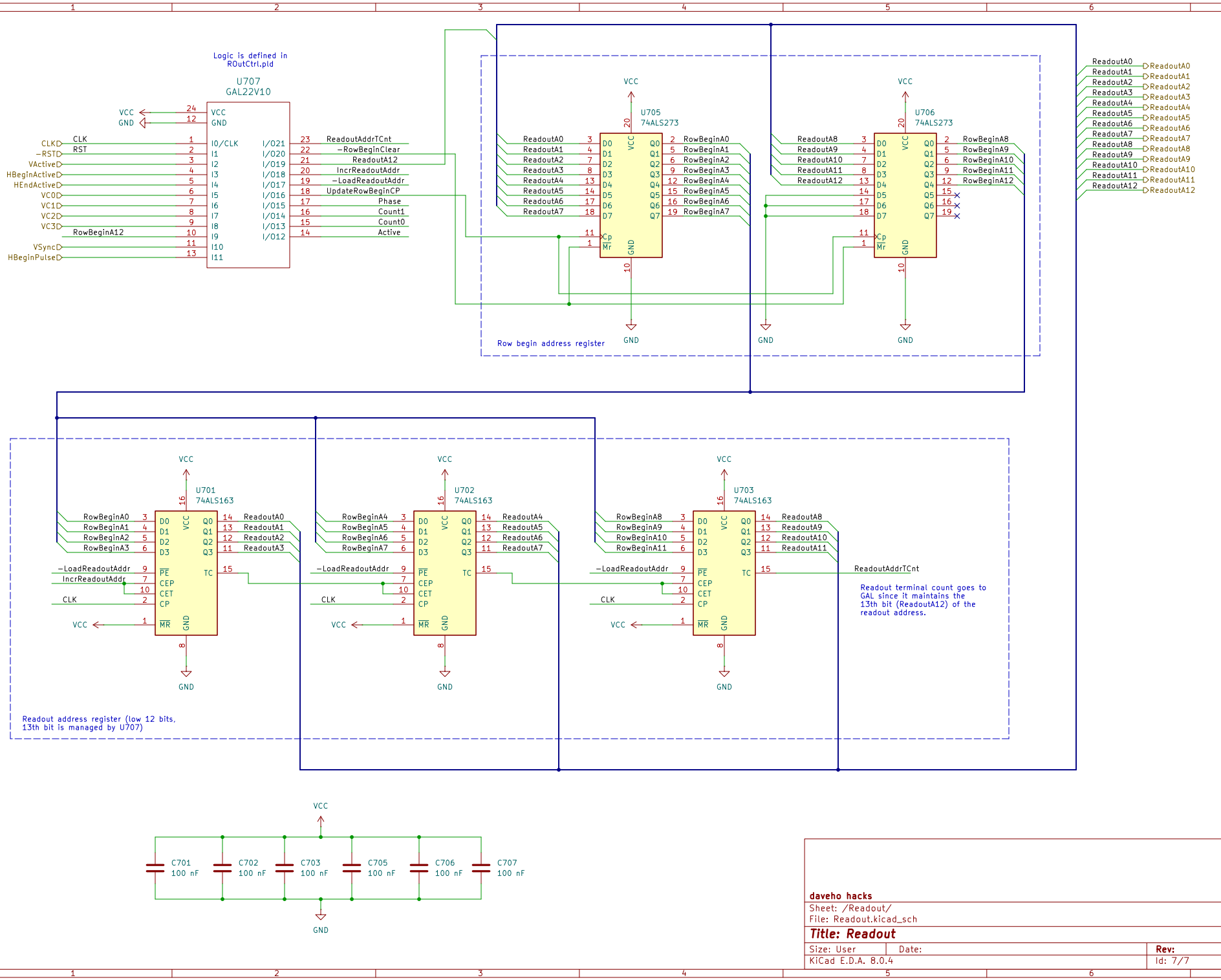


daveho hacks	
Sheet: /VCount/	
File: VCount.kicad_sch	
Title: Vertical count	
Size: USLetter | Date:	**Rev:**
KiCad E.D.A. 8.0.4	Id: 3/7

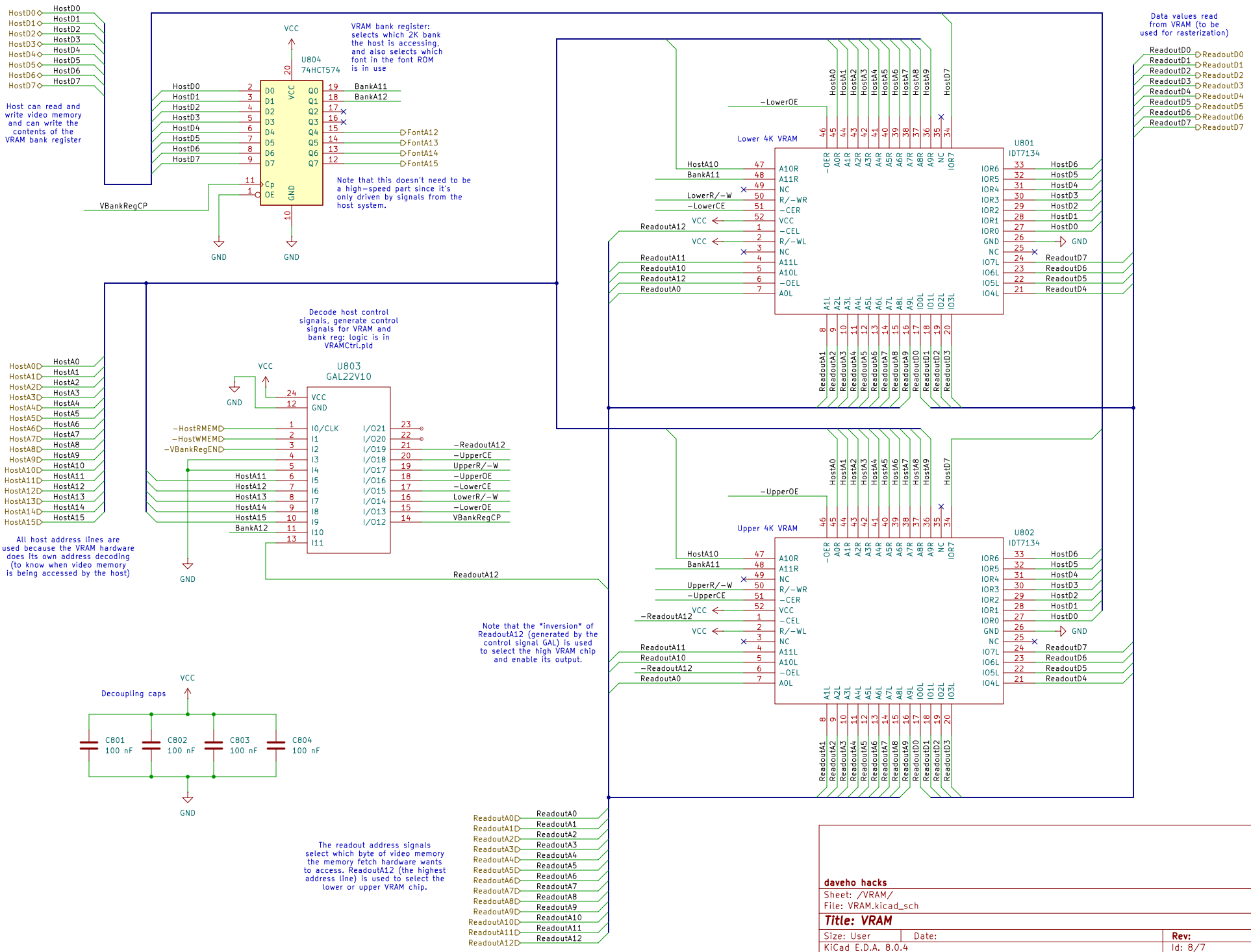

U401: select fg or bg color value (outputs all low color signals if −VIS is not asserted)
U401
74ALS157
U403: color output register
U403
74ACT574
BGRed
BGGreen
BGBlue
BGIntens
FGRed
FGGreen
FGBlue
FGIntens
PixIn
−VIS
HSync
VSync
CLK
Red
Green
Blue
Intense
Some VGA monitors don't like 5V logic high on HSync and VSync, so divide it down to 3V.
R413 2K
R414 3K
R415 2K
R416 3K
HSyncOut
VSyncOut
Resistor DAC to generate VGA color signals (0V to 0.7V into 75 Ohms)
R401 620
R402 75
R403 1K
R404 390
R405 620
R406 75
R407 1K
R408 390
R409 620
R410 75
R411 1K
R412 390
Bout
Gout
Rout
Decoupling caps for ICs
C401 100 nF
C403 100 nF
VCC
GND
daveho hacks
Sheet: /Output/
File: Output.kicad_sch
Title: Output
Size: USLetter
Date:
Rev:
KiCad E.D.A. 8.0.4
Id: 4/7



daveho hacks	
Sheet: /Pixgen/	
File: Pixgen.kicad_sch	
Title: Pixel generator	
Size: USLetter | Date:	**Rev:**
KiCad E.D.A. 8.0.4	Id: 6/7



daveho hacks	
Sheet: /Readout/	
File: Readout.kicad_sch	
Title: Readout	
Size: User	Date:
KiCad E.D.A. 8.0.4	Rev:
	Id: 7/7


HostD0
HostD1
HostD2
HostD3
HostD4
HostD5
HostD6
HostD7
Host can read and write video memory and can write the contents of the VRAM bank register
VCC
U804
74HCT574
VRAM bank register: selects which 2K bank the host is accessing, and also selects which font in the font ROM is in use
BankA11
BankA12
FontA12
FontA13
FontA14
FontA15
Cp
OE
GND
VBankRegCP
Note that this doesn't need to be a high-speed part since it's only driven by signals from the host system.
Data values read from VRAM (to be used for rasterization)
ReadoutD0
ReadoutD1
ReadoutD2
ReadoutD3
ReadoutD4
ReadoutD5
ReadoutD6
ReadoutD7
Lower 4K VRAM
U801
IDT7134
-LowerOE
HostA0
HostA1
HostA2
HostA3
HostA4
HostA5
HostA6
HostA7
HostA8
HostA9
HostD7
HostA10
BankA11
LowerR/-W
-LowerCE
VCC
ReadoutA12
ReadoutA11
ReadoutA10
ReadoutA0
ReadoutA1
ReadoutA2
ReadoutA3
ReadoutA4
ReadoutA5
ReadoutA6
ReadoutA7
ReadoutA8
ReadoutA9
ReadoutD0
ReadoutD1
ReadoutD2
ReadoutD3
Decode host control signals, generate control signals for VRAM and bank reg; logic is in VRAMCtrl.pld
U803
GAL22V10
-HostRMEM
-HostWMEM
-VBankRegEN
HostA11
HostA12
HostA13
HostA14
HostA15
BankA12
-ReadoutA12
-UpperCE
UpperR/-W
-UpperOE
-LowerCE
LowerR/-W
VBankRegCP
All host address lines are used because the VRAM hardware does its own address decoding (to know when video memory is being accessed by the host)
Upper 4K VRAM
U802
IDT7134
-UpperOE
UpperR/-W
-UpperCE
-ReadoutA12
Note that the *inversion* of ReadoutA12 (generated by the control signal GAL) is used to select the high VRAM chip and enable its output.
Decoupling caps
C801
100 nF
C802
100 nF
C803
100 nF
C804
100 nF
The readout address signals select which byte of video memory the memory fetch hardware wants to access. ReadoutA12 (the highest address line) is used to select the lower or upper VRAM chip.
daveho hacks
Sheet: /VRAM/
File: VRAM.kicad_sch
Title: VRAM
Size: User
Date:
Rev:
KiCad E.D.A. 8.0.4
Id: 8/7