Module 1: core (CPU and glue logic)

CPUandGlueLogic

File: CPUandGlueLogic.kicad_sch

Module 2: memory and core peripherals

Memory

File: Memory.kicad_sch

CorePeriphs

File: CorePeriphs.kicad_sch

Module 3: interrupt controller

Interrupts

File: Interrupts.kicad_sch

Module 4: keyboard controller

Keyboard

File: Keyboard.kicad_sch

Module 5: TMS9918A/YM2149

TMS9918ADisplay

File: TMS9918ADisplay.kicad_sch

YM2149_Sound

File: YM2149_Sound.kicad_sch

Module 6: FPGA display controller

FPGADisplayController

File: FPGADisplayController.kicad_sch

Backplane connector: one per board PCB
(appears here because all backplane signals
exist on this sheet)

back row (backplane)
bottom row (board)

front row (backplane)
top row (board)

J001
Conn_02x40_Odd_Even

	1	2	
IRQ	3	4	D0
PC0	5	6	D1
PC1	7	8	D2
PC2	9	10	D3
PC3	11	12	D4
PC4	13	14	D5
PC5	15	16	D6
PC6	17	18	D7
PC7	19	20	A8
IRQ3	21	22	A9
IRQ1	23	24	A10
IRQ2	25	26	A11
IRQ4	27	28	A12
IRQ5	29	30	A13
IRQ6	31	32	A14
IRQ7	33	34	A15
TCOUNT2	35	36	A0
	37	38	A1
	39	40	A2
IOR1	41	42	A3
IOR2	43	44	A4
IOR3	45	46	A5
IODEV0	47	48	A6
IODEV1	49	50	A7
IODEV2	51	52	
IODEV3	53	54	
IODEV4	55	56	
IODEV5	57	58	
IODEV6	59	60	
IODEV7	61	62	
IODEV8	63	64	RAMEN
IODEV9	65	66	RW
IODEV10	67	68	ROMEN
IODEV11	69	70	E
IODEV12	71	72	RMEM
IODEV13	73	74	WMEM
IODEV14	75	76	RST
IODEV15	77	78	RST
	79	80	VCC

GND

VCC

C001
22µF

Bulk decoupling for board,
place near power pins of
2x40 connector to backplane

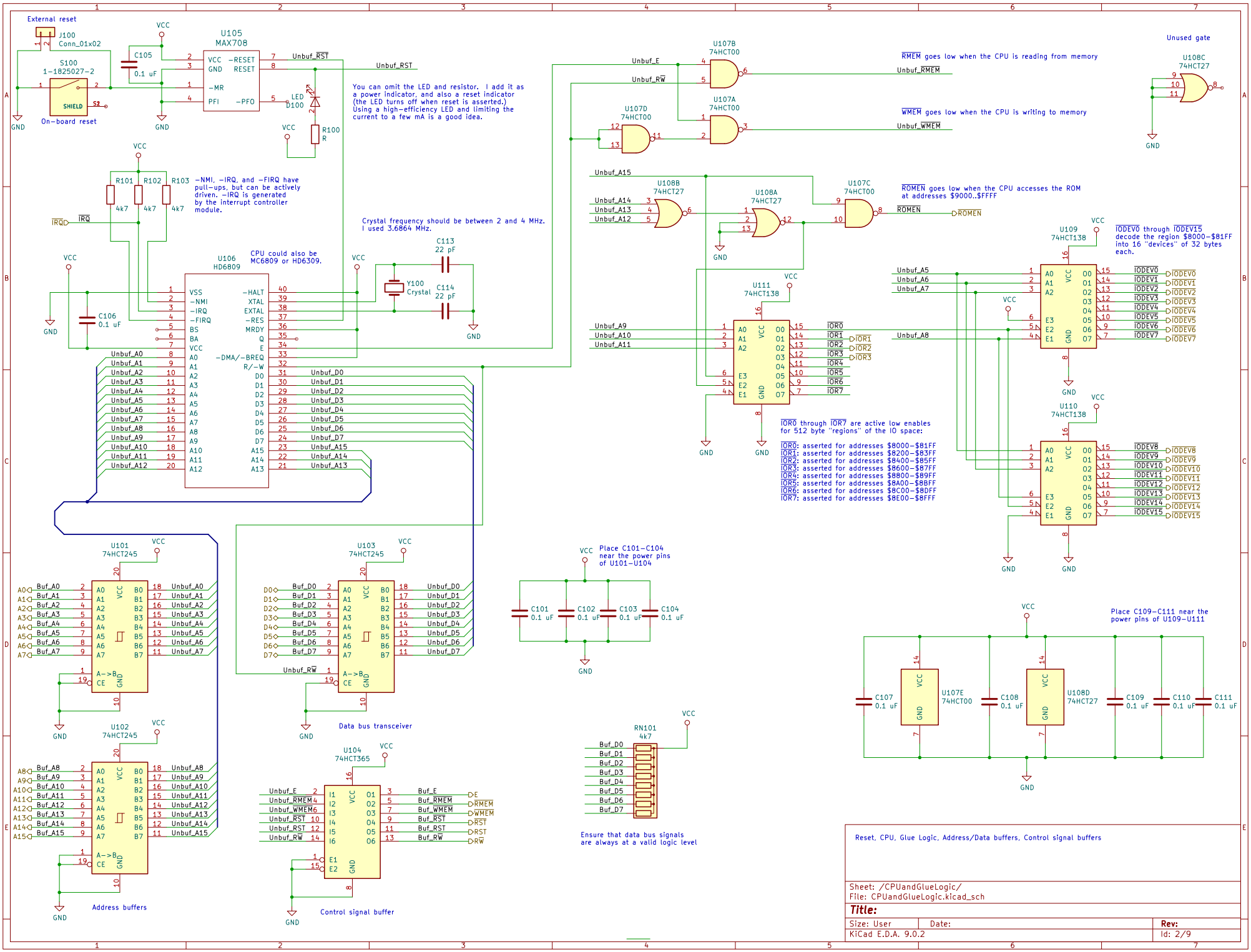
GND

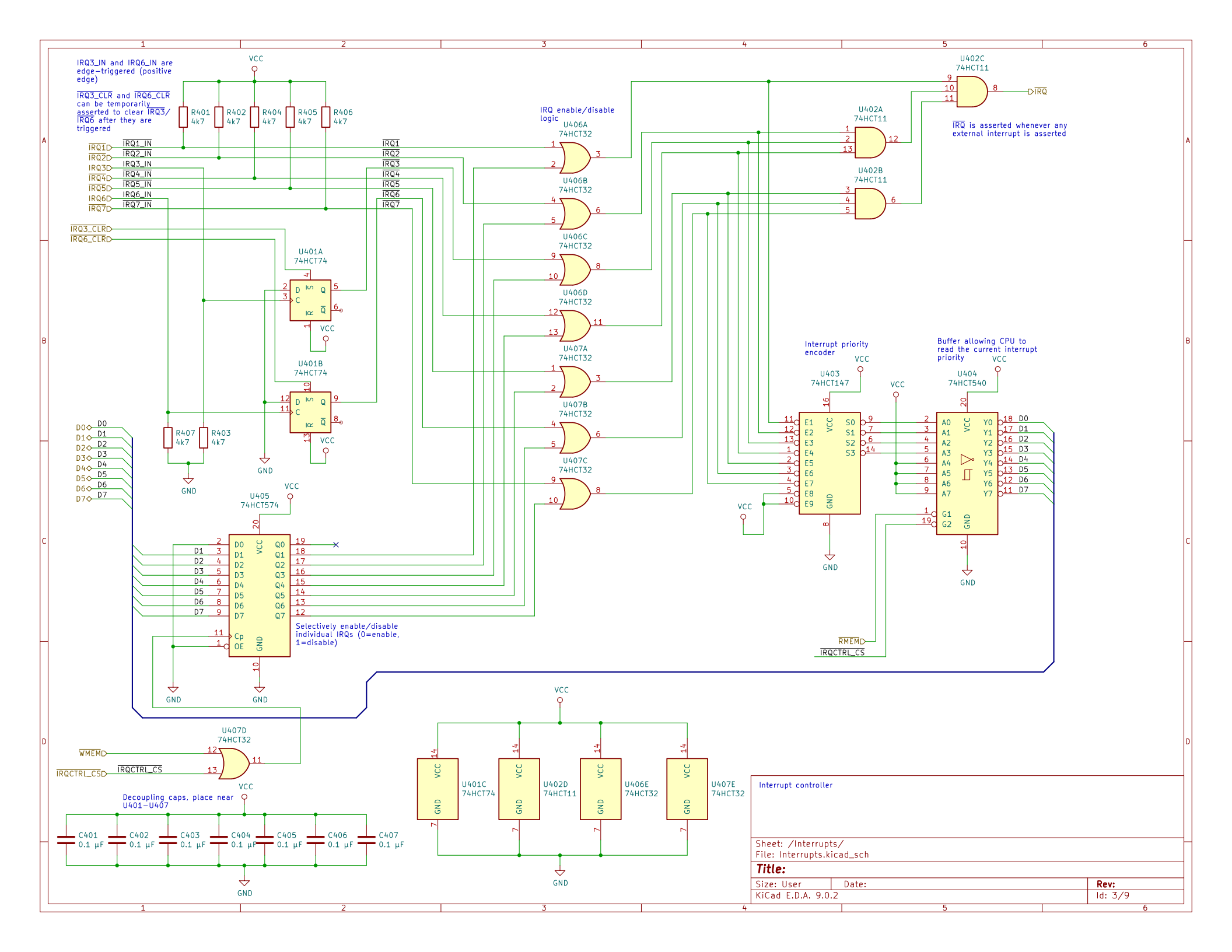
F68: A DIY 6809 microcomputer system

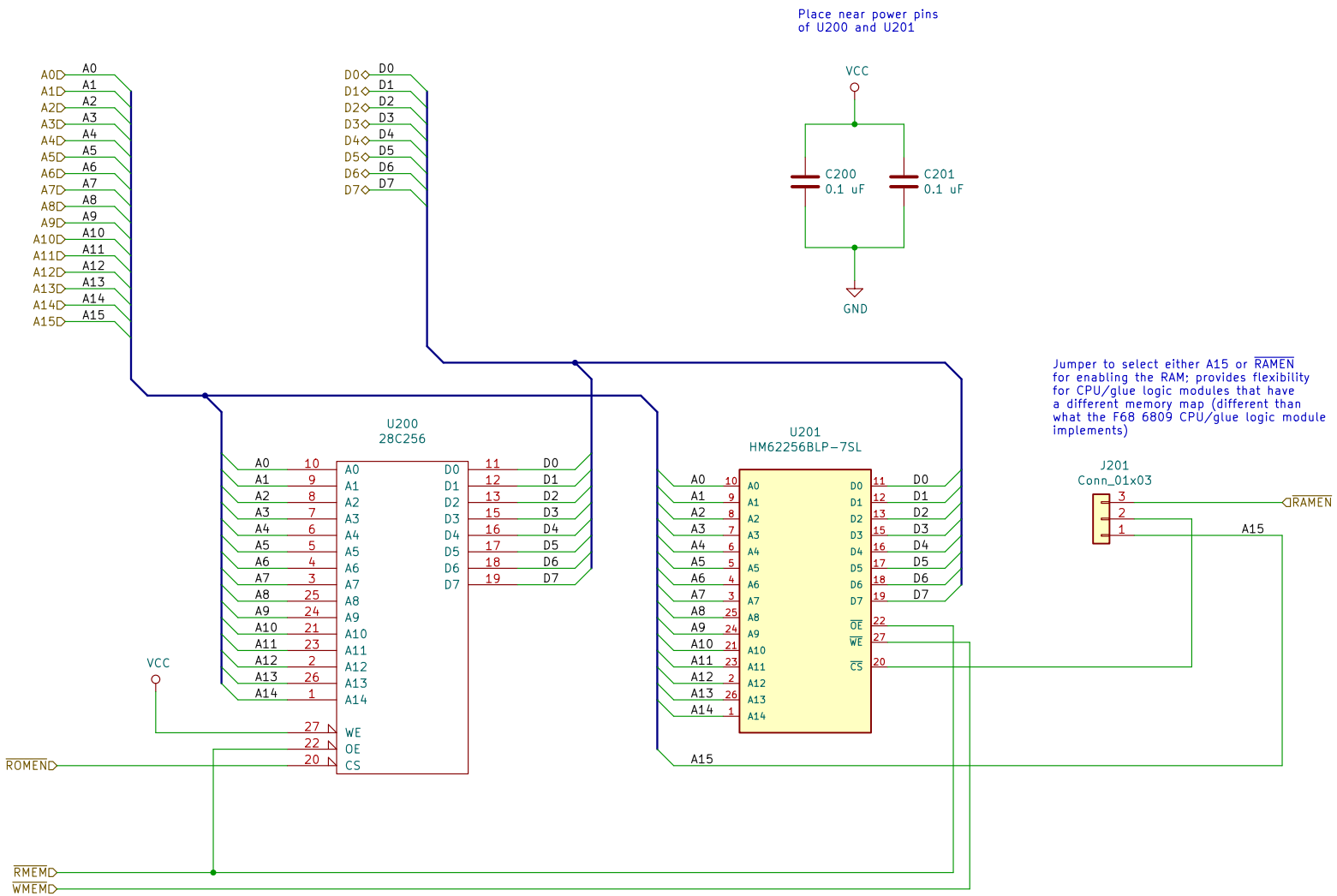
Sheet: /
File: F68.kicad_sch

Title:

Size: User	Date:	**Rev:**
KiCad E.D.A. 9.0.2		Id: 1/10


External reset
J100
Conn_01x02
S100
1-1825027-2
SHIELD
On-board reset
VCC
GND
C105
0.1 uF
U105
MAX708
VCC
GND
-RESET
RESET
-MR
PFI
-PFO
Unbuf_RST
LED
D100
R100
R
You can omit the LED and resistor. I add it as a power indicator, and also a reset indicator (the LED turns off when reset is asserted.) Using a high-efficiency LED and limiting the current to a few mA is a good idea.
R101
R102
R103
4k7
-NMI, -IRQ, and -FIRQ have pull-ups, but can be actively driven. -IRQ is generated by the interrupt controller module.
IRQ
U106
HD6809
CPU could also be MC6809 or HD6309.
Crystal frequency should be between 2 and 4 MHz. I used 3.6864 MHz.
Y100
Crystal
C113
22 pF
C114
22 pF
C106
0.1 uF
VSS
-NMI
-IRQ
-FIRQ
BS
BA
VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
D0
D1
D2
D3
D4
D5
D6
D7
-HALT
XTAL
EXTAL
-RES
MRDY
Q
E
-DMA/-BREQ
R/-W
Unbuf_A0
Unbuf_A1
Unbuf_A2
Unbuf_A3
Unbuf_A4
Unbuf_A5
Unbuf_A6
Unbuf_A7
Unbuf_A8
Unbuf_A9
Unbuf_A10
Unbuf_A11
Unbuf_A12
Unbuf_A13
Unbuf_A14
Unbuf_A15
Unbuf_D0
Unbuf_D1
Unbuf_D2
Unbuf_D3
Unbuf_D4
Unbuf_D5
Unbuf_D6
Unbuf_D7
U101
74HCT245
U102
74HCT245
U103
74HCT245
Buf_A0
Buf_A1
Buf_A2
Buf_A3
Buf_A4
Buf_A5
Buf_A6
Buf_A7
Buf_A8
Buf_A9
Buf_A10
Buf_A11
Buf_A12
Buf_A13
Buf_A14
Buf_A15
Buf_D0
Buf_D1
Buf_D2
Buf_D3
Buf_D4
Buf_D5
Buf_D6
Buf_D7
A->B
CE
Unbuf_R/W
Data bus transceiver
Address buffers
U104
74HCT365
Unbuf_E
Unbuf_RMEM
Unbuf_WMEM
Unbuf_RST
Unbuf_R/W
Buf_E
Buf_RMEM
Buf_WMEM
Buf_RST
Buf_R/W
E
RMEM
WMEM
RST
R/W
Control signal buffer
Place C101-C104 near the power pins of U101-U104
C101
C102
C103
C104
0.1 uF
RN101
4k7
Ensure that data bus signals are always at a valid logic level
U107B
74HCT00
U107A
74HCT00
U107D
74HCT00
RMEM goes low when the CPU is reading from memory
WMEM goes low when the CPU is writing to memory
Unbuf_RMEM
Unbuf_WMEM
Unused gate
U108C
74HCT27
U108B
74HCT27
U108A
74HCT27
U107C
74HCT00
ROMEN goes low when the CPU accesses the ROM at addresses $9000..$FFFF
ROMEN
U111
74HCT138
IOR0
IOR1
IOR2
IOR3
IOR4
IOR5
IOR6
IOR7
IOR0 through IOR7 are active low enables for 512 byte "regions" of the IO space:
IOR0: asserted for addresses $8000-$81FF
IOR1: asserted for addresses $8200-$83FF
IOR2: asserted for addresses $8400-$85FF
IOR3: asserted for addresses $8600-$87FF
IOR4: asserted for addresses $8800-$89FF
IOR5: asserted for addresses $8A00-$8BFF
IOR6: asserted for addresses $8C00-$8DFF
IOR7: asserted for addresses $8E00-$8FFF
U109
74HCT138
IODEV0 through IODEV15 decode the region $8000-$81FF into 16 "devices" of 32 bytes each.
IODEV0
IODEV1
IODEV2
IODEV3
IODEV4
IODEV5
IODEV6
IODEV7
U110
74HCT138
IODEV8
IODEV9
IODEV10
IODEV11
IODEV12
IODEV13
IODEV14
IODEV15
Place C109-C111 near the power pins of U109-U111
C107
C108
C109
C110
C111
0.1 uF
U107E
74HCT00
U108D
74HCT27
Reset, CPU, Glue Logic, Address/Data buffers, Control signal buffers
Sheet: /CPUandGlueLogic/
File: CPUandGlueLogic.kicad_sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. 9.0.2
Id: 2/9


IRQ3_IN and IRQ6_IN are edge-triggered (positive edge)
IRQ3_CLR and IRQ6_CLR can be temporarily asserted to clear IRQ3/IRQ6 after they are triggered
VCC
R401 4k7
R402 4k7
R404 4k7
R405 4k7
R406 4k7
IRQ1_IN
IRQ2_IN
IRQ3_IN
IRQ4_IN
IRQ5_IN
IRQ6_IN
IRQ7_IN
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ3_CLR
IRQ6_CLR
IRQ enable/disable logic
U406A 74HCT32
U406B 74HCT32
U406C 74HCT32
U406D 74HCT32
U407A 74HCT32
U407B 74HCT32
U407C 74HCT32
U401A 74HCT74
U401B 74HCT74
R407 4k7
R403 4k7
GND
U405 74HCT574
D0
D1
D2
D3
D4
D5
D6
D7
Selectively enable/disable individual IRQs (0=enable, 1=disable)
U402C 74HCT11
U402A 74HCT11
U402B 74HCT11
IRQ
IRQ is asserted whenever any external interrupt is asserted
Interrupt priority encoder
U403 74HCT147
Buffer allowing CPU to read the current interrupt priority
U404 74HCT540
RMEM
IRQCTRL_CS
U407D 74HCT32
WMEM
Decoupling caps, place near U401-U407
C401 0.1 µF
C402 0.1 µF
C403 0.1 µF
C404 0.1 µF
C405 0.1 µF
C406 0.1 µF
C407 0.1 µF
U401C 74HCT74
U402D 74HCT11
U406E 74HCT32
U407E 74HCT32
Interrupt controller
Sheet: /Interrupts/
File: Interrupts.kicad_sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. 9.0.2
Id: 3/9



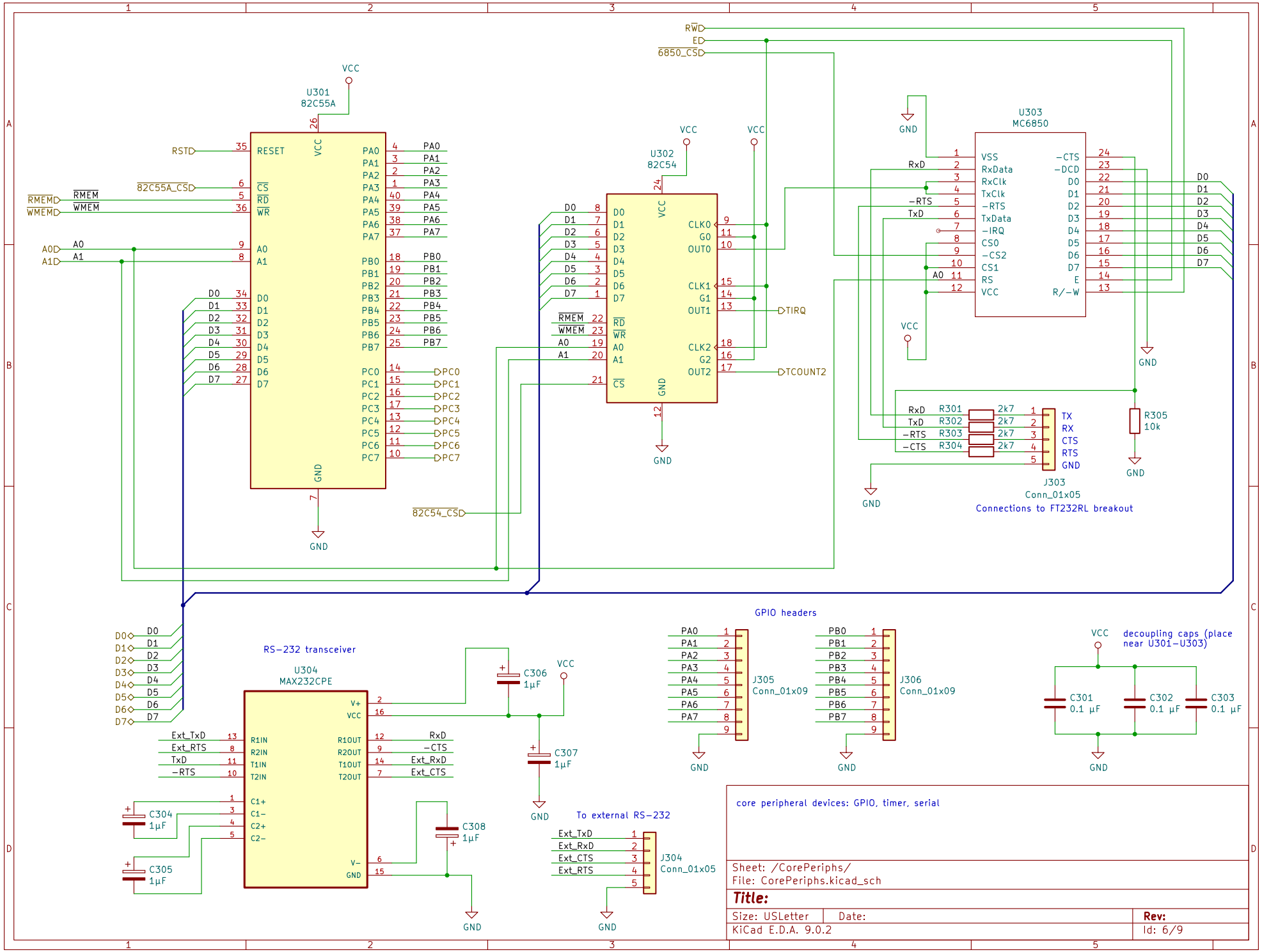
Memory devices

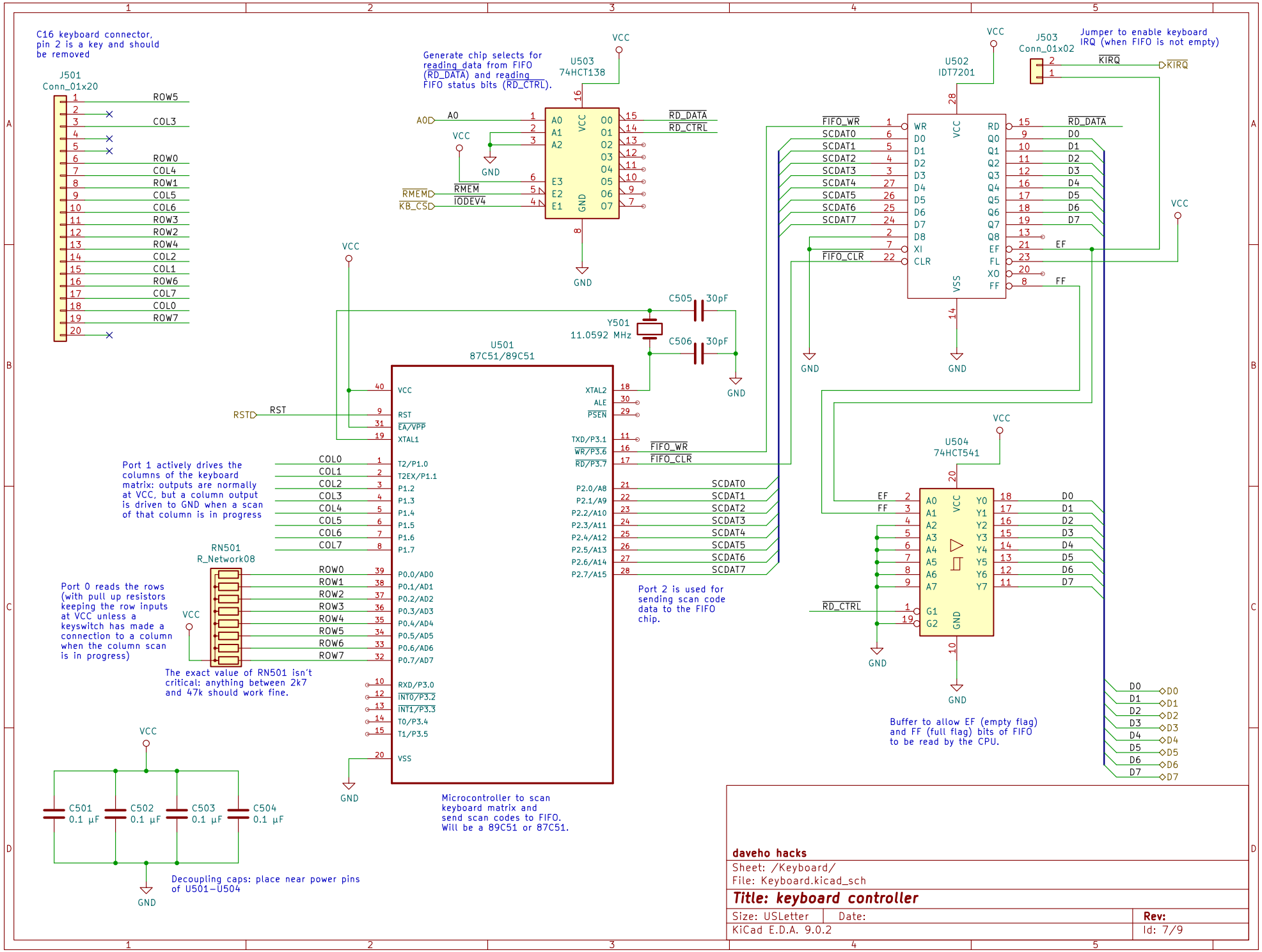
Sheet: /Memory/
File: Memory.kicad_sch

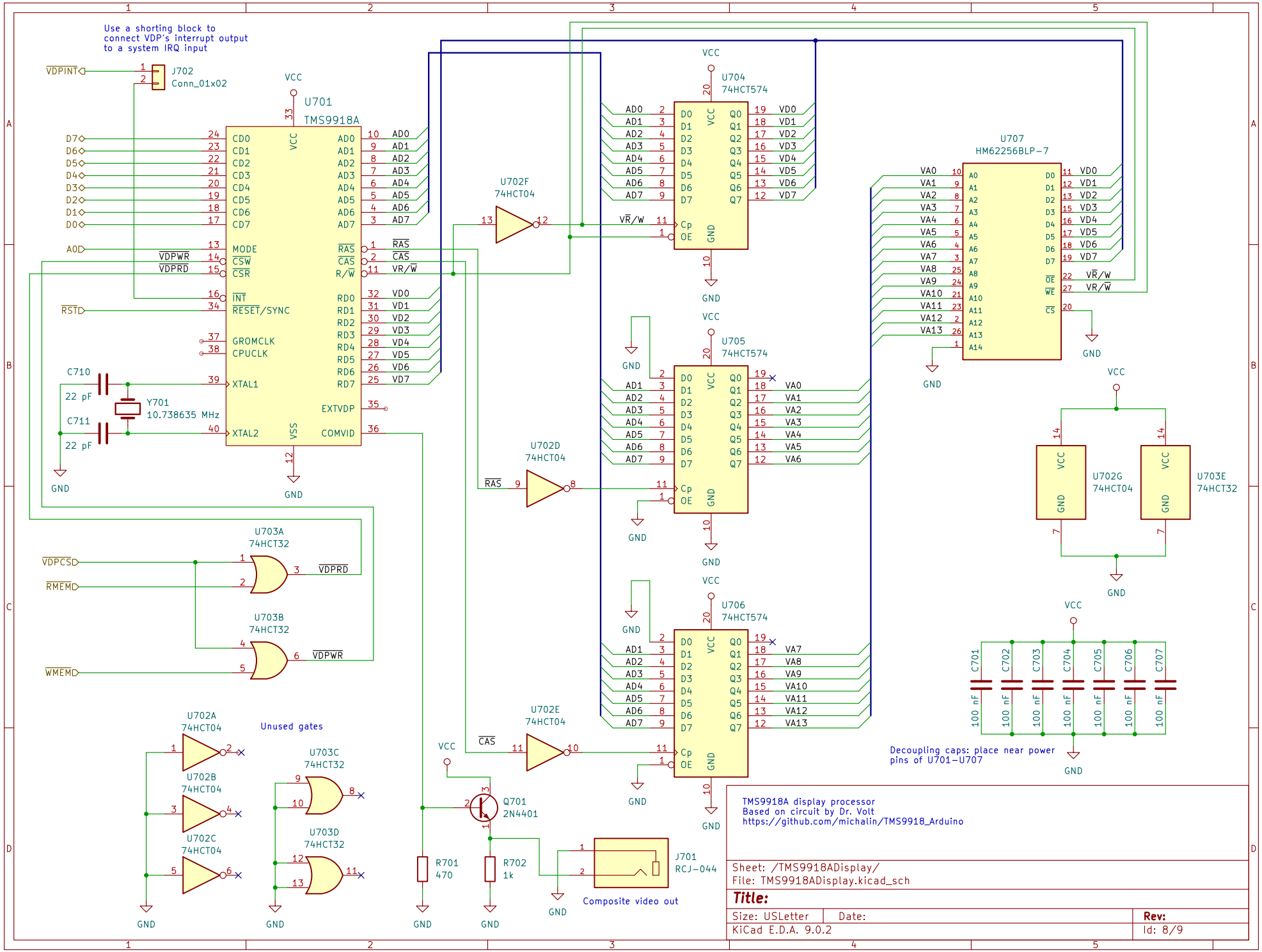
Title:

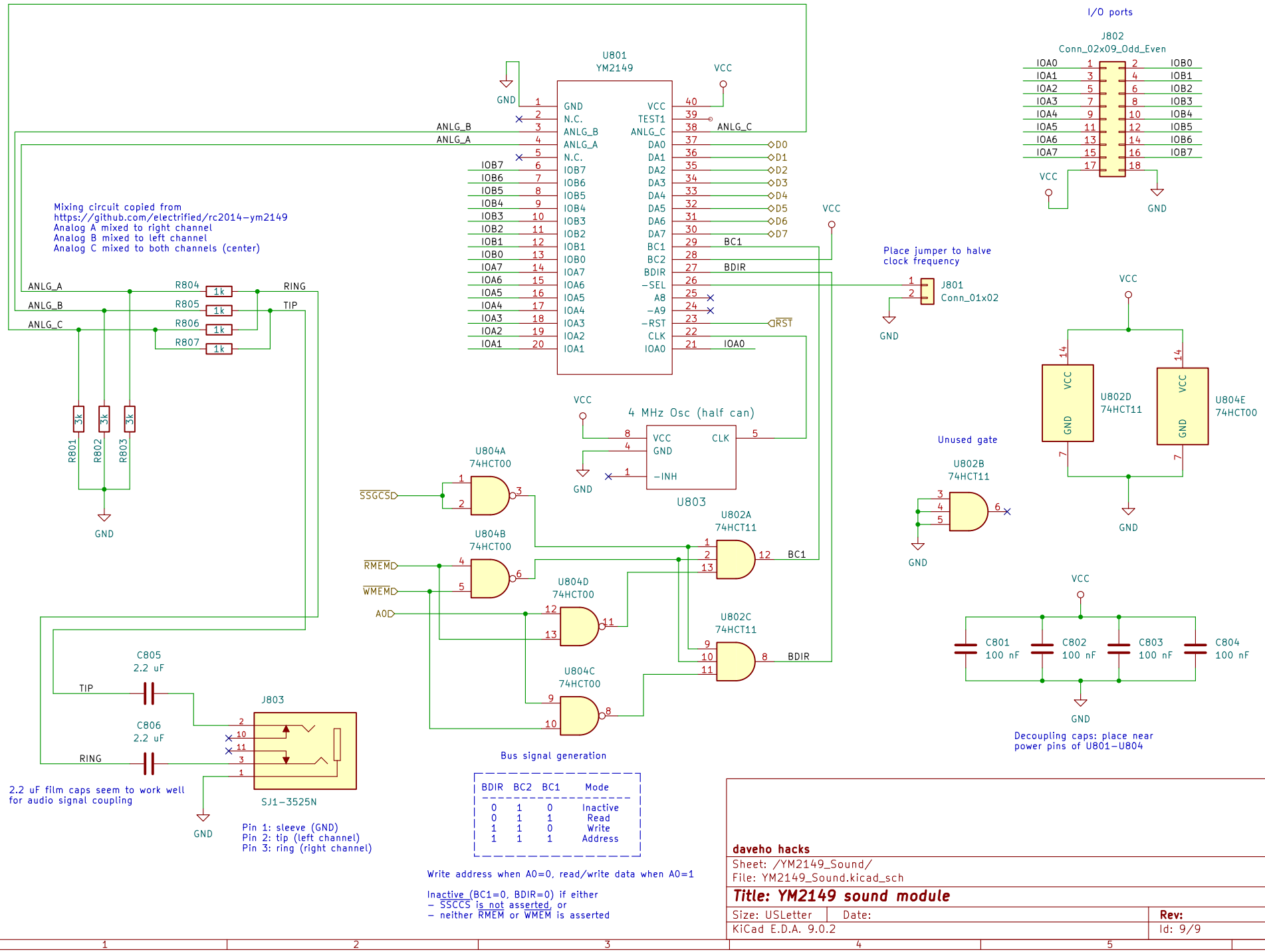
Size: USLetter | Date: | **Rev:**

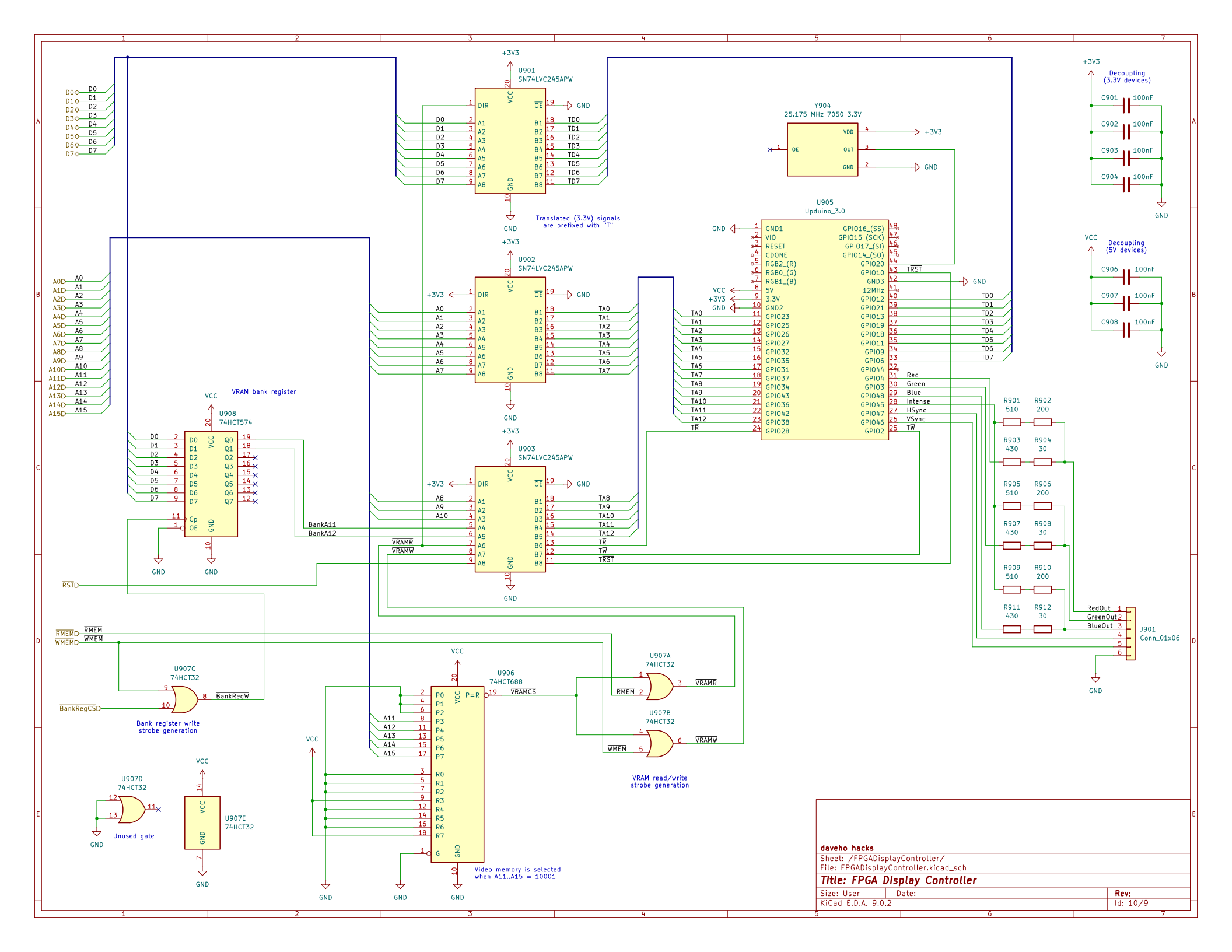
KiCad E.D.A. 9.0.2 | Id: 5/9


U301
82C55A
RST
82C55A_CS
RMEM
WMEM
A0
A1
RESET
CS
RD
WR
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
D0
D1
D2
D3
D4
D5
D6
D7
VCC
GND
U302
82C54
CLK0
G0
OUT0
CLK1
G1
OUT1
CLK2
G2
OUT2
TIRQ
TCOUNT2
82C54_CS
RW
E
6850_CS
U303
MC6850
VSS
RxData
RxClk
TxClk
−RTS
TxData
−IRQ
CS0
−CS2
CS1
RS
R/−W
−CTS
−DCD
RxD
TxD
R301
R302
R303
R304
2k7
R305
10k
TX
RX
CTS
RTS
J303
Conn_01x05
Connections to FT232RL breakout
RS−232 transceiver
U304
MAX232CPE
R1IN
R2IN
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
V+
V−
C1+
C1−
C2+
C2−
Ext_TxD
Ext_RTS
TxD
−RTS
RxD
−CTS
Ext_RxD
Ext_CTS
C304
C305
C306
C307
C308
1µF
To external RS−232
J304
Conn_01x05
GPIO headers
J305
Conn_01x09
J306
Conn_01x09
decoupling caps (place near U301−U303)
C301
C302
C303
0.1 µF
core peripheral devices: GPIO, timer, serial
Sheet: /CorePeriphs/
File: CorePeriphs.kicad_sch
Title:
Size: USLetter
Date:
Rev:
KiCad E.D.A. 9.0.2
Id: 6/9


C16 keyboard connector, pin 2 is a key and should be removed
J501
Conn_01x20
ROW5
COL3
ROW0
COL4
ROW1
COL5
COL6
ROW3
ROW2
ROW4
COL2
COL1
ROW6
COL7
COL0
ROW7
Generate chip selects for reading data from FIFO (RD_DATA) and reading FIFO status bits (RD_CTRL).
U503
74HCT138
A0
RMEM
IODEV4
KB_CS
RD_DATA
RD_CTRL
VCC
GND
U502
IDT7201
FIFO_WR
SCDAT0
SCDAT1
SCDAT2
SCDAT3
SCDAT4
SCDAT5
SCDAT6
SCDAT7
FIFO_CLR
EF
FF
J503
Conn_01x02
KIRQ
Jumper to enable keyboard IRQ (when FIFO is not empty)
C505 30pF
C506 30pF
Y501
11.0592 MHz
U501
87C51/89C51
RST
XTAL1
XTAL2
ALE
PSEN
WR/P3.6
RD/P3.7
Port 1 actively drives the columns of the keyboard matrix: outputs are normally at VCC, but a column output is driven to GND when a scan of that column is in progress
COL0
COL1
COL2
COL3
COL4
COL5
COL6
COL7
RN501
R_Network08
Port 0 reads the rows (with pull up resistors keeping the row inputs at VCC unless a keyswitch has made a connection to a column when the column scan is in progress)
ROW0
ROW1
ROW2
ROW3
ROW4
ROW5
ROW6
ROW7
The exact value of RN501 isn't critical: anything between 2k7 and 47k should work fine.
Port 2 is used for sending scan code data to the FIFO chip.
U504
74HCT541
Buffer to allow EF (empty flag) and FF (full flag) bits of FIFO to be read by the CPU.
D0
D1
D2
D3
D4
D5
D6
D7
C501 0.1 µF
C502 0.1 µF
C503 0.1 µF
C504 0.1 µF
Decoupling caps: place near power pins of U501–U504
Microcontroller to scan keyboard matrix and send scan codes to FIFO. Will be a 89C51 or 87C51.
daveho hacks
Sheet: /Keyboard/
File: Keyboard.kicad_sch
Title: keyboard controller
Size: USLetter
Date:
Rev:
KiCad E.D.A. 9.0.2
Id: 7/9


Use a shorting block to connect VDP's interrupt output to a system IRQ input
VDPINT
J702
Conn_01x02
U701
TMS9918A
VCC
GND
D7
D6
D5
D4
D3
D2
D1
D0
A0
VDPWR
VDPRD
RST
C710
22 pF
Y701
10.738635 MHz
C711
22 pF
U704
74HCT574
U705
74HCT574
U706
74HCT574
U707
HM62256BLP-7
U702F
74HCT04
U702D
74HCT04
U702E
74HCT04
U702A
74HCT04
U702B
74HCT04
U702C
74HCT04
U702G
74HCT04
U703A
74HCT32
U703B
74HCT32
U703C
74HCT32
U703D
74HCT32
U703E
74HCT32
VDPCS
RMEM
WMEM
RAS
CAS
VR/W
Unused gates
Q701
2N4401
R701
470
R702
1k
J701
RCJ-044
Composite video out
C701
C702
C703
C704
C705
C706
C707
100 nF
Decoupling caps: place near power pins of U701–U707
TMS9918A display processor
Based on circuit by Dr. Volt
https://github.com/michalin/TMS9918_Arduino
Sheet: /TMS9918ADisplay/
File: TMS9918ADisplay.kicad_sch
Title:
Size: USLetter
Date:
Rev:
KiCad E.D.A. 9.0.2
Id: 8/9


I/O ports
J802
Conn_02x09_Odd_Even
IOA0 IOA1 IOA2 IOA3 IOA4 IOA5 IOA6 IOA7
IOB0 IOB1 IOB2 IOB3 IOB4 IOB5 IOB6 IOB7
VCC
GND
U801
YM2149
GND N.C. ANLG_B ANLG_A N.C. IOB7 IOB6 IOB5 IOB4 IOB3 IOB2 IOB1 IOB0 IOA7 IOA6 IOA5 IOA4 IOA3 IOA2 IOA1
VCC TEST1 ANLG_C DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7 BC1 BC2 BDIR −SEL A8 −A9 −RST CLK IOA0
D0 D1 D2 D3 D4 D5 D6 D7
Mixing circuit copied from
https://github.com/electrified/rc2014-ym2149
Analog A mixed to right channel
Analog B mixed to left channel
Analog C mixed to both channels (center)
ANLG_A
ANLG_B
ANLG_C
R804 R805 R806 R807
1k
RING
TIP
R801 R802 R803
3k
Place jumper to halve
clock frequency
J801
Conn_01x02
4 MHz Osc (half can)
VCC
GND
CLK
−INH
U803
U804A
74HCT00
SSGCS
U804B
RMEM
WMEM
A0
U804D
U804C
U802A
U802C
BC1
BDIR
RST
IOA0
Unused gate
U802B
U802D
74HCT11
U804E
C805
2.2 uF
C806
TIP
RING
J803
SJ1-3525N
2.2 uF film caps seem to work well
for audio signal coupling
Pin 1: sleeve (GND)
Pin 2: tip (left channel)
Pin 3: ring (right channel)
C801 C802 C803 C804
100 nF
Decoupling caps: place near
power pins of U801-U804
Bus signal generation
BDIR BC2 BC1 Mode
0 1 0 Inactive
0 1 1 Read
1 1 0 Write
1 1 1 Address
Write address when A0=0, read/write data when A0=1
Inactive (BC1=0, BDIR=0) if either
− SSCCS is not asserted, or
− neither RMEM or WMEM is asserted
daveho hacks
Sheet: /YM2149_Sound/
File: YM2149_Sound.kicad_sch
Title: YM2149 sound module
Size: USLetter
Date:
Rev:
KiCad E.D.A. 9.0.2
Id: 9/9



daveho hacks

Sheet: /FPGADisplayController/

File: FPGADisplayController.kicad_sch

Title: FPGA Display Controller

Size: User	Date:	Rev:
KiCad E.D.A. 9.0.2		Id: 10/9