D Y PATIL
RAMRAO ADIK INSTITUTE OF TECHNOLOGY
NAVI MUMBAI

Department of Computer Engineering

Academic Year: 2019-20(EVEN)

ASSIGNMENT NO:1

Subject: Computer Organization & Architecture	**Semester:** IV

Ques. No.	Bit	Question	Max. Marks	CO	BT
Q. 1		Convert the following number 256.325 into IEEE single and double precision.	8M	CO1	BT3
Q. 2	a)	Discuss difference between RISC and CISC processors.	7M	CO2	BT2
Q. 2	b)	A non-pipelined processor X has a clock rate of 25MHz and an average CPI (cycles per instruction) of 4. Processor Y, an improved successor of X, is designed with a five-stage linear instruction pipeline. However, due to latch delay and clock skew effects, the clock rate of Y is only 20MHz. (a) It is a program containing 100 instructions is executed on both processors, what is the speedup of processor Y compared with that of processor X? (b) Calculate the MIPS rate of each processor.	7M	CO2	BT5
Q. 3		Write a microprogram for: ADD [R1], [R2]	8M	CO3	BT3

==========

Course Outcomes (CO) Students' will be able to:

CO1: To describe basic structure of the computer system and demonstrate the arithmetic algorithms for solving ALU operations.
CO 2: To describe instruction level parallelism and infer hazards in typical processor pipelines.
CO 3: To determine control unit design methods / operations.
CO 4: To demonstrate the memory mapping techniques.
CO 5: To identify various types of buses, interrupts and I/O operations in a computer system.
CO 6: To summarize superscalar architectures, multi-core architecture and their advantages.

Bloom's Taxonomy

BT1- Remember, BT2- Understand, BT3- Apply, BT4- Analyze, BT5- Evaluate, BT6- Create

Subject In charge

DQA Member