Testing Upgrades to icestorm, yosys, zipcpu and nextpnr zipcpu, autofpga & verilator icozip catzip-dev branch **mypi3-20** 10/12/21

Build steps:

git clone git@github.com:develone/icozip.git -b catzip-dev catzip-dev

cd catzip-dev/

devel@mypi3-20:~/testbuilds/catzip-dev \$ mousepad rtl/catzip/cpu/zipcpu.v line 737

Note: These next 4 steps might be needed to be repeated one or more times. This creates a catzip.bin. If the runipeg does not end in ./arm-netpport window with the following.

- . w=256 h=256
- . 1401000 2
- . flag 2 0x204fe08
- . 1401004 1
- . 140100c 200fe08

cd ~/testbuilds/catzip/rtl/catzip/

rm -f catzip.asc catzip.json catzip.bin

make bin

. ./myenv-a.sh

Testing upgrade to zipcpu that fixes LOCK instruction generation in GCC

rtl/catzip/cpu/zipcpu.v line 737

.OPT_LOCK(OPT_LOCK),

FPGA Tools:

autofpga

commit 5b57538081d60a04cd32aeba2436816062cb0141 (HEAD -> master, upstream/master,

upstream/dev)

Author: ZipCPU <dgisselq@ieee.org> Date: Fri Aug 14 07:55:55 2020 -0400 Fixes MacOS build err--std::string vs char * in gbl_msg.err()

zipcpu

devel@mypi3-20:~/zipcpu \$ git log

commit 548a0efbe5729279f2ae9779a2af4229e8241e52 (HEAD -> master, upstream/master,

upstream/dev)

Author: ZipCPU <dgisselq@ieee.org> Date: Wed Oct 6 11:54:56 2021 -0400

Fixed LOCK instruction generation in GCC

devel@mypi3-20:~/autofpga \$ yosys -V

Yosys 0.9+4081 (git sha1 83a21814, gcc 8.3.0-6+rpi1 -fPIC -Os)

devel@mypi3-20:~/autofpga \$ nextpnr-ice40 -V

nextpnr-ice40 -- Next Generation Place and Route (Version 67bd349e)

Verilator 4.100 2020-09-07 rev v4.100-10-g39eea781

Simulation:

devel@mypi3-20:~/testbuilds/catzip-dev/sim/verilated \$ clear; ./arm-main_tb

Listening on port 8363

Listening on port 8364

> T

Running CPU self-test

CIS Instructions Supported

Break test #1 **Pass** Break test #2 **Pass** Break test #3 Pass Early Branch test Pass Trap test/AND **Pass** Trap test/CLR Pass Overflow test **Pass** Carry test **Pass** Loop test Pass Shift test Pass Pipeline test **Pass** Mem-Pipeline test **Pass** Conditional Execution test **Pass** No-waiting pipeline test Pass Conditional Branching test Pass Ill Instruction test, NULL PC Pass Ill Instruction test, two Pass Comparison test, == **Pass** Comparison test, != **Pass**

CC Register test Pass
Multi-Arg test Pass
Multiply test Pass

devel@mypi3-20:~/testbuilds/catzip-dev/sim/verilated \$ clear; ./arm-main_tb

Listening on port 8363

Listening on port 8364

> T

Accepted CMD connection

< A0400001Wf

> A0400001K00000000

< [CLOSED]

Hello, World

devel@mypi3-20:~/testbuilds/catzip-dev/sw/host \$./arm-zipload -v ../board/cputest

Halting the CPU Memory regions:

Block RAM: 01400000 - 01402000 SDRAM : 02000000 - 03000000

Loading: ../board/cputest

Section 0: 02000000 - 020039f0

Writing to MEM: 02000000-020039f0

Clearing the CPUs registers Setting PC to 02000000

The CPU should be fully loaded, you may now

start it (from reset/reboot) with:

> wbregs cpu 0x0f

CPU Status is: 0000060f

devel@mypi3-20:~/testbuilds/catzip-dev/sw/host \$./arm-wbregs cpu 0x0f

04000000 (CPU)-> 0000000f

devel@mypi3-20:~/testbuilds/catzip-dev/sw/host \$./arm-zipload -v ../board/hello

Halting the CPU Memory regions:

Block RAM: 01400000 - 01402000 SDRAM : 02000000 - 03000000

Loading: ../board/hello

Section 0: 02000000 - 020047c8 Writing to MEM: 02000000-020047c8

Clearing the CPUs registers Setting PC to 02000000

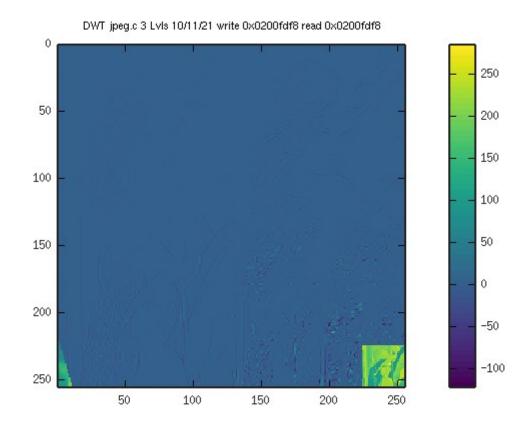
The CPU should be fully loaded, you may now

start it (from reset/reboot) with:

> wbregs cpu 0x0f

CPU Status is: 0000060f

devel@mypi3-20:~/testbuilds/catzip-dev/sw/host \$./arm-wbregs cpu 0x0f jpeg simulation



y2= 318,416

Testing Verilog bins:

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/rtl/uart \$ sudo config_cat helloworld.bin devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/rtl/uart \$ sudo config_cat rtl/basic/dimmer.bin devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/rtl/uart \$ sudo config_cat rtl/basic/blinky.bin devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/rtl/uart \$ sudo config_cat rtl/basic/blinky.bin devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/rtl/uart \$ sudo config_cat rtl/switch_leds/switch_leds.bin

 $devel@mypi3-19: \sim / testbuilds/mypi3-20/catzip-dev/rtl/uart \$ sudo config_cat rtl/leddigits/leddigits.bin$

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$ sudo ./arm-netpport Listening on port 8363 Listening on port 8364

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/rtl/pptest \$ sudo config_cat hellopp.bin

```
File Edit Tabs Help

Listening on port 8363

Listening on port 8364

ello, World!

Hello, World!
```

 $devel@mypi3-19:{\sim}/testbuilds/mypi3-20/catzip-dev/rtl/pptest\ \$\ sudo\ config_cat\ speechpp.bin$

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$ sudo config_cat ../../rtl/catzip/catzip.bin

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$ clear; sudo ./arm-netpport

Listening on port 8363 Listening on port 8364

File Edit Tabs Help

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$./arm-wbregs version

Listening on port 8363 Listening on port 8364 Hello, World! Hello, World! Four score and seven years ago our fathers brought forth on this continent, a new nation, conceived in Liberty, and dedicated to the proposition that all men are created equal. Now we are engaged in a great civil war, testing whether that nation, or any nation so conceived and so dedicated, can long endure. We are met on a great battle-field of that war. We have come to dedicate a portion of that field, as a final resting place for those who here gave their lives that that nation might live. It is altogether fitting and proper that we should do this. But, in a larger sense, we can not dedicate-we can not consecratewe can not hallow-this ground. The brave men, living and dead, who struggled here, have consecrated it, far above our poor power to add or detract. The world will little note, nor long remember what we say here, but it can never forget what they did here. It

is for us the living, rather, to be dedicated here to the unfinished work which they who fought here have thus far so nobly advanced. It is rather for us to be here dedicated to the great task remaining before us-that from these honored dead we take increased devotion to that cause for which they gave the last full measure of devotion-that we here highly resolve that these dead shall not have died in vain-that this nation, under God,

01000014 (VERSION) : [.!..] 20211012

Testing sdram Write & Read:

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host $\$./arm-wrsdram r.bin The size of the buffer is 0x010000 or 65536 words

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$./arm-rdsdram sdram.bin

Write-COMPLETE

Command port is now connected

The size of the buffer is 0x010000 or 65536 words devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$ diff r.bin sdram.bin

```
< A0400001Wf
> A04000001K00000000
Command port disconnect
. w=2-5 h=2-5
. 1401000 2
. flag 2 0x204fdf8
. 1401004 1
. 140100c 200fdf8
. ptrs.alt 0x2054498 0x200fdf8
.1:p/?1
. 0x200fdf8 0xe2
. 0x200fdfc 0xe2
. 0x200fe00 0xe1
. 0x200fe04 0xe1
. 0x202fdf8 0xcf
. 0x202fdfc 0xcf
. 0x202fe00 0xcf
. 0x202fe04 0xcf
. 0x204fde8 0x96
. 0x204fdec 0xa1
. 0x204fdf0 0xab
. 0x204fdf4 0xb4
. 2-5 0x200fdf8 0x2054498 0x 1401004
. 2-5
```

The runjpeg,sh sets several values in blkram used to wait on user.

Block RAM: 01400000 - 01402000 SDRAM : 02000000 - 03000000

Loading: ../board/jpeg

Section 0: 02000000 - 0204fe7c Writing to MEM: 02000000-0204fe7c

Clearing the CPUs registers
Setting PC to 02000000
The CPU should be fully loaded, you may now start it (from reset/reboot) with:
> wbregs cpu 0x0f

CPU Status is: 0000060f

04000000 (CPU)-> 0000000f

This step writes the file r.bin to the sdram. The values can be g.bin or b.bin.

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$./arm-wrsdram r.bin The size of the buffer is 0x010000 or 65536 words

READ-COMPLETE

This steps lets the user where the input and output will be written and read.

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$./arm-wbregs 0x0140100c 0140100c (): [....] 0200fdf8

This step clears the wait loop.

This step clears the wait1 loop.

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$./arm-wbregs 0x01401010 0x0 01401010 ()-> 00000000

This step reads the sdram and stores the data in dwt.bin used by octave to show the lifting step results.

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$ rm -f dwt.bin; ./arm-rdsdram dwt.bin

Write-COMPLETE

The size of the buffer is 0x010000 or 65536 words

devel@mypi3-19:~/testbuilds/mypi3-20/catzip-dev/sw/host \$ octave

libEGL warning: DRI3: failed to query the version libEGL warning: DRI2: failed to authenticate

GNU Octave, version 4.4.1

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FITNESS FOR A PARTICULAR PURPOSE. For details, type 'warranty'.

Octave was configured for "arm-unknown-linux-gnueabihf".

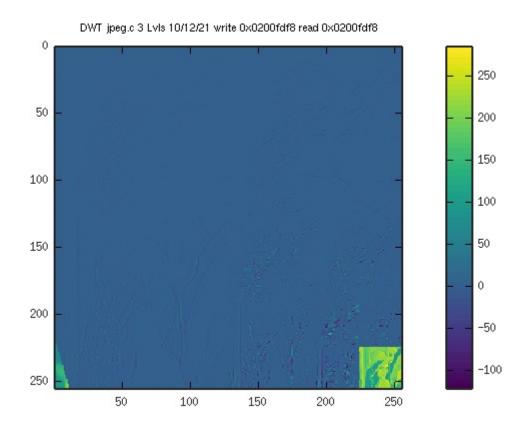
Additional information about Octave is available at https://www.octave.org.

Please contribute if you find this software useful. For more information, visit https://www.octave.org/get-involved.html

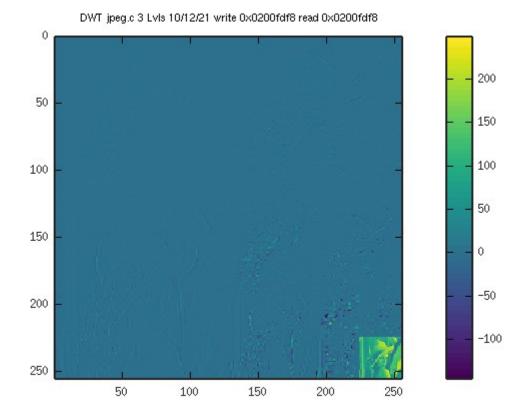
Read https://www.octave.org/bugs.html to learn how to submit bug reports. For information about changes from previous versions, type 'news'.

octave:1>rgb

dwt-r

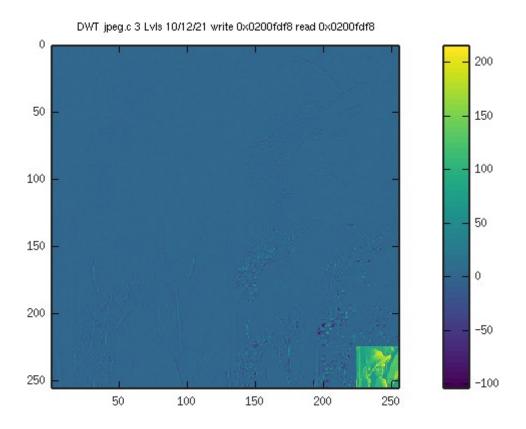


y2= 13,1087 dwt-g



y2=-199,205

dwt-b



y2=-146.934