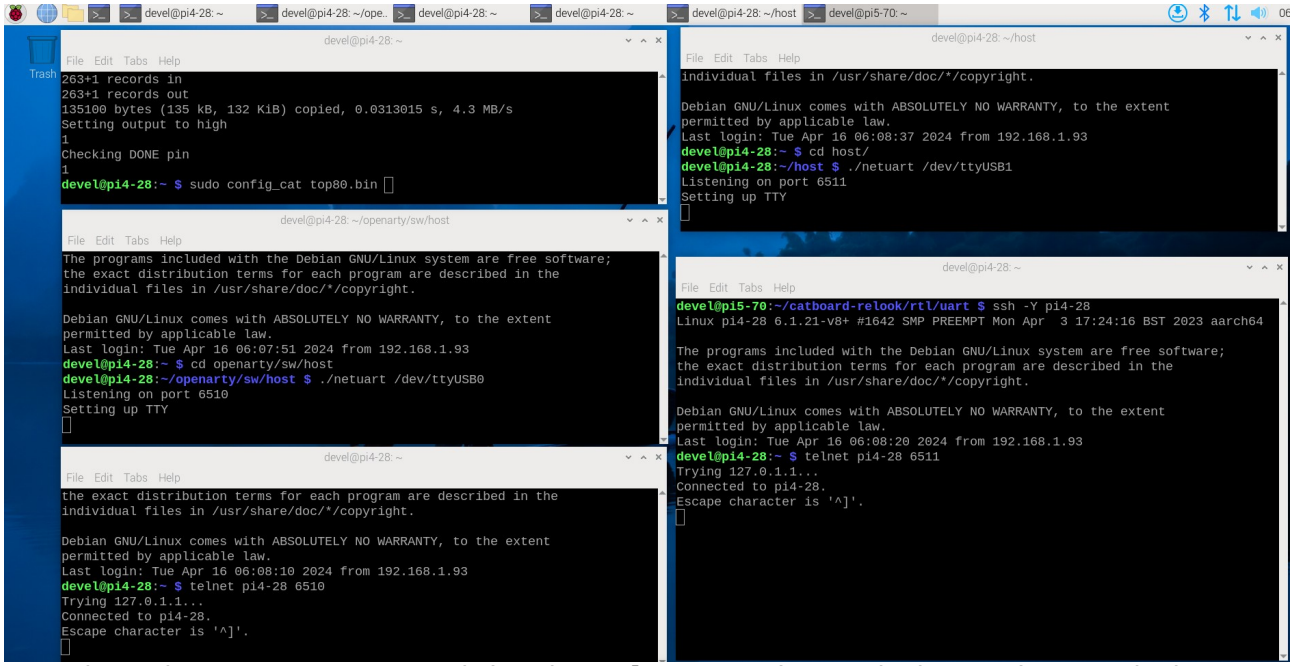
**********Draft**********

Catboard Lattice ice40HX8K FPGA program with Yosys Tools and Raspberry Pi 3B
FPGA is programmed to receive and transmit on two UARTS at a BAUD_RATE of 4000000
04/16/24

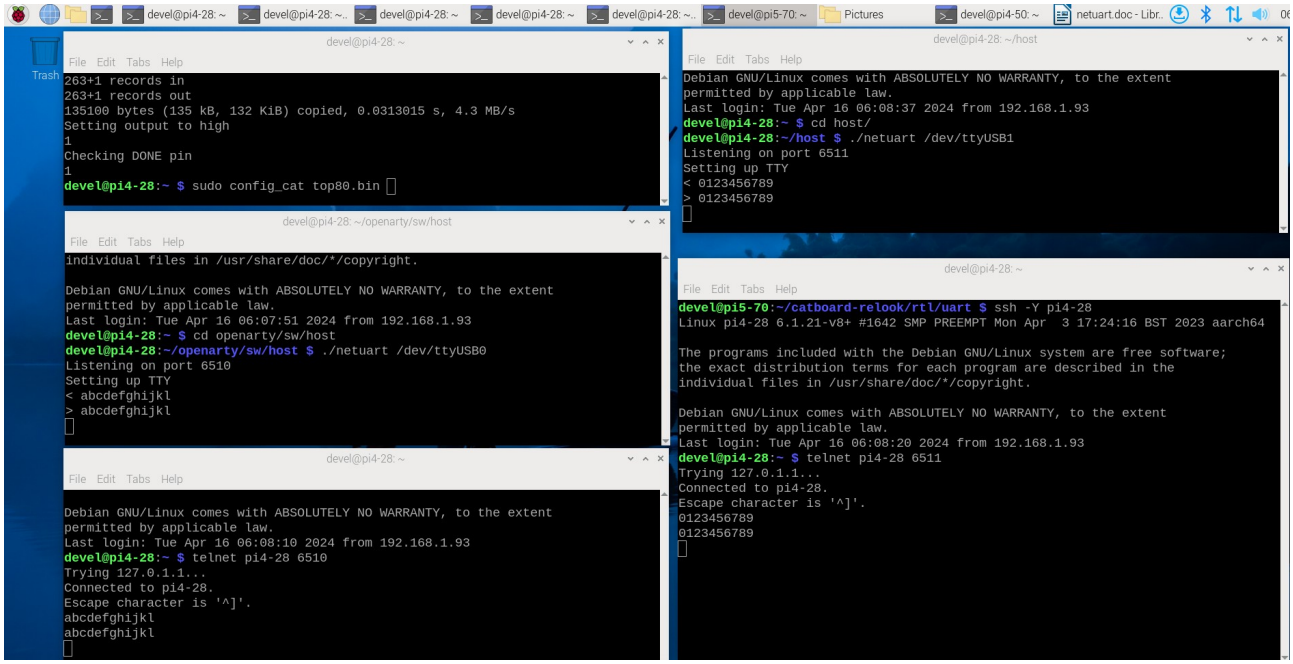
**********Draft**********

The FPGA is programmed in the upper left shell.

```
devel@pi4-28:~ $ sudo config_cat top80.bin

OK: GPIO 25 exported
OK: GPIO 17 exported
OK: GPIO 22 exported

OK: SPI driver loaded

Setting GPIO directions
out
out
in
Setting output to low
0
Reseting FPGA
0
1
Checking DONE pin
0
Continuing with configuration procedure
263+1 records in
263+1 records out
135100 bytes (135 kB, 132 KiB) copied, 0.0284037 s, 4.8 MB/s
Setting output to high
1
Checking DONE pin
1
```



Now when characters are typed in the telnet session and the CR is typed the netuart session receives the data.



The code that provides the source code for netuart is found /openarty /sw/host/netuart.cpp in the repo below. Two versions were compiled the defualt at port 6510 and a 2nd at port 6511. The host folder was extracted from the repo and the defualt port was changed to 6511.

```
devel@pi4-30:~ $ diff openarty/sw/host/port.h host/port.h
50c50
< #define   FPGAPORT    6510
---
> #define   FPGAPORT    6511
```

The 2 versions are compiled with make command.
https://github.com/develone/openarty.git

https://github.com/develone/catboard-relook/blob/master/doc/tools/yosys-tools.txt

This was the initial code used to generate top.bin.
https://github.com/develone/vhd2icestorm/blob/dev/doc/testing-top.txt

This is code that generates top80.bin found rtl/2uarts. The command ./build.sh creates top.bin. It is then copied to the system that has the catboard as top80.bin since now a pll is used to reduce the 100MHz input clk to 80MHz.
https://github.com/develone/102121icozip.git

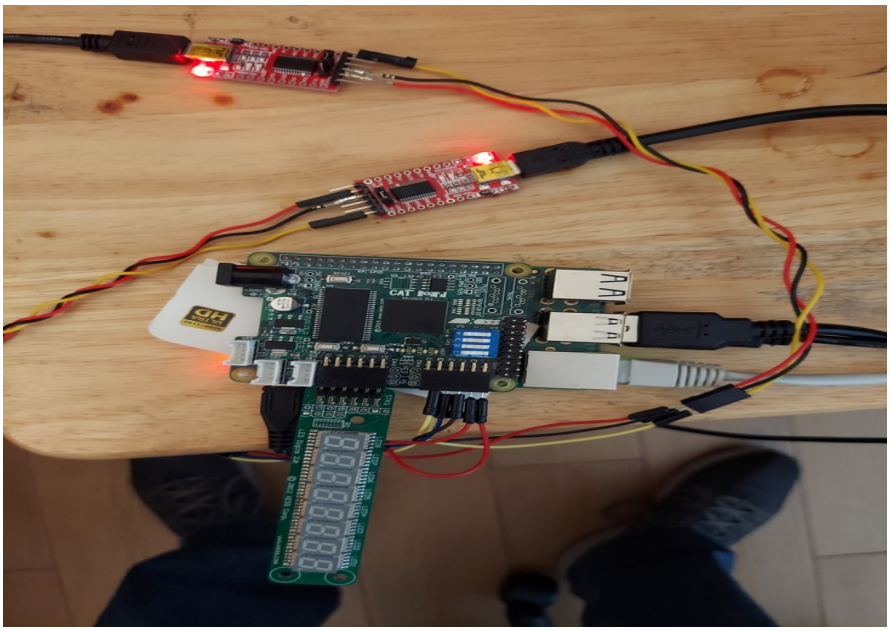
https://github.com/develone/vhd2icestorm/blob/dev/doc/testing-top-031524.txt

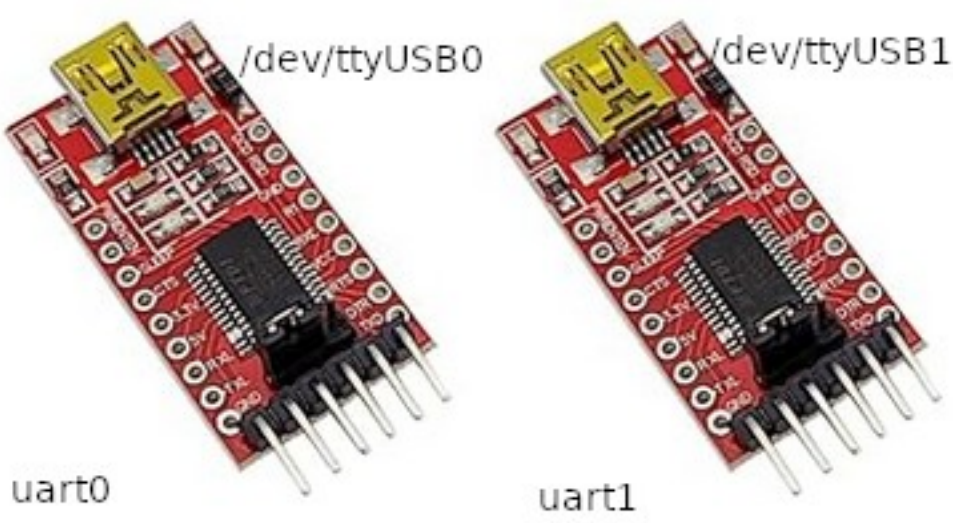
https://github.com/develone/tangnano9k-series-examples/blob/dev/catboard/doc/uart_vcd.png

https://zipcpu.com/blog/2017/05/26/simpledbg.html

ZipCPU provided the following:
[A -: B] means to grab B bits ending at A. So the most significant bit grabbed will be bit A, then A-1, then A-2, all the way down to A-(B-1)

```
.rx_data(sig_rx_data[7 + 8 * i -: 7 + 1]),
.tx_data(sig_tx_data[7 + 8 * i -: 7 + 1]))
if i=0 7 + 8 * 0 - : 8
if i=0 7  - : 8
if i=1 7 + 8 * 1 - : 8
if i=1 15 - : 8
if i=0 .rx_data(sig_rx_data[7  -: 8]),  7 6 5 4 3 2 1 0
if i=0 .tx_data(sig_tx_data[7  -: 8]))
if i=1 .rx_data(sig_rx_data[15  -: 8]),
if i=1 .tx_data(sig_tx_data[15  -: 8])) 15 14 13 12 11 10 9 8
```





rx[0] B5 PM2-A3 tx BLACK FTDI-USB

tx[0] B3 PM2-A2 rx RED FTDI-USB

grd   PM2-A5 grd YELLOW FTDI-USB

```
rx[1] B6 PM2-A4 tx BLACK FTDI-USB

tx[1] A1 PM2-A1 rx RED FTDI-USB

grd     PM2-B5  grd YELLOW FTDI-USB

Changes needed to top.v
devel@pi4-30:~/102121icozip/rtl/2uarts $ git diff top.v
diff --git a/rtl/2uarts/top.v b/rtl/2uarts/top.v
index 0ec7580..276257f 100644
--- a/rtl/2uarts/top.v
+++ b/rtl/2uarts/top.v
@@ -19,10 +19,10 @@ parameter BIT_WIDTH = 11;
 parameter BAUD_RATE = 4000000;
 parameter CLOCK_FREQ_HZ = 80000000;
 reg [23:0] sig_counter;
-wire [uarts - 1:0] sig_send;
-wire [uarts - 1:0] sig_valid;
-wire [8 * (uarts - 1) + 7:0] sig_rx_data;
-wire [8 * (uarts - 1) + 7:0] sig_tx_data;  //signal sig_rx_data :
std_logic_vector(7 downto 0);
+reg [uarts - 1:0] sig_send;
+reg [uarts - 1:0] sig_valid;
+reg [8 * (uarts - 1) + 7:0] sig_rx_data;
+reg [8 * (uarts - 1) + 7:0] sig_tx_data;  //signal sig_rx_data :
std_logic_vector(7 downto 0);
 //signal sig_tx_data : std_logic_vector(7 downto 0);
 reg [4:0] sig_led;
These chgs did not seem to have and impact on the way the 2uarts performed.
```

Debugging an FPGA through the serial port--first steps

```
Info: Program finished normally.
icetime -d hx8k -mtr top.rpt top.asc
// Reading input .asc file..
// Reading 8k chipdb file..
// Creating timing netlist..
// Timing estimate: 6.72 ns (148.79 MHz)
icepack top.asc top.bin
make[1]: Leaving directory '/home/devel/vhd2icestorm/verilog'
```

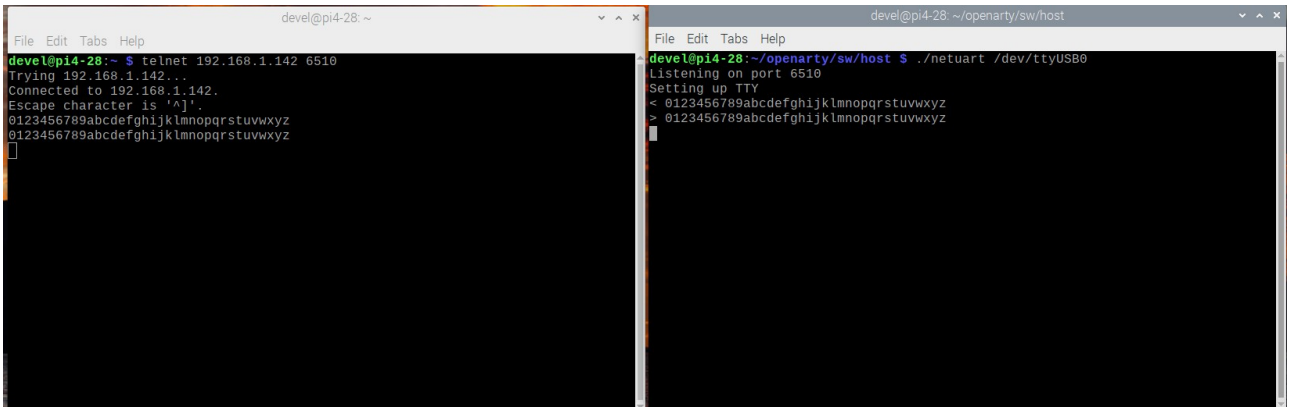
Modified vhdstorm/vhd/top.vhd to increase the baudrate from 230400 to 4M.
The follow command is used to program the FPGA **“sudo config_cat top.bin”**.

```
In the right window connected ./netuart /dev/ttyUSB0
Listening on port 6510
Setting up TTY
< 0123456789abcdefghijklmnopqrstuvwxyz
> 0123456789abcdefghijklmnopqrstuvwxyz
```

```
In the left window connected to telnet 192.168.1.142 6510
Trying 192.168.1.142...
Connected to 192.168.1.142.
Escape character is '^]'.
0123456789abcdefghijklmnopqrstuvwxyz
```

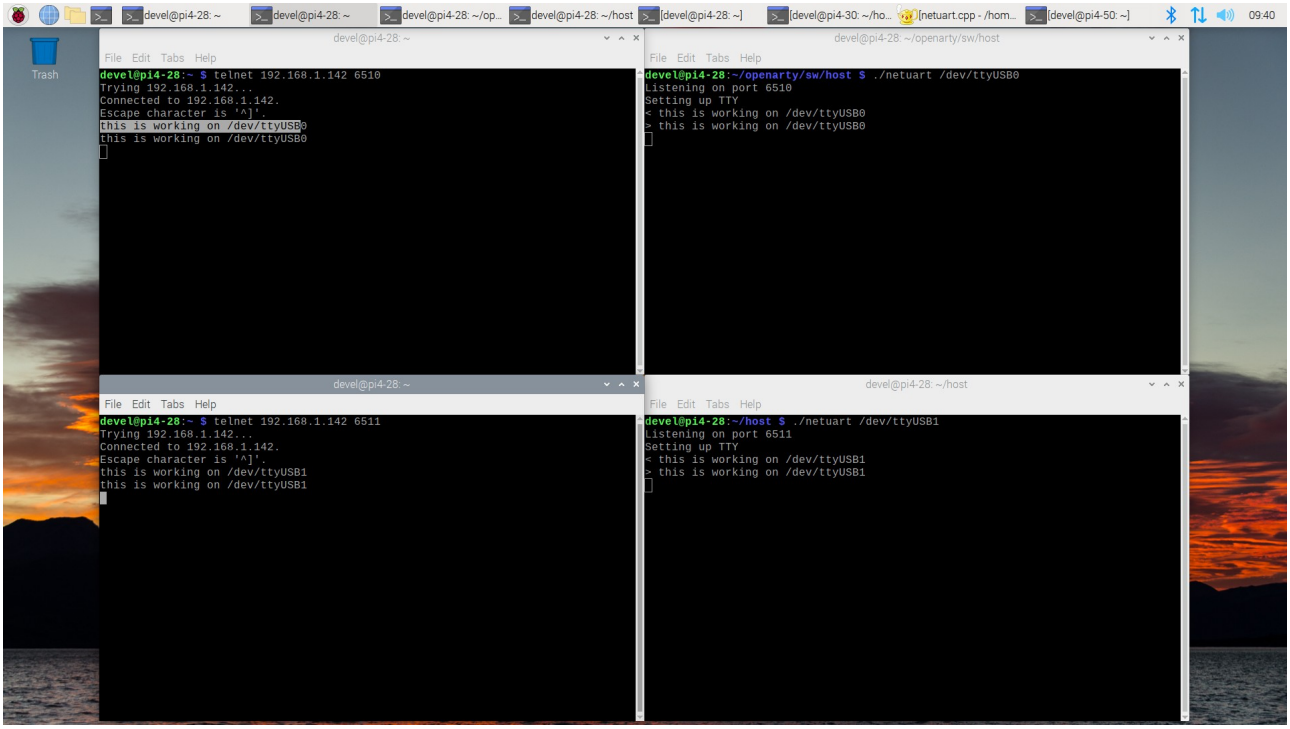
0123456789abcdefghijklmnopqrstuvwxyz

The program in the left window is executing the command **“telnet 192.168.1.142 6510”**. The program in the right window is executing the command **“./netuart /dev/ttyUSB0”**. When the characters were typed in the left window and the return entered they appeared in the right window.




```
icepll -i 100 -o 80

F_PLLIN:   100.000 MHz (given)
F_PLLOUT:   80.000 MHz (requested)
F_PLLOUT:   80.000 MHz (achieved)

FEEDBACK: SIMPLE
F_PFD:   20.000 MHz
F_VCO:  640.000 MHz

DIVR:  4 (4'b0100)
DIVF: 31 (7'b0011111)
DIVQ:  3 (3'b011)

FILTER_RANGE: 2 (3'b010)
The FPGA is running top80.bin which provides 2 uarts.
       wire    clk_80mhz, pll_locked;
        wire            s_clk;
        SB_PLL40_CORE #(
                .FEEDBACK_PATH("SIMPLE"),
                .DELAY_ADJUSTMENT_MODE_FEEDBACK("FIXED"),
                .DELAY_ADJUSTMENT_MODE_RELATIVE("FIXED"),
                .PLLOUT_SELECT("GENCLK"),
                .FDA_FEEDBACK(4'b1111),
                .FDA_RELATIVE(4'b1111),
                .DIVR(4'b0100),         // DIVR =  4
                .DIVF(7'b0011111),              // DIVQ =  31
                .DIVQ(3'b011),          // DIVF =  3
                .FILTER_RANGE(3'b010)   // FILTER_RANGE = 2
        ) plli (
                .REFERENCECLK     (clk        ),
                .PLLOUTCORE     (clk_80mhz    ),
                .LOCK           (pll_locked  ),
                .BYPASS         (1'b0        ),
                .RESETB         (1'b1        )
        );
        //SB_GB global_buffer(clk_40mhz, s_clk);
        assign  s_clk = clk_80mhz;

=== top ===
```

```
   Number of wires:                114
   Number of wire bits:            396
   Number of public wires:         114
   Number of public wire bits:     396
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                285
     SB_CARRY                       36
     SB_DFF                          4
     SB_DFFE                        56
     SB_DFFESR                      36
     SB_DFFSR                       36
     SB_DFFSS                        8
     SB_LUT4                       108
     SB_PLL40_CORE                   1
=== top ===

   Number of wires:                114
   Number of wire bits:            396
   Number of public wires:         114
   Number of public wire bits:     396
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                285
     SB_CARRY                       36
     SB_DFF                          4
     SB_DFFE                        56
     SB_DFFESR                      36
     SB_DFFSR                       36
     SB_DFFSS                        8
     SB_LUT4                       108
     SB_PLL40_CORE                   1


Info: Program finished normally.
// Reading input .asc file..
// Reading 8k chipdb file..
// Creating timing netlist..
// Timing estimate: 5.92 ns (168.89 MHz)
// Checking 12.50 ns (80.00 MHz) clock constraint: PASSED.

Created a 2nd netuart which uses port 6511 instead of port 6510.
```


devel@pi4-28: ~
devel@pi4-28: ~/op...
devel@pi4-28: ~/host
[devel@pi4-28: ~]
[devel@pi4-30: ~/ho...
[netuart.cpp - /hom...
[devel@pi4-50: ~]
09:40
Trash
devel@pi4-28: ~
File Edit Tabs Help
devel@pi4-28:~ $ telnet 192.168.1.142 6510
Trying 192.168.1.142...
Connected to 192.168.1.142.
Escape character is '^]'.
this is working on /dev/ttyUSB0
this is working on /dev/ttyUSB0
devel@pi4-28:~/openarty/sw/host $ ./netuart /dev/ttyUSB0
Listening on port 6510
Setting up TTY
< this is working on /dev/ttyUSB0
> this is working on /dev/ttyUSB0
devel@pi4-28: ~
File Edit Tabs Help
devel@pi4-28:~ $ telnet 192.168.1.142 6511
Trying 192.168.1.142...
Connected to 192.168.1.142.
Escape character is '^]'.
this is working on /dev/ttyUSB1
this is working on /dev/ttyUSB1
devel@pi4-28: ~/host
File Edit Tabs Help
devel@pi4-28:~/host $ ./netuart /dev/ttyUSB1
Listening on port 6511
Setting up TTY
< this is working on /dev/ttyUSB1
> this is working on /dev/ttyUSB1