*******DRAFT*****

SLIP for Ultibo UART Following Synapase

03/25/20

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This test was run on 03/25/20.

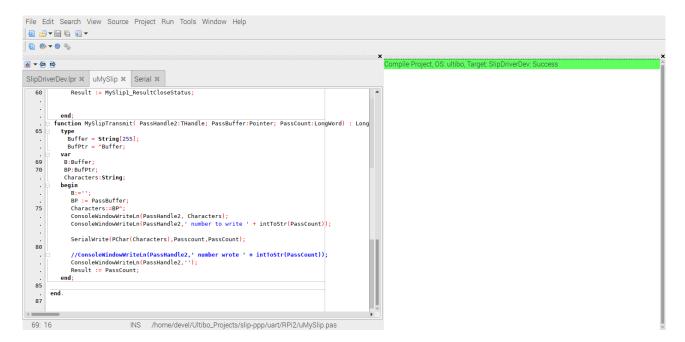
00000000 41 42 43 31 32 33 34 35 0A 41 42 43 31 32 33 34 ABC12345.ABC1234 00000010 35 0A 41 42 43 31 32 33 34 35 36 37 38 39 30 41 5.ABC1234567890A 00000020 42 43 31 32 33 34 35 36 37 38 39 30 0A BC1234567890.

Compile time is less than a min. Using Lazarus FPC.

devel@mypi3-15:~/Ultibo_Projects/slip-ppp/uart/RPi2 \$./upker7.sh Updating kernel7.img tftp> tftp> Sent 2837720 bytes in 14.8 seconds tftp> done

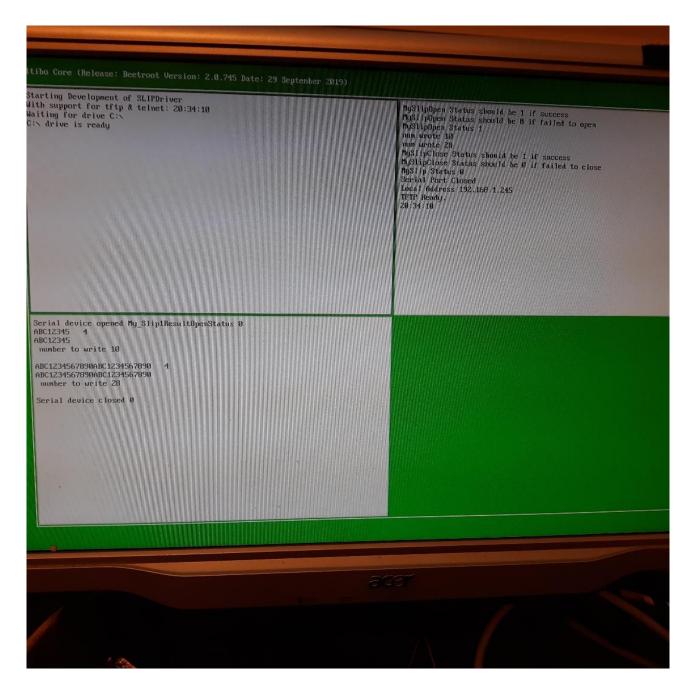
-rwxr-xr-x 1 devel devel 2837720 Mar 26 12:56 kernel7.img

Time to reboot after the transfer of kernel7.img completed 31.79 sec.



https://github.com/develone/Ultibo Projects/tree/master/slip-ppp/uart/RPi2

Ultibo Test System.



Minicom

