VHDL implementation of a 5-stage pipelined MIPS processor

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***Abstract*—The MIPS processor is the most widely used processor example in academia for it is simple enough to understand and teach with its classic RISC architecture yet can implement new architectural design with little changes to the core architecture. In this article, we will present our attempt at implementing a MIPS processor in VHDL along with some optimization we tried. The different optimization are also compared to find an optimal design amongst those tried.**

I. Introduction

II. Optimization

To optimize the performance of our pipelined processor, we decided to implement prediction hardware to reduce the number of invalid instruction fetch after a branch instruction. First we implemented a one bit predictor as a proof of concept and then implemented the two bit predictor. We compared the performance of both based on <FIND PERFORMANCE CRITERIA>.

A. One Bit Predictor

The first optimization we implemented was adding a 1 bit predictor to the fetch stage. The predictor monitors the output of the branch resolution hardware in the decode stage and records the result of the latest branching instruction. It also records the program counter associated with that instruction. The predictor then compares the program counter to the recorded counter for the prediction. Upon match, it will set the next program counter address to the address it recorded when updating the prediction from the decode stage. Finally, if the prediction was wrong, the predictor will stall the wrong instruction and update the records for the next iteration.

B. Two Bit Predictor

The next iteration of the predictor was building a two bit predictor. It's interface to the rest of the fetch and decode stage is the same, except that the internal structure uses a state machine instead of a blind comparator to drive the prediction output. The state machine was implemented according to the behavior specified in the lecture slides, lecture 13, page 17. The two bit predictor implements the same wrong prediction detection and correction strategy as the one bit predictor.