

Time-energy Measurements of Shared-memory Applications on Modern Multicore Systems

Dumitrel Loghin, Yong Meng Teo
Department of Computer Science
National University of Singapore
[dumitrel,teoym]@comp.nus.edu.sg

ABSTRACT

In this article, we present the time-energy data collected and analyzed in our research paper entitled “The Time and Energy Efficiency of Modern Multicore Systems”. While the full data set and the source code are available on Github, this data-in-brief article includes some samples, describes the experimental setup and explains how to use the data in conjunction with our time-energy models.

1. INTRODUCTION

Motivated by the increasing number of processor cores (CPU cores) integrated in the same die, we extend Amdahl’s [4] and Gustafson’s [5] speedup laws to determine both the time and energy efficiency of shared-memory applications on multicore systems. In this paper, we describe our measurements methodology and provide data samples used in our research paper entitled “The Time and Energy Efficiency of Modern Multicore Systems” [2]. The full dataset and the source code of our research models are available on Github [3].

The contributions of this article are:

- the experimental methodology used to acquire time-energy measurements on modern multicore systems. These systems include both high-performance and low-power, homogeneous and heterogeneous, and are representative for server, desktop and mobile domains
- a dataset that includes execution time and energy measurements of up to ten shared-memory applications covering multiple domains on a wide range of modern multicore systems
- the source code implementing the models described in our previous works [1, 2] which serve as a starting point for researchers, developers and system designers

In the next section, we present the format of raw and processed data and include some samples. In Section 3, we describe our methodology.

2. DATA

We provide two data sets for each system and application evaluated in our work, (i) measured, or raw, time-energy values and (ii) model output. Measured time-energy data consists of seven columns, as shown in Table 1 for EP execution on Xeon (see next section for the description of the experimental setup). Each row represents the execution of the given application on the target system using a certain number of cores. The columns represent the number of nodes, number of cores per node, the core clock frequency of the cores, the execution time in seconds (s), the energy in Watts-hour (Wh) and Joules (J), respectively, and the average power consumption in Watts (W). The number of nodes is always one because these experiments are run on single-node shared-memory multicore systems. Our models [1,2] are using the following key columns: Cores, Time and Energy.

For heterogeneous systems, such as XU3 and TX2, we provide four measured data sets per application, as exemplified in Tables 2-5 for EP on XU3. The first two data sets represent the execution with OpenMP static scheduling on big and little cores, respectively. The last two data sets represent the execution on all cores using static and dynamic OpenMP execution, respectively.

Table 1. Raw Time-Energy Measurements (EP on Xeon)

| Procs | Cores | Freq | Time[s] | Energy[Wh] | Energy[J] | AvgPower[W] |
|-------|-------|---------|---------|------------|-----------|-------------|
| 1 | 1 | 2.20GHz | 384.14 | 8.46 | 30456 | 79.48 |
| 1 | 2 | 2.20GHz | 195.63 | 4.60 | 16560 | 84.93 |
| 1 | 3 | 2.20GHz | 138.33 | 3.36 | 12096 | 88.32 |
| 1 | 4 | 2.20GHz | 106.39 | 2.71 | 9756 | 92.10 |
| 1 | 5 | 2.20GHz | 89.29 | 2.31 | 8316 | 94.73 |
| 1 | 6 | 2.20GHz | 77.76 | 2.08 | 7488 | 97.18 |
| 1 | 7 | 2.20GHz | 69.07 | 1.87 | 6732 | 99.04 |
| 1 | 8 | 2.20GHz | 62.09 | 1.73 | 6228 | 100.73 |
| 1 | 9 | 2.20GHz | 55.23 | 1.58 | 5688 | 103.89 |
| 1 | 10 | 2.20GHz | 49.65 | 1.46 | 5256 | 107.49 |
| 1 | 11 | 2.20GHz | 49.64 | 1.46 | 5256 | 107.85 |
| 1 | 12 | 2.20GHz | 45.94 | 1.37 | 4932 | 109.42 |
| 1 | 13 | 2.20GHz | 42.85 | 1.28 | 4608 | 110.22 |
| 1 | 14 | 2.20GHz | 40.12 | 1.20 | 4320 | 110.81 |
| 1 | 15 | 2.20GHz | 37.48 | 1.14 | 4104 | 112.08 |
| 1 | 16 | 2.20GHz | 35.42 | 1.10 | 3960 | 112.64 |
| 1 | 17 | 2.20GHz | 34.02 | 1.06 | 3816 | 112.98 |
| 1 | 18 | 2.20GHz | 31.58 | 0.97 | 3492 | 113.88 |
| 1 | 19 | 2.20GHz | 29.93 | 0.92 | 3312 | 114.54 |
| 1 | 20 | 2.20GHz | 28.83 | 0.89 | 3204 | 115.21 |

Table 2. Raw Time-Energy Measurements on Big Cores with Static Scheduling (EP on XU3)

| #Procs | Cores | Freq | Time[s] | Energy[Wh] | Energy[J] | AvgPower[W] |
|--------|-------|---------|---------|------------|-----------|-------------|
| 1 | 1 | 2.00GHz | 710.81 | 0.02 | 60.12 | 9.27 |
| 1 | 2 | 2.00GHz | 363.58 | 0.01 | 42.12 | 12.51 |
| 1 | 3 | 2.00GHz | 250.09 | 0.01 | 36.00 | 15.03 |
| 1 | 4 | 2.00GHz | 197.88 | 0.01 | 29.52 | 15.56 |

Table 3. Raw Time-Energy Measurements on Little Cores with Static Scheduling (EP on XU3)

| #Procs | Cores | Freq | Time[s] | Energy[Wh] | Energy[J] | AvgPower[W] |
|--------|-------|---------|---------|------------|-----------|-------------|
| 1 | 1 | 2.00GHz | 1607.79 | 0.03 | 99.00 | 6.65 |
| 1 | 2 | 2.00GHz | 820.67 | 0.01 | 53.28 | 7.10 |
| 1 | 3 | 2.00GHz | 548.60 | 0.01 | 37.80 | 7.51 |
| 1 | 4 | 2.00GHz | 413.19 | 0.01 | 29.88 | 7.89 |

Table 4. Raw Time-Energy Measurements on All Cores with Static Scheduling (EP on XU3)

| #Procs | Cores | Freq | Time[s] | Energy[Wh] | Energy[J] | AvgPower[W] |
|--------|-------|---------|---------|------------|-----------|-------------|
| 1 | 1 | 2.00GHz | 714.61 | 0.017 | 61.2 | 9.24 |
| 1 | 2 | 2.00GHz | 363.75 | 0.012 | 43.2 | 12.45 |
| 1 | 3 | 2.00GHz | 250.87 | 0.01 | 36 | 14.69 |
| 1 | 4 | 2.00GHz | 198.74 | 0.008 | 28.8 | 15.32 |
| 1 | 5 | 2.00GHz | 321.7 | 0.01 | 36 | 10.94 |
| 1 | 6 | 2.00GHz | 273.5 | 0.008 | 28.8 | 11.10 |
| 1 | 7 | 2.00GHz | 235.14 | 0.007 | 25.2 | 11.35 |
| 1 | 8 | 2.00GHz | 206.75 | 0.007 | 25.2 | 11.67 |

Table 5. Raw Time-Energy Measurements on All Cores with Dynamic Scheduling (EP on XU3)

| #Procs | Cores | Freq | Time[s] | Energy[Wh] | Energy[J] | AvgPower[W] |
|--------|-------|---------|---------|------------|-----------|-------------|
| 1 | 1 | 2.00GHz | 709.82 | 0.017 | 61.2 | 9.25 |
| 1 | 2 | 2.00GHz | 364.94 | 0.012 | 43.2 | 12.47 |
| 1 | 3 | 2.00GHz | 248.67 | 0.01 | 36 | 15.11 |
| 1 | 4 | 2.00GHz | 198.96 | 0.008 | 28.8 | 15.31 |
| 1 | 5 | 2.00GHz | 179.27 | 0.007 | 25.2 | 15.32 |
| 1 | 6 | 2.00GHz | 162.8 | 0.007 | 25.2 | 15.41 |
| 1 | 7 | 2.00GHz | 149.53 | 0.006 | 21.6 | 15.54 |
| 1 | 8 | 2.00GHz | 137.73 | 0.006 | 21.6 | 15.67 |

Model output data consists of nine columns, as shown in Table 6 for EP running on Xeon when Amdahl's law [4] for speedup is used. The first column represents the number of cores used for execution, while the other eight columns represent measured and predicted speedup, energy savings, execution time and energy, respectively. In addition, the source code implementing the model reports the sequential fraction and the RMSD between measured and predicted values across all core counts.

The speedup values for EP running on Xeon are plotted in Figure 1 and summarized in Table 6. The predicted values are computed using Amdahl's law [4]. On the other hand, Figure 2 plots the same measurements, while the predicted speedup is determined using Gustafson's law [5]. The results for other systems are presented in our research papers [1,2].

Table 6. Model Output Data (EP on Xeon, Amdahl's Law)

| Cores | Measured Speedup | Predicted Speedup | Measured Energy Savings | Predicted Energy Savings | Measured Time | Predicted Time | Measured Energy | Predicted Energy |
|--------------|-----------------------------|------------------------------|--|---|--------------------------|---------------------------|----------------------------|-----------------------------|
| 1 | 1 | 1 | 0 | 0 | 384.1 | 384.1 | 30530 | 24233.8 |
| 2 | 1.96 | 1.94 | 0.456 | 0.464 | 195.6 | 198 | 16615.1 | 13024.5 |
| 3 | 2.78 | 2.82 | 0.6 | 0.619 | 138.3 | 136 | 12217.2 | 9288 |
| 4 | 3.61 | 3.66 | 0.679 | 0.696 | 106.4 | 105 | 9798.4 | 7419.8 |
| 5 | 4.3 | 4.45 | 0.723 | 0.743 | 89.3 | 86.4 | 8458.3 | 6298.9 |
| 6 | 4.94 | 5.19 | 0.752 | 0.773 | 77.8 | 73.9 | 7556.8 | 5551.6 |
| 7 | 5.56 | 5.9 | 0.776 | 0.796 | 69.1 | 65.1 | 6841 | 5017.8 |
| 8 | 6.19 | 6.57 | 0.795 | 0.812 | 62.1 | 58.4 | 6254.2 | 4617.5 |
| 9 | 6.96 | 7.21 | 0.812 | 0.825 | 55.2 | 53.3 | 5737.6 | 4306.1 |
| 10 | 7.74 | 7.82 | 0.825 | 0.835 | 49.6 | 49.1 | 5336.9 | 4057 |
| 11 | 7.74 | 8.4 | 0.825 | 0.844 | 49.6 | 45.7 | 5353.9 | 3853.2 |
| 12 | 8.36 | 8.95 | 0.835 | 0.851 | 45.9 | 42.9 | 5026.8 | 3683.4 |
| 13 | 8.96 | 9.47 | 0.845 | 0.857 | 42.9 | 40.5 | 4723 | 3539.7 |
| 14 | 9.57 | 9.98 | 0.854 | 0.862 | 40.1 | 38.5 | 4445.6 | 3416.5 |
| 15 | 10.25 | 10.46 | 0.862 | 0.866 | 37.5 | 36.7 | 4200.6 | 3309.7 |
| 16 | 10.85 | 10.92 | 0.869 | 0.87 | 35.4 | 35.2 | 3989.6 | 3216.3 |
| 17 | 11.29 | 11.36 | 0.874 | 0.874 | 34 | 33.8 | 3843.4 | 3133.9 |
| 18 | 12.16 | 11.79 | 0.882 | 0.877 | 31.6 | 32.6 | 3596.3 | 3060.6 |
| 19 | 12.83 | 12.19 | 0.888 | 0.879 | 29.9 | 31.5 | 3428.1 | 2995.1 |
| 20 | 13.32 | 12.59 | 0.891 | 0.882 | 28.8 | 30.5 | 3321.6 | 2936.1 |

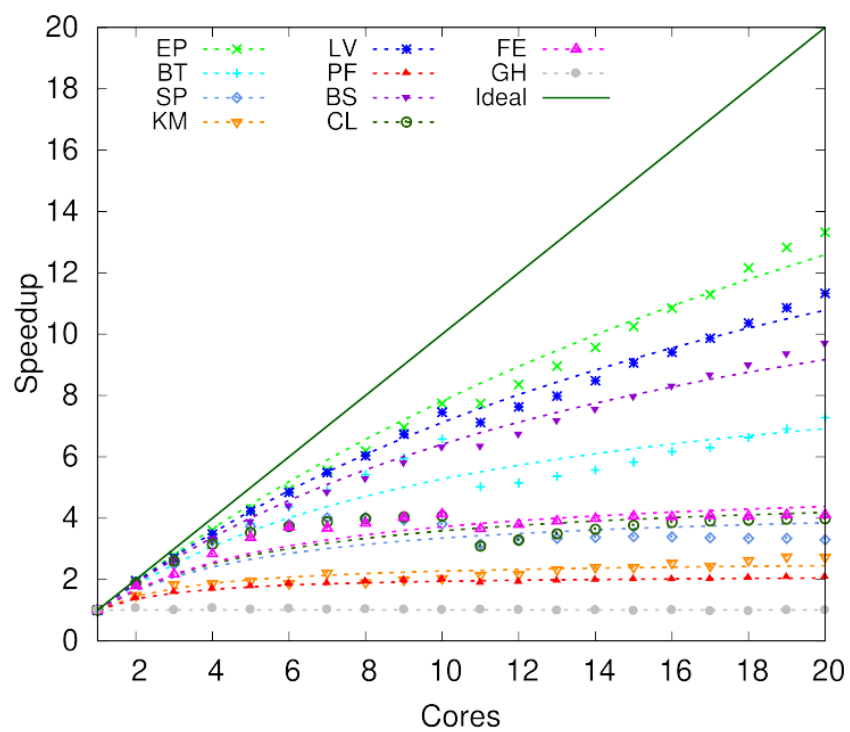


Figure 1. Amdahl Speedup on Xeon

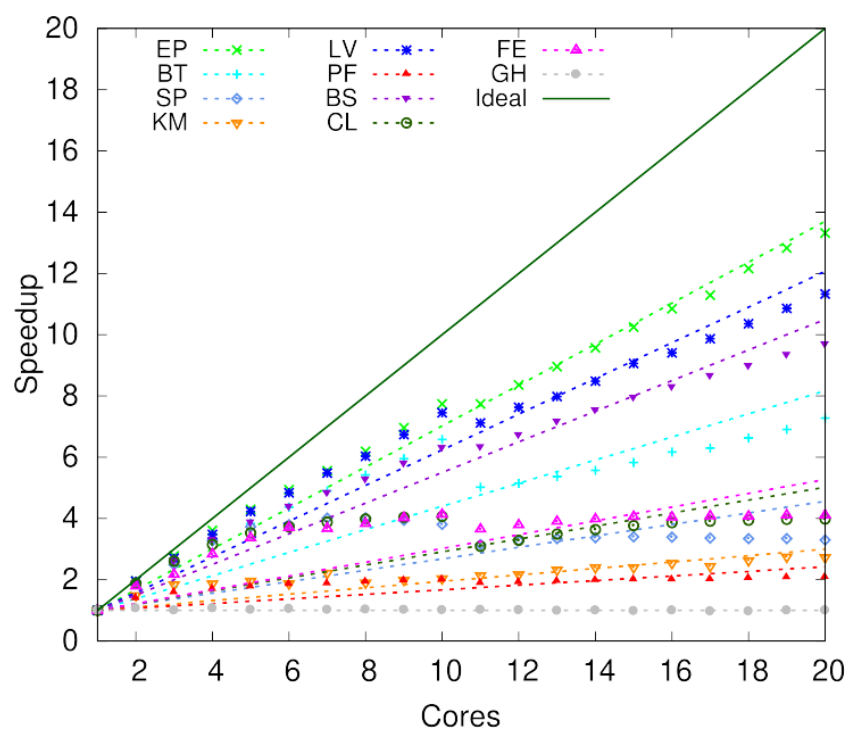


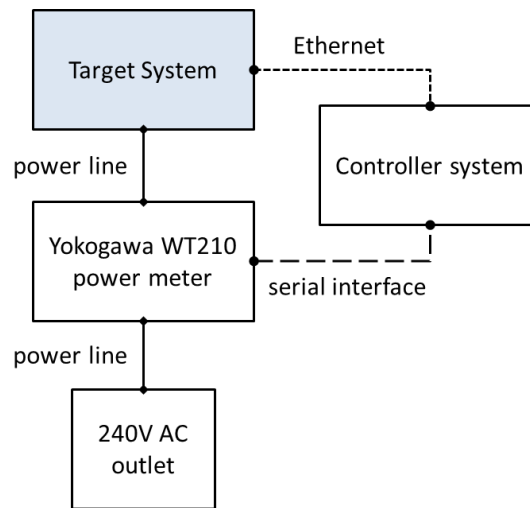
Figure 2. Gustafson Speedup on Xeon

Table 7. Systems

| System | CPU | Cores | Frequency [GHz] | Memory [GB] |
|--------|--|------------|-----------------|-------------|
| AMD | AMD Opteron K10 | 48 | 2.10 | 64 (NUMA) |
| ARM | Cavium ThunderX (64-bit ARM) | 48 | 2.00 | 128 (UMA) |
| Xeon | Intel Xeon E5-2630 v4 | 10 (20 HT) | 2.20 | 64 (UMA) |
| i7 | Intel Core i7-6700 | 4 (8 HT) | 3.40 | 16 |
| Pi3 | ARM Cortex-A53 | 4 | 1.20 | 1 |
| XU3 | ARM big.LITTLE HMP (ARM Cortex-A15 + ARM Cortex-A7) | 8 (4+4) | 2.00 | 2 |
| TX2 | HMP (Denver + ARM Cortex-A57) | 6 (2+4) | 2.04 | 8 |

Table 8. Applications

| Application | Benchmark Suite | Input Size | OpenMP Scheduling |
|-----------------------------------|-----------------|---|-------------------|
| EP (Embarrassingly Parallel) | NPB [6] | Class C (Random-number pairs: 2^{32}) | default |
| BT (Block Tri-diagonal Solver) | NPB [6] | Class C (Grid size: 162 x 162 x 162, Iterations: 200) | static |
| SP (Scalar Penta-Diagonal solver) | NPB [6] | Class C (Grid size: 162 x 162 x 162, Iterations: 400) | static |
| LV (LavaMD) | Rodinia [7] | Boxes1d: 24 | default |
| KM (Kmeans) | Rodinia [7] | n=1,000,000 m=34 k=5 | static |
| PF (Pathfinder) | Rodinia [7] | Width (rows): 900000, number of steps (columns): 500 | default |
| BS (BlackScholes) | Parsec [8] | 4,000,000 options | default |
| CL (CloverLeaf) | Mantevo [9] | Grid size 1000, end_time=30.0 | default |
| FE (miniFE) | Mantevo [9] | nx=150 | default |
| GH (miniGhost) | Mantevo [9] | nx=100, num_tsteps=1,000 | default |

**Figure 3. Experimental Setup**

3. EXPERIMENTAL DESIGN, MATERIALS AND METHODS

The experimental setup used in our work is depicted in Figure 3. To collect power and energy, we use a Yokogawa WT201 power meter connected to the 240V AC power line. A controller system is used to start the experiments and collect execution and power data. The power and energy samples are collected once per second.

Table 7 summarizes the characteristics of the target systems used in our work. This table should serve as a reference for users that apply our models [1,2], or any other time-energy models for shared-memory multicore systems. The systems are selected to represent both homogeneous and heterogeneous systems, both brawny and wimpy nodes, as well as server, desktop and mobile domains. Hence, AMD and Xeon represent homogeneous brawny servers, while ARM is an emerging homogeneous wimpy server. i7 represents homogeneous brawny desktops and Pi3 represents homogeneous wimpy mobile devices. Both systems have low core counts, which is typical for desktop and mobile domains. Lastly, XU3 and TX2 represent heterogeneous systems, both being wimpy mobile nodes. To the best of our knowledge, there is no heterogeneous multicore server system available in the market.

Table 8 summarizes the shared-memory applications used in our work. These applications are selected from well-known benchmarking suites, such as NPB [6], Rodinia [7], Parsec [8] and Mantevo [9]. These applications cover a wide range of sequential fractions, from less than 1% to more than 99%. In addition to the first seven applications presented in our previous work [1,2], we provide data for CloverLeaf (CL), miniFE (FE) and miniGhost (GH) benchmarks from Mantevo suite [9], running on Xeon, i7 and Pi3.

ACKNOWLEDGEMENTS

This work was supported by the Ministry of Education of Singapore through Academic Research Fund Tier 1 and Tier 3. The authors thank GIGABYTE for providing access to the 48-core R120-T30 ARM server, and NVIDIA for providing the Jetson TX2 development kit.

REFERENCES

- [1] D. Loghin, Y. M. Teo, The Energy Efficiency of Modern Multicore Systems, Proc. of 47th International Conference on Parallel Processing Companion, pages 28:1–28:10, 2018.
- [2] D. Loghin, Y. M. Teo, The Time and Energy Efficiency of Modern Multicore Systems, Parallel Computing, 2019.
- [3] Datasets and Source Code, <https://github.com/dloghin/multicores-time-energy>
- [4] G. M. Amdahl, Validity of the Single Processor Approach to Achieving Large Scale Computing Capabilities, Proc. of April 18-20, 1967, Spring Joint Computer Conference, pages 483–485, 1967.

- [5] J. L. Gustafson, Reevaluating Amdahl's Law, *Communications of the ACM*, 31(5):532–533, 1988.
- [6] D. Bailey, T. Harris, W. Saphir, R. Van Der Wijngaart, A. Woo, M. Yarrow, The NAS Parallel Benchmarks 2.0, Technical Report NAS-95-020, NASA Ames Research Center, 1995.
- [7] S. Che, M. Boyer, J. Meng, D. Tarjan, J. W. Sheaffer, S.-H. Lee, K. Skadron, Rodinia: A Benchmark Suite for Heterogeneous Computing, *Proc. of 2009 IEEE International Symposium on Workload Characterization*, pages 44–54, 2009.
- [8] C. Bienia, S. Kumar, J. P. Singh, K. Li, The PARSEC Benchmark Suite: Characterization and Architectural Implications, *Proc. of 17th International Conference on Parallel Architectures and Compilation Techniques*, pages 72–81, 2008.
- [9] M. A. Heroux, D. W. Doerfler, P. S. Crozier, J. M. Willenbring, H. C. Edwards, A. Williams, M. Rajan, E. R. Keiter, H. K. Thornquist, R. W. Numrich, Improving Performance via Mini-applications, Technical Report SAND2009-5574, Sandia National Laboratories, 2009.