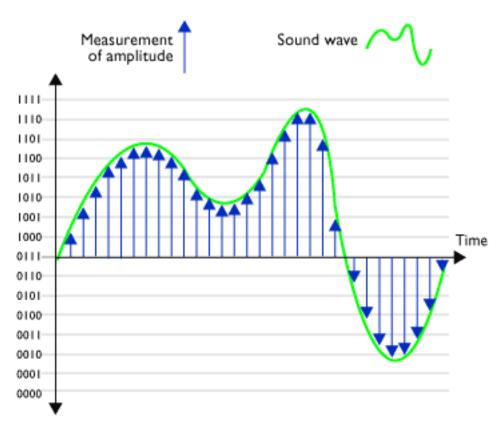
Conversão de Analógico para Digital



Each measurement is assigned a number (byte) according to its amplitude. The end result is a file comprising a string of bytes, eg ... 1001 1110 0001 1010 0111 0100 1111 1101 etc

Conversor A/D por aproximações sucessivas

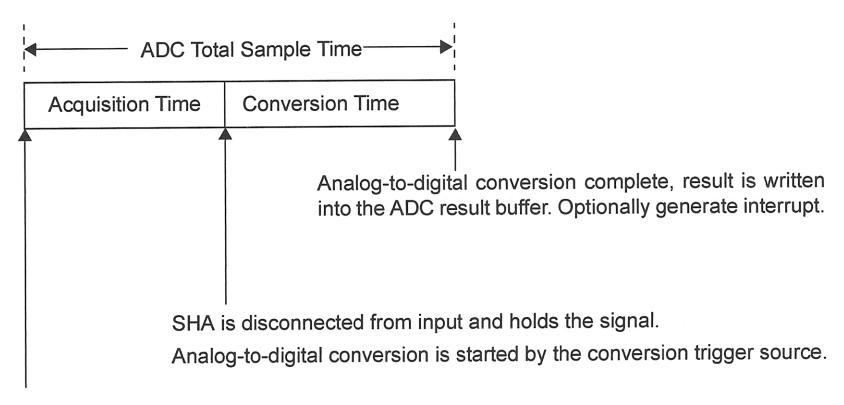
Successive Approximation Register (SAR) clock Up-Down Up-Down Counter Control Digital Output V_{DAC} DA Analog Input

Sample-and-Hold (SH) Output

PIC32 10-bit ADC VREF+(1) AVDD VREF-(1) AVSS Successive Approximation ADC 16 canais VCFG<2:0> ADC1BUF0 AN0 ADC1BUF1 AN15⊠ ADC1BUF2 SHA VREFH VREFL Channel Scan SAR ADC CH0SB<3:0> CH0SA<3:0> CSCNA AN1 ⊠ ADC1BUFE VREFL ADC1BUFF **SAR** – Successive Approx. Reg. CHONA CHONB **SHA** – Sample and Hold Amplifier

Alternate Input Selection

ADC Timing



SHA is connected to the analog input pin for sampling.

Acquisition Time – automático: determinado por SAMC (AD1CON3<12:8>) ou

manual: SAMP bit (AD1CON1<1>)

Conversion Time – 12 ciclos de relógio

Amostragem pode ser feita uma única vez, periodicamente ou desencadeada por um trigger

Registos de Controle da ADC

- AD1CON1: ADC Control Register 1
- AD1CON2: ADC Control Register 2
- AD1CON3: ADC Control Register 3

The AD1CON1, AD1CON2 and AD1CON3 registers control the operation of the ADC module.

- AD1CHS: ADC Input Select Register
 - The AD1CHS register selects the input pins to be connected to the SHA.
- AD1PCFG: ADC Port Configuration Register^(1,2)
 - The AD1PCFG register configures the analog input pins as analog inputs or as digital I/O.
- AD1CSSL: ADC Input Scan Select Register⁽¹⁾
 - The AD1CSSL register selects inputs to be sequentially scanned.

Select the voltage reference source using VCFG<2:0> (AD1CON2<15:13>) (see 17.4.7).
 Select the Scan mode using CSCNA (AD1CON2<10>) (see 17.4.8).
 Set the number of conversions per interrupt SMP<3:0> (AD1CON2<5:2>), if interrupts are

Configure the analog port pins in AD1PCFG<15:0> (see 17.4.1).

1.

2.

3.

4.

to be used (see 17.4.9).

Set Buffer Fill mode using BUFM (AD1CON2<1>) (see 17.4.10).
 Select the MUX to be connected to the ADC in ALTS AD1CON2<0> (see 17.4.11).

Select the analog inputs to the ADC multiplexers in AD1CHS<32:0> (see 17.4.2).

Select the sample clock source using SSRC<2:0> (AD1CON1<7:5>) (see 17.4.4).

Select the format of the ADC result using FORM<2:0> (AD1CON1<10:8>) (see 17.4.3).

Select the ADC clock source using ADRC (AD1CON3<15>) (see 17.4.12).
 Select the sample time using SAMC<4:0> (AD1CON3<12:8>), if auto-convert is to be used (see 17-2).

12. Select the ADC clock prescaler using ADCS<7:0> (AD1CON3<7:0>) (see 17.4.12).

- 13. Turn the ADC module on using AD1CON1<15> (see 17.4.14).
- Note: Steps 1 through 12, above, can be performed in any order, but Step 13 must be the final step in every case.
- 14. To configure ADC interrupt (if required):
 a) Clear the AD1IF bit (IFS1<1>) (see 17.7).
 - Select ADC interrupt priority AD1IP<2:0> (IPC<28:26>) and subpriority AD1IS<1:0> (IPC<24:24>) if interrupts are to be used (see 17.7).
- 15. Start the conversion sequence by initiating sampling (see 17.4.15).