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SIM-69

DESCRIPTION

SIM-69 is a Motorola MC6809 based single board computer running at 2Mhz and comes with a full complement of I/O for interfacing, including an I2C bus. The board can be mounted in a Mini-ITX case if desired.

HARDWARE

SIM-69 is based on the Motorola MC68B09, or Hitachi CMOS version, the HD63B09 and is located at U2. This design uses the internal clock version, not the "E" version of the 6809 CPU that requires an external quadrature clock generator. This simplifies the design somewhat and only requires a single 8.00Mhz crystal oscillator at X1 to run the system with a bus frequency of 2.00Mhz. A Power Design chip is provided at U1 to generate a clean power up reset signal for the CPU, along with a reset button at SW1 and a connector for a case Reset button at J25 if desired. Full CPU bus signals are provided on 40 pin connector JP1 for use in expanding the system if desired. Additional +5v and Ground pins are provided on connector JP2.

Address decoding is done by a pair of IC's, a GAL22V10 and a 74LS138 (or 74HCT138). Two versions of the GAL code are provided, depending on the type and size of RAM chip used for system RAM. A 32K GAL is used if a HM62256 RAM chip is installed. A 64K GAL is used if a W24512AK RAM chip is installed. Note that only a total of 42KB of the 64KB ram chip is usable as ROM and I/O take up the remaining space in the 64KB address map.

System RAM is either a "skinny" DIP 64KB ram chip at U5 or a 32KB "wide" DIP chip inserted across the U5 and J55 connector.

System ROM is a 27C256 style chip used at U3. Only 12KB of ROM space is decoded at the upper end of the memory map. Address line A14 of U3 is brought out to a Jumper at J2 to allow bank switching the ROM. For example, a monitor ROM can be burned into one half of the chip and Extended Basic can be burned into the other half, then the system can boot into either code at power up depending on the jumper at J2.

J2 ROM bank switch

J2	1-2	jumper removed	Access upper half of ROM
	1-2	jumper installed	Access lower half of ROM

Non-volatile storage is accomplished with an EEPROM at U4. Either a AT28C64 or AT28C256 can be used. The EEPROM is mapped into 8KB of space in the memory map. If a AT28C256 is used, the total 32KB of EEPROM in the chip is bank switched into that 8KB space, either manually or programmatically using VIA2 Port B pins. This is selected by J23 and J24. Also, the Write Enable on the EEPROM is controlled either manually or programmatically with a VIA2 port B pin using J22. Code is provided in the SmartBug monitor to automatically select pages (or Banks) to read and write from the EEPROM if J22, J23, J24 are all set to pins 1-2.

J22, J23, J24 EEPROM Bank Addressing and Write Enable

J22	1-2	jumper installed	/WE software controlled by VIA2 PB2
	2-3	jumper installed	EEPROM in Write Enabled state
		no jumper	EEPROM is Read Only

Bank	J23	J24	
	1-2	1-2	Bank Switching software controlled by VIA2 PB0 and PB1
	2-3	2-3	Manual Bank 0
	2-3	NC	Manual Bank 1
	NC	2-3	Manual Bank 2
	NC	NC	Manual Bank 3

A LCD2004a style 20x4 LCD panel can be mounted on the motherboard at J4. This LCD is directly on the CPU bus and is address decoded by the GAL. LCD contrast can be adjusted by RV1 potentiometer. Backlight power is provided by R3. Subroutines are provided in the SmartBug monitor for initializing and displaying text on the LCD panel.

Two serial ports are provided by U12 and U13 with type 65B51 ACIA's. SmartBug only uses Serial Port 1, leaving the second serial port free for other uses. Both serial ports use crystal oscillator X2 for baud rate generation. Baud rates are available up to 38.4Kbaud, in the case of serial port1 this is selectable by a command in SmartBug and defaults to 19.2K. Both serial ports are available on DB9 connectors. If it is desired to use a FTDI style USB to Serial converter, connectors J18 and J19 are available for use, after the corresponding MAX232 level shifter chip is removed from its socket

at U14 or U15. Note that some USB to Serial converters supply +5V power from the USB port. To prevent back feeding the SIM-69 board from USB, bend out or cut off the Vcc pin on the converter board. Mounting holes are provided for use with standoffs to allow Peter Hizalev's VT100 terminal daughter board to be mounted on the SIM-69 board and then a PS/2 style keyboard and VGA monitor can be used. See Peter's Tindie page for purchasing his VT100 board.

Two 65B22 VIA's are located at U10 and U11 to provide parallel IO ports and timers. Each VIA can have its Interrupt pin mapped to either the IRQ or FIRQ of the CPU via Jumpers J12 and J13. All parallel IO pins are available at Connectors J14 through J17. Note that VIA2 PortB pins PB0 – PB2 are also used to control the bank switching of the EEPROM, if used and configured with jumpers J22 – J24.

J12	VIA-1 Interrupt
1-2	VIA-1 sends interrupt to CPU /IRQ
2-3	VIA-1 sends interrupt to CPU /FIRQ

J13	VIA-2 Interrupt
1-2	VIA-2 sends interrupt to CPU /IRQ
2-3	VIA-2 sends interrupt to CPU /FIRQ

An I2C bus is provided by the PCF8584 chip at U7. Clocking for the I2C bus is derived from the 8Mhz clock provided by X1. If the CPU bus speed is increased above 2Mhz by using a faster crystal oscillator, the I2C bus timing can be out of specification. Jumper J5 is used to select a slower clock to bring the I2C bus back under spec in these cases. Two I2C devices are provided for on the motherboard and connectors J7 – J10 are provided to connect up to 6 additional external I2C peripherals. Note that Smartbugs initialization routines attempts to initialize and configure the PCF8584 at power up and may hang if the chip is not present.

J5	I2C Clock Source
1-2	8Mhz clock (main clock for CPU)
2-3	2Mhz clock (E clock from CPU)

A 24LC256 32K serial EEPROM is provided at U8. Its I2C address is selectable using jumpers at J6, if another I2C device conflicts with the default address. Sample subroutines are provided in SmartBug to read and write the serial EEPROM at the default address.

J6			Serial EEPROM I2C slave address	
			Address	
out	out	out	1010111	(default)
5-6	3-4	1-2	1010000	
5-6	3-4	out	1010001	
5-6	out	1-2	1010010	
5-6	out	out	1010011	
out	3-4	1-2	1010100	etc.

A HW-111 style I2C Real Time Clock module can be installed on connector J11. Commands are provided in SmartBug to read and write the clock chip for time and date.

Connectors J3 and J25 are provided for connection to a Power LED and Reset button on a Mini-ITX case front panel if desired.

Power for the SIM-69 system is provided by an external “wall wart” style +5V DC power adaptor. Note there is no power regulation done on the SIM-69 board. Be very careful to use only a +5VDC adaptor and note the polarity voltage at Jack J1. The center pin is positive. A 2 Amp adapter is specified in the Bill of Materials. If all CMOS components are used on the motherboard, a 1 Amp adapter may be substituted.

Mounting Holes H1, H2, H3, and H4 are provided for installing the board into a mini-ITX case. Mounting hole H5 is used with a standoff to support the end of a LCD2004a module if installed. Mounting holes H4, H6, H7 and H8 are used with standoffs to support the optional VT100 board.

SOFTWARE

SmartBug is a ROM monitor written in the style of MikBug to allow entering and executing code on the SIM-69. It is contained in the ROM chip at the top 12KB of the memory map $D000 - $FFFF. At

powerup or reset, SmartBug initialized the ACIA-1 and the I2C chip, sets up the Direct Page, Stack and User Stack areas, and initializes some space in RAM for variable storage. It also checks for the presence of auto starting code in the EEPROM by checking for a AUXROM flag and if found, passes control to the AUXROM cold start vector instead of dropping into the SmartBug prompt.

SmartBug Commands are upper case two letter commands used to enter, edit and execute code.

AI	ASCII INPUT
AO	ASCII OUTPUT
AU	AUTO MEMORY INPUT
BR	BAUD RATE
CL	DISPLAY/SET CLOCK
CP	COMPARE MEMORY BLOCKS
DS	DOWNLOAD S1 S9 FILES
DI	DOWNLOAD INTEL HEX FILES
ER	READ FROM EEPROM
EW	WRITE TO EEPROM
EX	EXAMINE MEMORY
FI	FIND BYTES
FL	FILL MEMORY
GO	GOTO PROGRAM
HE	HEX DUMP OF MEMORY
MO	MOVE A BLOCK OF MEMORY
PR	PRINTER ENABLE/DISABLE
UR	USER COMMAND
VR	ROM VERSION NUMBERS
XX	EXIT BACK TO PRIMARY TASK
??	HELP SCREEN