הנדסת תוכנה

Software Engineering

מערכות משובצות מחשב (קורס מס' 10110_)

הרצאה מספר 5 – המרה של ערך אנלוגי לערך דיגיטלי

PIC32

בקורס מערכות משובצות מחשב

כתב: ד"ר מנחם אפשטיין

COMPATIBLE 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

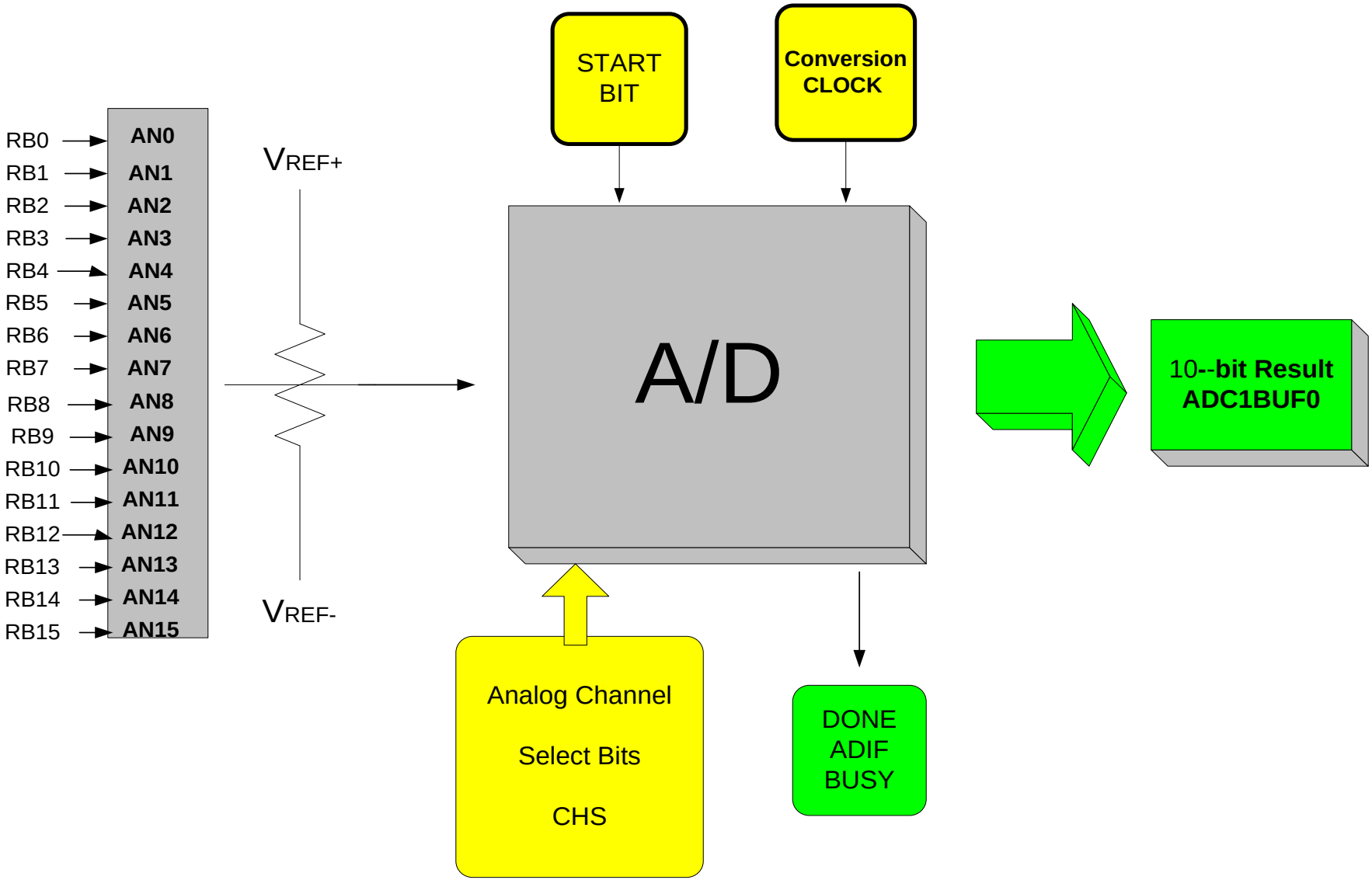

START BIT
Conversion CLOCK
RB0
RB1
RB2
RB3
RB4
RB5
RB6
RB7
RB8
RB9
RB10
RB11
RB12
RB13
RB14
RB15
AN0
AN1
AN2
AN3
AN4
AN5
AN6
AN7
AN8
AN9
AN10
AN11
AN12
AN13
AN14
AN15
VREF+
VREF-
A/D
10--bit Result
ADC1BUF0
Analog Channel
Select Bits
CHS
DONE
ADIF
BUSY

TABLE 22-1: ADC SFR SUMMARY

Virtual Address	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
BF80_9000	AD1CON1	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	ON	FRZ	SIDL	—	—	FORM2	FORM1	FORM0
		7:0	SSRC2	SSRC1	SSRC0	CLRASAM	—	ASAM	SAMP	DONE
BF80_9004	AD1CON1CLR	31:0	Write clears selected bits in AD1CON1, read yields undefined value							
BF80_9008	AD1CON1SET	31:0	Write sets selected bits in AD1CON1, read yields undefined value							
BF80_900C	AD1CON1INV	31:0	Write inverts selected bits in AD1CON1, read yields undefined value							
BF80_9010	AD1CON2	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	—	—
		7:0	BUFS	—	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
BF80_9014	AD1CON2CLR	31:0	Write clears selected bits in AD1CON2, read yields undefined value							
BF80_9018	AD1CON2SET	31:0	Write sets selected bits in AD1CON2, read yields undefined value							
BF80_901C	AD1CON2INV	31:0	Write inverts selected bits in AD1CON2, read yields undefined value							
BF80_9020	AD1CON3	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
		7:0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
BF80_9024	AD1CON3CLR	31:0	Write clears selected bits in AD1CON3, read yields undefined value							
BF80_9028	AD1CON3SET	31:0	Write sets selected bits in AD1CON3, read yields undefined value							
BF80_902C	AD1CON3INV	31:0	Write inverts selected bits in AD1CON3, read yields undefined value							
BF80_9040	AD1CHS	31:24	CH0NB	—	—	—	CH0SB3	CH0SB2	CH0SB1	CH0SB0
		23:16	CH0NA	—	—	—	CH0SA3	CH0SA2	CH0SA1	CH0SA0
		15:8	—	—	—	—	—	—	—	—
		7:0	—	—	—	—	—	—	—	—
BF80_9044	AD1CHSCLR	31:0	Write clears selected bits in AD1CHS, read yields undefined value							
BF80_9048	AD1CHSSET	31:0	Write sets selected bits in AD1CHS, read yields undefined value							
BF80_904C	AD1CHSINV	31:0	Write inverts selected bits in AD1CHS, read yields undefined value							
BF80_9060	AD1PCFG	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8
		7:0	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
BF80_9064	AD1PCFGCLR	31:0	Write clears selected bits in AD1PCFG, read yields undefined value							
BF80_9068	AD1PCFGSET	31:0	Write sets selected bits in AD1PCFG, read yields undefined value							
BF80_906C	AD1PCFGINV	31:0	Write inverts selected bits in AD1PCFG, read yields undefined value							
BF80_9050	AD1CSSL	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
		7:0	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	r-x	r-x	R/W-0	R/W-0	R/W-0
ON	FRZ	SIDL	—	—	FORM<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	r-x	R/W-0	R/W-0	R/C-0
SSRC<2:0>			CLRASAM	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-16 **Reserved:** Write ‘0’; ignore read

הפעלה

bit 15 **ON:** ADC Operating Mode bit
1 = A/D converter module is operating
0 = A/D converter is off

צורות בהפעלת דיבאגר

bit 14 **FRZ:** Freeze in Debug Exception Mode bit
1 = Freeze operation when CPU enters Debug Exception mode
0 = Continue operation when CPU enters Debug Exception mode
Note: FRZ is writable in Debug Exception mode only. It reads ‘0’ in Normal mode.

הסבר בהמשך

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **Reserved:** Write ‘0’; ignore read

תוצאה

bit 10-8 **FORM<2:0>:** Data Output Format bits
011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
111 = Internal counter ends sampling and starts conversion (auto-convert)
110 = Reserved
101 = Reserved
100 = Reserved
011 = Reserved

הסבר בהמשך

010 = Timer 3 period match ends sampling and starts conversion
001 = Active transition on INT0 pin ends sampling and starts conversion
000 = Clearing SAMP bit ends sampling and starts conversion

SIDL: Stop in Idle Mode bit

1= להפסיק את פעולת המודול כאשר המכשיר
נכנס למצב המתנה
0 = פעולת המשך מודול במצב המתנה

SSRC<2:0>: Conversion Trigger Source Select bits

111- דגימה מסתיים ומתחיל המרה (המרה אוטומטית)

010- TIMER3 שולטת על תהליך הדגימה וקובעה את תחילת המרה

001- INT0 שולטת על תהליך הדגימה וקובעה את תחילת המרה

000 = ניקוי SAMP הדגימה מסתיים ומתחיל המרה

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first A/D converter interrupt is generated)
1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
0 = Normal operation, buffer contents will be overwritten by the next conversion sequence

פסיקות

bit 3 **Reserved:** Write '0'; ignore read

bit 2 **ASAM:** ADC Sample Auto-Start bit

צורת הפעלה

1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit

אפשור דגימה

1 = The ADC SHA is sampling
0 = The ADC sample/hold amplifier is holding
When ASAM = 0, writing '1' to this bit starts sampling.
When SSRC = 000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** A/D Conversion Status bit

דגל BUSY

1 = A/D conversion is done
0 = A/D conversion is not done or has not started
Clearing this bit will not affect any operation in progress.
Note: The DONE bit is not persistent in automatic modes. It is cleared by hardware at the beginning of the next sample.

REGISTER 22-2: AD1CON2: ADC CONTROL REGISTER 2

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit

R/W-0	R/W-0	R/W-0	R/W-0	r-x	R/W-0	r-x	r-x
VCFG<2:0>			OFFCAL	—	CSCNA	—	—
bit 15							bi

R-0	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	—	SMPI<3:0>				BUFM	ALTS
bit 7							bi

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-16 **Reserved:** Write ‘0’; ignore read

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	ADC VR+	ADC VR-
000	AVDD	AVSS
001	External VREF+ pin	AVSS
010	AVDD	External VREF- pin
011	External VREF+ pin	External VREF- pin
1xx	AVDD	AVSS

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode
VINH and VINL of the SHA are connected to VR-
0 = Disable Offset Calibration mode
The inputs to the SHA are controlled by AD1CHS or AD1CSSL

מתח יחוס

bit 11 **Reserved:** Write ‘0’; ignore read

bit 10 **CSCNA:** Scan Input Selections for CH0+ SHA Input for MUX A Input Multiplexer Setting bit

1 = Scan inputs
0 = Do not scan inputs

סריקה של הכניסות

bit 9-8 **Reserved:** Write ‘0’; ignore read

bit 7 **BUFS:** Buffer Fill Status bit

רגיסטר תוצאה

Only valid when BUFM = 1 (ADRES split into 2 x 8-word buffers).
1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Reserved:** Write ‘0’; ignore read

REGISTER 22-2: AD1CON2: ADC CONTROL REGISTER 2 (CONTINUED)

פסיקות

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
. . . . .
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF(7...0), ADC1BUF(15...8)
0 = Buffer configured as one 16-word buffer ADC1BUF(15...0.)

תוצאה

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses MUX A input multiplexer settings for first sample, then alternates between MUX B and MUX A input multiplexer settings for all subsequent samples
0 = Always use MUX A input multiplexer settings

שימוש ב-MUX

REGISTER 22-3: AD1CON3: ADC CONTROL REGISTER 3

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit

R/W-0	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC<4:0>				
bit 15							bi

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS<7:0>							
bit 7							bi

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-16 **Reserved:** Write ‘0’; ignore read

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = ADC internal RC clock
0 = Clock derived from Peripheral Bus Clock (PBClock)

bit 14-13 **Reserved:** Write ‘0’; ignore read

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
.....
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits
11111111 = TPB • (ADCS<7:0> + 1) • 2 = 512 • TPB = TAD
.....
00000001 = TPB • (ADCS<7:0> + 1) • 2 = 4 • TPB = TAD
00000000 = TPB • (ADCS<7:0> + 1) • 2 = 2 • TPB = TAD

קצב המרה

REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

R/W-0	r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—	—	CH0SB<3:0>			
bit 31							bit 24

R/W-0	r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	—	—	CH0SA<3:0>			
bit 23							bit 16

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 15							bit 8

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31 **CH0NB:** Negative Input Select for MUX B bit
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VR-

bit 30-28 **Reserved:** Write ‘0’; ignore read

bit 27-24 **CH0SB<3:0>:** Positive Input Select for MUX B bits
1111 = Channel 0 positive input is AN15
1110 = Channel 0 positive input is AN14
1101 = Channel 0 positive input is AN13
. . . . . .
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select for MUX A Multiplexer Setting bit(2)
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VR-

bit 22-20 **Reserved:** Write ‘0’; ignore read

bit 19-16 **CH0SA<3:0>:** Positive Input Select for MUX A Multiplexer Setting bits
1111 = Channel 0 positive input is AN15
1110 = Channel 0 positive input is AN14
1101 = Channel 0 positive input is AN13
. . . . . .
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0

bit 15-0 **Reserved:** Write ‘0’; ignore read

REGISTER 22-5: AD1PCFG: ADC PORT CONFIGURATION REGISTER

r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
—	—	—	—	—	—	—	—
bit 31							bit 24

r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: ('0', '1', x = Unknown)		

bit 31-16 **Reserved:** Reserved for future use, maintain as '0'

bit 15-0 PCFG<15:0>: Analog Input Pin Configuration Control bits

1 = Analog input pin in Digital mode, port read input enabled, ADC input multiplexer input for this analog input connected to AVss

0 = Analog input pin in Analog mode, digital port read will return as a '1' without regard to the voltage on the pin, ADC samples pin voltage

REGISTER 22-6: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: ('0', '1', x = Unknown)		

bit 31-16 **Reserved:** Write '0'

bit 15-0 **CSSL<15:0>:** ADC Input Pin Scan Selection bits
1 = Select ANx for input scan
0 = Skip ANx for input scan

TABLE 22-3: PINS ASSOCIATED WITH THE ADC MODULE

Pin Name	Module Control	Controlling Bit Field	Pin Type	Buffer Type	TRIS	Description
AN0	ON	AD1PCFG<0>	A	—	Input	Analog Input
AN1	ON	AD1PCFG<1>	A	—	Input	Analog Input
AN2	ON	AD1PCFG<2>	A	—	Input	Analog Input
AN3	ON	AD1PCFG<3>	A	—	Input	Analog Input
AN4	ON	AD1PCFG<4>	A	—	Input	Analog Input
AN5	ON	AD1PCFG<5>	A	—	Input	Analog Input
AN6	ON	AD1PCFG<6>	A	—	Input	Analog Input
AN7	ON	AD1PCFG<7>	A	—	Input	Analog Input
AN8	ON	AD1PCFG<8>	A	—	Input	Analog Input
AN9	ON	AD1PCFG<9>	A	—	Input	Analog Input
AN10	ON	AD1PCFG<10>	A	—	Input	Analog Input
AN11	ON	AD1PCFG<11>	A	—	Input	Analog Input
AN12	ON	AD1PCFG<12>	A	—	Input	Analog Input
AN13	ON	AD1PCFG<13>	A	—	Input	Analog Input
AN14	ON	AD1PCFG<14>	A	—	Input	Analog Input
AN15	ON	AD1PCFG<15>	A	—	Input	Analog Input
VREF+	ON	AD1CON2<15:13>	P	—	—	Positive Voltage Reference
VREF-	ON	AD1CON2<15:13>	P	—	—	Negative Voltage Reference

Legend: ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
A = Analog
P = Power

If the user wants to use the audio out module without the AUDIO library, they must implement their own audio functionality.

18 Microphone

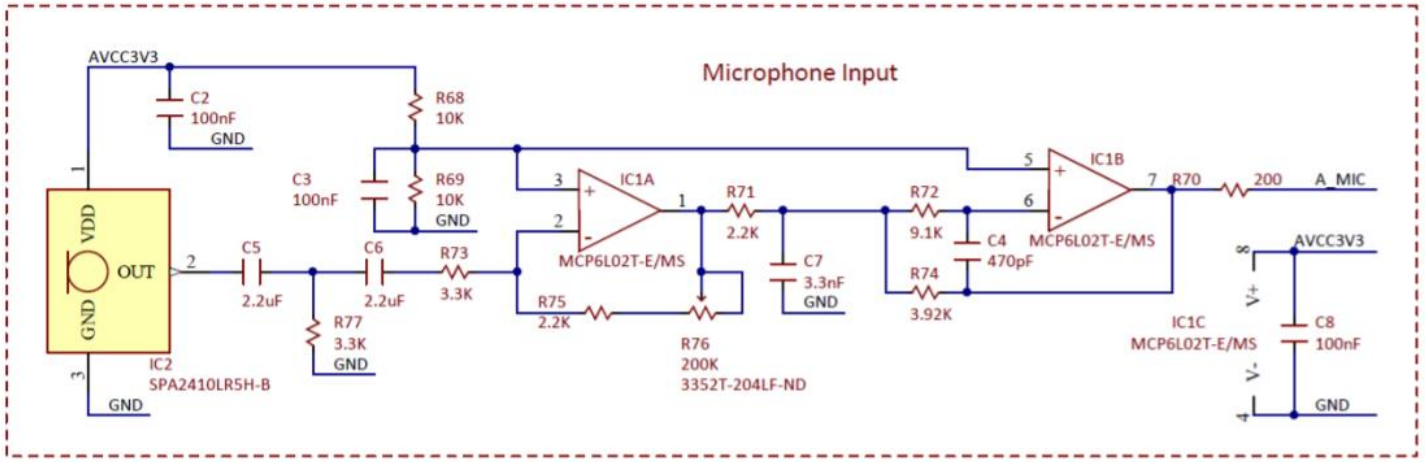


Figure 18.1. Microphone schematic diagram.

the PIC32 documentation.

The microphone on the Basys MX3 also features adjustable gain that is controlled using a thumbwheel potentiometer labeled MIC VOLUME. This dial directly controls the gain of the A_MIC signal going into the PIC32.

18.1 Connectivity

Table 18.1 below shows the details about the A_MIC signal connecting the microphone module to the PIC32.

Name	PIC32 pin	SPA2410LR5H-B pin
A_MIC	AN4/C1INB/RB4	OUT

Table 18.1. Microphone connectivity.

The A_MIC pin will be used as analog input pin:

- The corresponding TRIS bit must be set to 1:
  ```
  TRISBbits.TRISB4 = 1;
  ```
- The corresponding ANSEL bit should be set to 1:
  ```
  ANSELBbits.ANSB4 = 1;
  ```

implement their own ADC functionality.

19 Analog Input Control

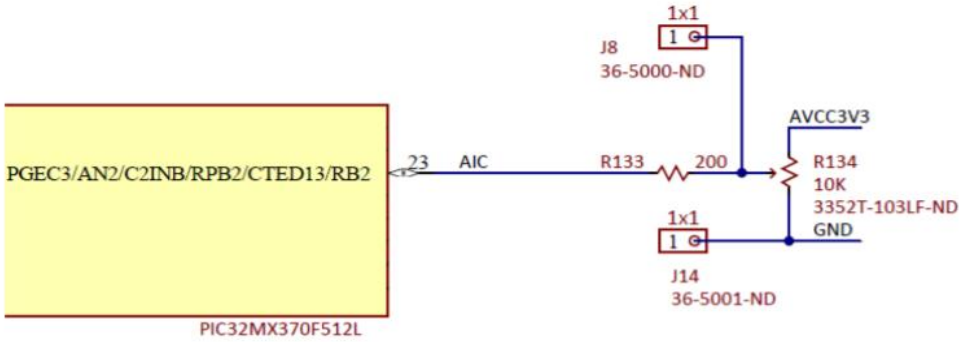


Figure 19.1. Analog input control schematic diagram.

The Basys MX3 provides a basic analog input module. This module exposes an analog input signal called AIC to the PIC32. The user can provide an analog value between 0 and 3.3V using a thumbwheel potentiometer labeled ANALOG INPUT CONTROL.

A pair of wire loops on the Basys MX3, labeled AIC and GND (J8 and J14 on the schematics), can be used to

The AIC analog signal must be sampled using the PIC32's ADC functionality to get a digital value. The PIC32 provides 10-bit data ADC sampling. Read more on the PIC32's ADC functionality in the Analog-To-Digital Converter (ADC) section of the PIC32 documentation.

19.1 Connectivity

Table 19.1 shows the details about the AIC signal connecting the analog input module to the PIC32.

Name	PIC32 pin
AIC	PGEC3/AN2/C2INB/RPB2/CTED13/RB2

Figure 19.1. Analog input control connectivity.

The AIC pin will be used as an analog input pin:

- The corresponding TRIS bit must be set to 1:

```
TRISBbits.TRISB2 = 1;
```

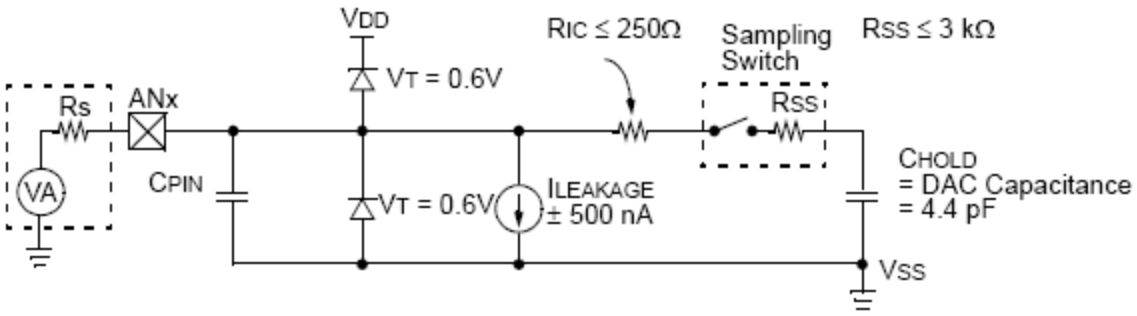
- The corresponding ANSEL bit should be set to 1:

```
ANSELBbits.ANSB2 = 1;
```

```
/*
 * File:   adc.c
 * Author: MenachemE
 *
 * Created on July 13, 2019, 4:41 PM
 */

#include <stdio.h>
#include <stdlib.h>
#include <xc.h>
#pragma config JTAGEN = OFF
#pragma config FWDTEN = OFF
#pragma config FNOSC =  FRCPLL
#pragma config FSOSCEN =OFF
#pragma config POSCMOD =EC
#pragma config OSCIOFNC =ON
#pragma config FPBDIV =     DIV_1
#pragma config FPLLIDIV =DIV_2
#pragma config FPLLMUL =MUL_20
#pragma config FPLLODIV =DIV_1

void ADC_Init()
{

    AD1CON1 =0;
    AD1CON1bits.SSRC = 7;   // Internal counter ends sampling and starts conversion (auto convert)
    AD1CON1bits.FORM = 0;   // Integer 16-bit
                    // Setup for manual sampling
    AD1CSSL  =0;
    AD1CON3 =0x0002;     // ADC Conversion Clock Select bits: TAD = 6 TPB
    AD1CON2 =0;
    AD1CON2bits.VCFG = 0;   // Voltage Reference Configuration bits: VREFH = AVDD and VREFL = AVSS
                    // Turn on ADC
    AD1CON1bits.ON = 1;
}
```

```
/* ************************************************************************** */
/***                ADC_AnalogRead
**
**                Parameters:
**                                unsigned char analogPIN - the number of the analog pin that must be read
**
**                Return Value:
**                                - the 16 LSB bits contain the result of analog to digital conversion of the analog value of the specified pin
**
**                Description:
**                                This function returns the digital value corresponding to the analog pin,
**     as the result of analog to digital conversion performed by the ADC module.
**
*/
unsigned int ADC_AnalogRead(unsigned char analogPIN)
{
   int adc_val = 0;

   IEC0bits.T2IE = 0;
   AD1CHS = analogPIN << 16;       // AD1CHS<16:19> controls which analog pin goes to the ADC

   AD1CON1bits.SAMP = 1;           // Begin sampling
   while( AD1CON1bits.SAMP );      // wait until acquisition is done
   while( ! AD1CON1bits.DONE );    // wait until conversion is done

   adc_val = ADC1BUF0;
   IEC0bits.T2IE = 1;
   return adc_val;
}


void main(void)
{    int x;
     TRISA &= 0xff00;
     TRISBbits.TRISB2 = 1;
     ANSELBbits.ANSB2 = 1;
     ADC_Init();
     while(1)
     {
       x= ADC_AnalogRead(2);//IN analog RB2
        PORTA=x/4;

     }
}
```

FIGURE 22-6: 10-BIT A/D CONVERTER ANALOG INPUT MODEL



Note: CPIN value depends on device package and is not tested. Effect of CPIN negligible if Rs ≤ 5 kΩ.

Legend

CPIN = input capacitance

VT = threshold voltage

RSS = sampling switch resistance

RIC = interconnect resistance

RS = source resistance

CHOLD = sample/hold capacitance (from DAC)

ILEAKAGE = leakage current at the pin due to various junctions

a/d

»end