AFEKA המכללה האקדמית להנדסה בתל-אביב TEL-AVIV ACADEMIC COLLEGE OF ENGINEERING אפקה

הנדסת תוכנה

Software Engineering

מערכות משובצות מחשב (קורס מס' 10110_)

הרצאה מספר 6 ב – הפעלת מערכת פסיקות

PIC32

בקורס מערכות משובצות מחשב

כתב: ד"ר מנחם אפשטיין

מערכות זמן אמת

Interrupt - פסיקות

Real Time – Embedded System

מהי פסיקה (Interrupt) ?

- פסיקה הינה אות אסינכרוני המתקבל מתוכנה או חומרה, ומאפשר שינוי בביצוע סדר התוכנית ללא בקרה מותנית.

- ביצוע הפסיקה גורם ליציאה לתוכנית משנה, ובסיום השגרה התוכנית חוזרת לאותה הנקודה שממה יצאה לטיפול בפסיקה.

- פסיקות משמשות כאמצעי תקשורת בין תהליכים במחשב ונמצאות בשימוש נרחב במחשבים הפועלים בריבוי משימות, ובפרט במערכות בזמן אמת.

כיצד פועלת פסיקה ?

- ברגע בקשת פסיקה, משתנה דגל הפסיקה הספציפית מרמה לוגית "0" לרמה לוגית "1", ונשלחת בקשת פסיקה הכוללת את עדיפות הפסיקה לבדיקה במעבד.

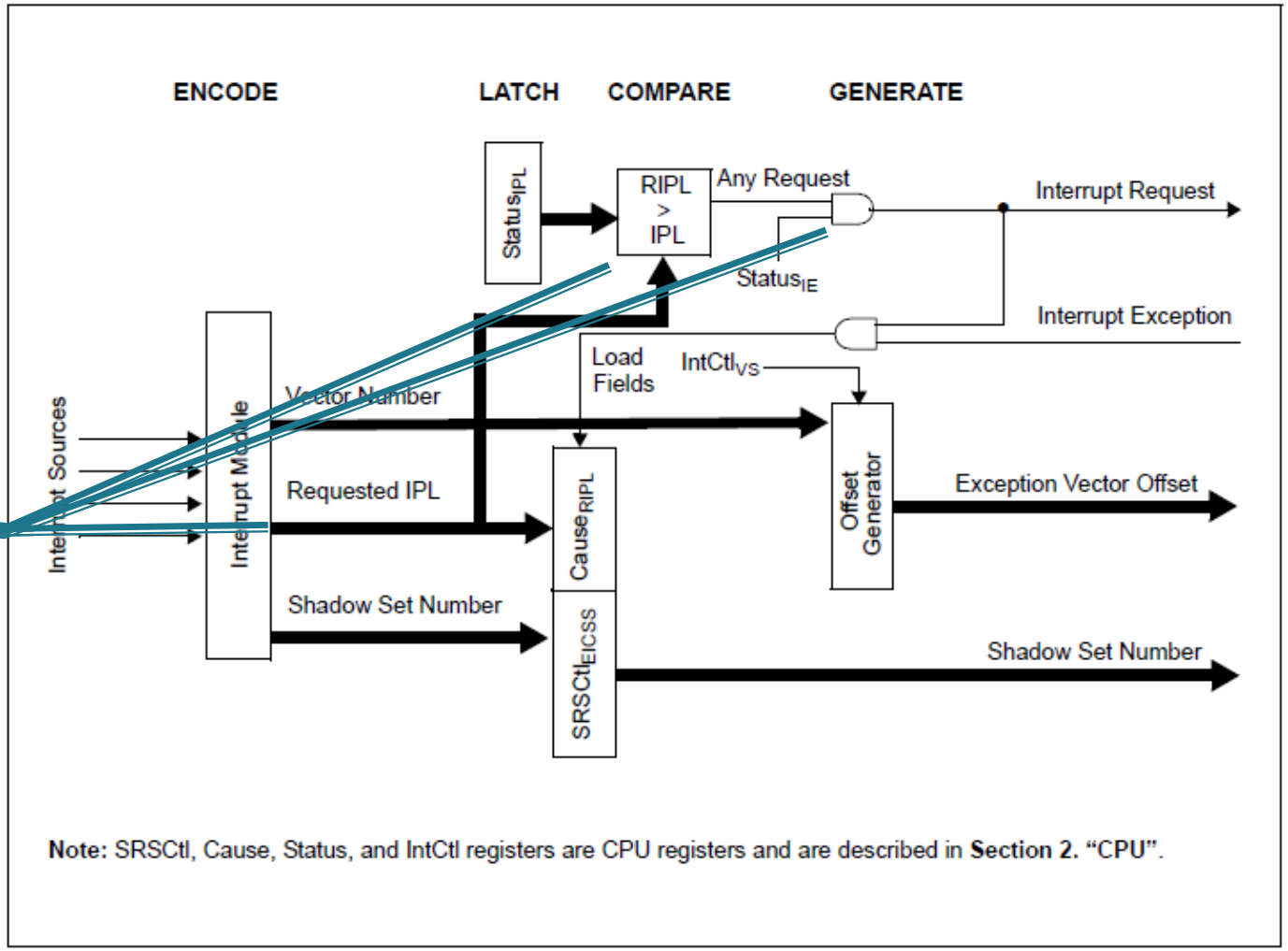
- המעבד מבצע בדיקת עדיפויות ומחליט על ביצוע הפסיקה בעלת העדיפות הגבוהה ביותר, ובמקביל להחלטה, מחושבת כתובת תוכנית הפסיקה שנקבעה.

- לאחר ההחלטה נעצר באקראי רצף התוכנית המקורית והמעבד פונה לטיפול בתוכנית המשנה של הפסיקה, בסיום תוכנית המשנה חוזר לאותה הנקודה שממנה יצא בתוכנית המקורית.

מנגנון הפסיקות ב PIC32

StatusIE=1
אפשור פסיקות
והמשך טיפול בפסיקה
בעלת העדיפות
הגבוהה ביותר.

FIGURE 8-2: INTERRUPT PROCESS



Note: SRSCtl, Cause, Status, and IntCtl registers are CPU registers and are described in **Section 2. "CPU"**.

Control Registers

- INTCON: Interrupt Control Register
- INTSTAT: Interrupt Status Register
- IPTMR: Interrupt Proximity Timer Register
- IFS0, IFS1: Interrupt Flag Status Registers
- IEC0, IEC1: Interrupt Enable Control Registers
- IPC0 – IPC11: Interrupt Priority Control Registers

IPC0-11:
רגיסטרים הקובעים את עדיפות הפסיקות (1-7)
7 - פסיקה בעדיפות הגבוהה ביותר.
1 - פסיקה בעדיפות הנמוכה ביותר.
0 - פסיקה לא פעילה.
וקביעת תת עדיפות (0-3).

REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	R/W-0
—	—	—	—	—	—	—	SS0
bit 23							bit 16

r-x	R/W-0	r-x	R/W-0	r-x	R/W-0	R/W-0	R/W-0
—	FRZ	—	MVEC	—	TPC<2:0>		
bit 15							bit 8

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP
bit 7							bit 0

bit 31-17 **Reserved:** Write '0'; ignore read

bit 16 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow register set
0 = Single vector is not presented with a shadow register set

bit 15 **Reserved:** Write '0'; ignore read

bit 14 **FRZ:** Freeze in Debug Exception Mode bit
1 = Freeze operation when CPU is in Debug Exception mode
0 = Continue operation even when CPU is in Debug Exception mode

Note: FRZ is writable in Debug Exception mode only, it is forced to '0' in normal mode.

bit 13 **Reserved:** Write '0'; ignore read

bit 12 **MVEC:** Multi-Vector Configuration bit
1 = Interrupt controller configured for Multi-Vectored mode
0 = Interrupt controller configured for Single Vectored mode

bit 11 **Reserved:** Write '0'; ignore read

bit 10-8 **TPC<2:0>:** Temporal Proximity Control bits
111 = Interrupt of group priority 7 or lower starts the IP timer
110 = Interrupt of group priority 6 or lower starts the IP timer
101 = Interrupt of group priority 5 or lower starts the IP timer
100 = Interrupt of group priority 4 or lower starts the IP timer
011 = Interrupt of group priority 3 or lower starts the IP timer
010 = Interrupt of group priority 2 or lower starts the IP timer
001 = Interrupt of group priority 1 starts the IP timer
000 = Disables proximity timer

bit 7-5 **Reserved:** Write '0'; ignore read

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

Bits 4–0: Edge P.
קביעת אופן פעולה
עבור קלט חיצוני.
סוג הפולס-עליה או ירדה

REGISTER 8-2: INTSTAT: INTERRUPT STATUS REGISTER

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 31							bit 24

r-x	r-x	r-x	r-x	r-x	r-x	r-x	r-x
—	—	—	—	—	—	—	—
bit 23							bit 16

r-x	r-x	r-x	r-x	r-x	R-0	R-0	R-0
—	—	—	—	—	RIPL<2:0>		
bit 15							bit 8

r-x	r-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	VEC<5:0>					
bit 7							bit 0

bit 31-11 **Reserved:** Write '0'; ignore read

bit 10-8 **RIPL<2:0>:** Requested Priority Level bits

000 – 111 = The priority level of the latest interrupt presented to the CPU

Note: This value should only be used when the interrupt controller is configured for Single Vector mode.

bit 5-0 **VEC:** Interrupt Vector bits

00000 – 11111 = The interrupt vector that is presented to the CPU

Note: This value should only be used when the interrupt controller is configured for Single Vector mode.

Bit 10-8: VEC
אפשור להפסקת פסיקה (בזמן תהליך פסיקה)

REGISTER 8-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IPTMR<31:24>							
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IPTMR<23:16>							
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IPTMR<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IPTMR<7:0>							
bit 7							bit 0

IPTMR bit 31-0:
ערך הטעינה של טיימר ניהול פסיקה.
IP Timer

bit 31-0 **IPTMR:** Interrupt Proximity Timer Reload bits
Used by the interrupt proximity timer as a reload value when the interrupt proximity timer is triggered by an interrupt event.

רגיסטרי דגלי הפסיקות:

REGISTER 8-4: IFS0: INTERRUPT FLAG STATUS REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
I2C1MIF	I2CSIF	I2CBIF	U1TXIF	U1RXIF	U1EIF	SPI1RXIF	SPI1TXIF	bit 13
bit 31							bit 24	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
SPI1EIF	OC5IF	IC5IF	T5IF	INT4IF	OC4IF	IC4IF	T4IF	bit 12
bit 23							bit 16	bit 11

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
INT3IF	OC3IF	IC3IF	T3IF	INT2IF	OC2IF	IC2IF	T2IF	bit 10
bit 15							bit 8	bit 9

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
INT1IF	OC1IF	IC2IF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	bit 8
bit 7							bit 0	bit 7

bit 31 **I2C1MIF:** I2C1 Master Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 30 **I2CSIF:** I2C1 Slave Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 29 **I2CBIF:** I2C1 Bus Collision Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 28 **U1TXIF:** UART1 Transmitter Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 27 **U1RXIF:** UART1 Receiver Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 26 **U1EIF:** UART1 Error Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 25 **SPI1RXIF:** SPI1 Receive Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 24 **SPI1TXIF:** SPI1 Transmitter Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 23 **SPI1EIF:** SPI1 Error Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 22 **OC5IF:** Output Compare 5 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 21 **IC5IF:** Input Compare 5 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 20 **T5IF:** Timer5 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 19 **INT4IF:** External Interrupt 4 Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 18 **OC4IF:** Output Compare 4 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 17 **IC4IF:** Input Compare 4 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 16 **T4IF:** Timer4 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 15 **INT3IF:** External Interrupt 3 Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 14 **OC3IF:** Output Compare 3 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

IC3IF: Input Compare 3 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

T3IF: Timer3 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

INT2IF: External Interrupt 2 Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

OC2IF: Output Compare 2 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

IC2IF: Input Compare 2 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

T2IF: Timer2 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

INT1IF: External Interrupt 1 Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

OC1IF: Output Compare 1 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

IC1IF: Input Compare 1 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

T1IF: Timer1 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

INT0IF: External Interrupt 0 Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

CS1IF: Core Software Interrupt 1 Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

CS0IF: Core Software Interrupt 0 Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

CTIF: Core Timer Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

המשך רגיסטרי דגלי הפסיקות:

REGISTER 8-5: IFS1: INTERRUPT FLAG STATUS REGISTER 1

r-x	r-x	r-x	r-x	r-x	r-x	R/W-0	R/W-0
—	—	—	—	—	—	USBIF	FCEIF
bit 31							bit 24

r-x	r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RTCCIF	FSCMIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPI2RXIF	SPI2TXIF	SPI2EIF	CMP2IF	CMP1IF	PMPIF	AD1IF	CNIF
bit 7							bit 0

bit 31-26 **Reserved:** Write '0'; ignore read

bit 25 **USBIF:** USB Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 24 **FCEIF:** Flash Control Event Interrupt Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 23-20 **Reserved:** Write '0'; ignore read

bit 19 **DMA3IF:** DMA3 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 18 **DMA2IF:** DMA2 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 17 **DMA1IF:** DMA1 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 16 **DMA0IF:** DMA0 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 15 **RTCCIF:** Real Time Clock Interrupt Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 14 **FSCMIF:** Fail-Safe Clock Monitor Interrupt Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 13 **I2C2MIF:** I2C2 Master Interrupt Request bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 12 **I2C2SIF:** I2C2 Slave Interrupt Request bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 11 **I2C2BIF:** I2C2 Bus Collision Interrupt Request bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 10 **U2TXIF:** UART2 Transmitter Interrupt Request bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 9 **U2RXIF:** UART2 Receiver Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 8 **U2EIF:** UART2 Error Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 7 **SPI2RXIF:** SPI2 Receiver Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 6 **SPI2TXIF:** SPI2 Transmitter Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 5 **SPI2EIF:** SPI2 Error Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 4 **CMP2IF:** Comparator 2 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 3 **CMP1IF:** Comparator 1 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 2 **PMPIF:** Parallel Master Port Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 1 **AD1IF:** Analog-to-Digital 1 Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

bit 0 **CNIF:** Input Change Interrupt Request Flag bit
1 = Interrupt request has occurred
0 = No interrupt request has a occurred

רגיסטרי אפשור הפסיקות:

REGISTER 8-6: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1RXIE	SPI1TXIE
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPI1EIE	OC5IE	IC5IE	T5IE	INT4IE	OC4IE	IC4IE	T4IE
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT3IE	OC3IE	IC3IE	T3IE	INT2IE	OC2IE	IC2IE	T2IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT1IE	OC1IE	IC1IE	T1IE	INT0IE	CS1IE	CS0IE	CTIE
bit 7							bit 0

bit 31 **I2C2MIE:** I2C2 Master Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 30 **I2C1SIE:** I2C1 Slave Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 29 **I2C1BIE:** I2C1 Bus Collision Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 28 **U1TXIE:** UART1 Transmitter Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 27 **U1RXIE:** UART1 Receiver Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 26 **U1EIE:** UART1 Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 25 **SPI1RXIE:** SPI1 Receive Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 24 **SPI1TXIE:** SPI1 Transmitter Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 23 **SPI1EIE:** SPI1 Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 22 **OC5IE:** Output Compare 5 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 21 **IC5IE:** Input Compare 5 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 20 **T5IE:** Timer5 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 19 **INT4IE:** External Interrupt 4 Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **OC4IE:** Output Compare 4 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **IC4IE:** Input Compare 4 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **T4IE:** Timer4 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15 **INT3IE:** External Interrupt 3 Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 14 **OC3IE:** Output Compare 3 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 13 **IC3IE:** Input Compare 3 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 12 **T3IE:** Timer3 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **INT2IE:** External Interrupt 2 Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 10 **OC2IE:** Output Compare 2 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **IC2IE:** Input Compare 2 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 8 **T2IE:** Timer2 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **OC1IE:** Output Compare 1 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **IC1IE:** Input Compare 1 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **T1IE:** Timer1 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **INT0IE:** External Interrupt 0 Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **CS1IE:** Core Software Interrupt 1 Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **CS0IE:** Core Software Interrupt 0 Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **CTIE:** Core Timer Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

המשך רגיסטרי אפשור פסיקות:

REGISTER 8-7: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

r-x	r-x	r-x	r-x	r-x	r-x	r-x	R/W-0
—	—	—	—	—	—	USBIE	FCEIE
bit 31							bit 24

r-x	r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RTCCIE	FSCMIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPI2RXIE	SPI2TXIE	SPI2EIE	CMP2IE	CMP1IE	PMPIE	AD1IE	CNIE
bit 7							bit 0

bit 31-26 **Reserved:** Write '0'; ignore read

bit 25 **USBIE:** USB Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 24 **FCEIE:** Flash Control Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 23-20 **Reserved:** Write '0'; ignore read

bit 19 **DMA3IE:** DMA3 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **DMA2IE:** DMA2 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **DMA1IE:** DMA1 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **DMA0IE:** DMA0 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15 **RTCCIE:** Real-Time Clock Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 14 **FSCMIE:** Fail-Safe Clock Monitor Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 13 **I2C2MIE:** I2C2 Master Interrupt Request bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 12 **I2C2SIE:** I2C2 Slave Interrupt Request bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **I2C2BIE:** I2C2 Bus Collision Interrupt Request bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 10 **U2TXIE:** UART2 Transmitter Interrupt Request bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **U2RXIE:** UART2 Receiver Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 8 **U2EIE:** UART2 Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **SPI2RXIE:** SPI2 Receiver Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **SPI2TXIE:** SPI2 Transmitter Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **SPI2EIE:** SPI2 Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **CMP2IE:** Comparator 2 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **CMP1IE:** Comparator 1 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **PMPIE:** Parallel Master Port Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **AD1IE:** Analog-to-Digital 1 Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **CNIE:** Input Change Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

רגיסטרי עדיפות הפסיקות:

REGISTER 8-8: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT0IP<2:0>			INT0IS<1:0>	
bit 31							bit 24

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CS1IP<2:0>			CS1IS<1:0>	
bit 23							bit 16

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CS0IP<2:0>			CS0IS<1:0>	
bit 15							bit 8

r-x	r-x	r-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CTIP<2:0>			CTIS<1:0>	
bit 7							bit 0

bit 31-29 **Reserved:** Write '0'; ignore read

bit 28-26 **INT0IP<2:0>:** External Interrupt 0 Priority bits
111 = Interrupt priority is 7
110 = Interrupt priority is 6
101 = Interrupt priority is 5
100 = Interrupt priority is 4
011 = Interrupt priority is 3
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 25-24 **INT0IS<1:0>:** External Interrupt 0 Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 23-21 **Reserved:** Write '0'; ignore read

bit 20-18 **CS1IP<2:0>:** Core Software 1 Interrupt Priority bits
111 = Interrupt priority is 7
110 = Interrupt priority is 6
101 = Interrupt priority is 5
100 = Interrupt priority is 4
011 = Interrupt priority is 3
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 17-16 **CS1IS<1:0>:** Core Software 1 Interrupt subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 15-13 **Reserved:** Write '0'; ignore read

bit 12-10 **CS0IP<2:0>:** Core Software 0 Interrupt Priority bits
111 = Interrupt priority is 7
110 = Interrupt priority is 6
101 = Interrupt priority is 5
100 = Interrupt priority is 4
011 = Interrupt priority is 3
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 9-8 **CS0IS<1:0>:** Core Software 0 Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 7-5 **Reserved:** Write '0'; ignore read

bit 4-2 **CTIP<2:0>:** Core Timer Interrupt Priority bits
111 = Interrupt priority is 7
110 = Interrupt priority is 6
101 = Interrupt priority is 5
100 = Interrupt priority is 4
011 = Interrupt priority is 3
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **CTIS<1:0>:** Core Timer Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

רגיסטר זה קובע באותו האופן את מצב הפסיקות:
CS1IP – Core Software 1
CS0IP– Core Software 0
CTIP – Core Timer

המשך רגיסטרי עדיפות הפסיקות:

- סיכום רגיסטרי עדיפות הפסיקות:

- IPC0 – External Interrupt 0
  Core Software 1 Interrupt
  Core Software 0 Interrupt
  Core Timer Interrupt
- IPC1 – External Interrupt 1
  Output Compare 1 Interrupt
  Input Compare 1 Interrupt
  Timer1 Interrupt

המשך רגיסטרי עדיפות הפסיקות:

- IPC2 – External Interrupt 2
  Output Compare 2 Interrupt
  Input Compare 2 Interrupt
  Timer2 Interrupt
- IPC3 – External Interrupt 3
  Output Compare 3
  Input Compare 3
  Timer3 Interrupt

המשך רגיסטרי עדיפות הפסיקות:

- IPC4 – External Interrupt 4
  Output Compare 4
  Input Compare 4
  Timer4 Interrupt
- IPC5 – SPI1 Interrupt
  Output Compare 5
  Input Compare 5
  Timer5 Interrupt

המשך רגיסטרי עדיפות הפסיקות:

- IPC6 – Analog-to-Digital 1
  Input Change Interrupt
  I2C1 Interrupt
  UART1 Interrupt
- IPC7 – SPI2 Interrupt
  Compare 2 Interrupt
  Compare 1 Interrupt
  Parallel Master Port Interrupt

המשך רגיסטרי עדיפות הפסיקות:

- IPC8 – Real-Time Clock Interrupt
  Fail-Safe Clock Monitor Interrupt
  I2C2 Interrupt
  UART2 Interrupt
- IPC9 – DMA3 Interrupt
  DMA2 Interrupt
  DMA1 Interrupt
  DMA0 Interrupt

המשך רגיסטרי עדיפות הפסיקות:

- IPC10 – Empty Register

- IPC11 – USB Interrupt
  Flash Control Event Interrupt

סדר פסיקות ומספרי ווקטורים:

TABLE 8-2: INTERRUPT IRQ AND VECTOR LOCATION

Interrupt Source	IRQ(1)	Vector Number
Highest Natural Order Priority		
CT – Core Timer Interrupt	0	0
CS0 – Core Software Interrupt 0	1	1
CS1 – Core Software Interrupt 1	2	2
INT0 – External Interrupt 0	3	3
T1 – Timer1	4	4
IC1 – Input Capture 1	5	5
OC1 – Output Compare 1	6	6
INT1 – External Interrupt 1	7	7
T2 – Timer2	8	8
IC2 – Input Capture 2	9	9
OC2 – Output Compare 2	10	10
INT2 – External Interrupt 2	11	11
T3 – Timer3	12	12
IC3 – Input Capture 3	13	13
OC3 – Output Compare 3	14	14
INT3 – External Interrupt 3	15	15
T4 – Timer4	16	16
IC4 – Input Capture 4	17	17
OC4 – Output Compare 4	18	18
INT4 – External Interrupt 4	19	19
T5 – Timer5	20	20
IC5 – Input Capture 5	21	21
OC5 – Output Compare 5	22	22
SPI1E – SPI1 Fault	23	23
SPI1TX – SPI1 Transfer Done	24	23
SPI1RX – SPI1 Receive Done	25	23
U1E – UART1 Error	26	24
U1RX – UART1 Receiver	27	24
U1TX – UART1 Transmitter	28	24

Interrupt Source	IRQ(1)	Vector Number
I2C1B – I2C1 Bus Collision Event	29	25
I2C1S – I2C1 Slave Event	30	25
I2C1M – I2C1 Master Event	31	25
CN – Input Change Interrupt	32	26
AD1 – ADC1 convert done	33	27
PMP – Parallel Master Port	34	28
CMP1 – Comparator Interrupt	35	29
CMP2 – Comparator Interrupt	36	30
SPI2E – SPI2 Fault	37	31
SPI2TX – SPI2 Transfer Done	38	31
SPI2RX – SPI2 Receive Done	39	31
U2E – UART2 Error	40	32
U2RX – UART2 Receiver	41	32
U2TX – UART2 Transmitter	42	32
I2C2B – I2C2 Bus Collision Event	43	33
I2C2S – I2C2 Slave Event	44	33
I2C2M – I2C2 Master Event	45	33
FSCM – Fail-Safe Clock Monitor	46	34
RTCC – Real-Time Clock	47	35
DMA0 – DMA Channel 0	48	36
DMA1 – DMA Channel 1	49	37
DMA2 – DMA Channel 2	50	38
DMA3 – DMA Channel 3	51	39
FCE – Flash Control Event	56	44
USB	57	45

יש לשים לב שמספר פסיקות מגיעות על אותו ווקטור פסיקה, ולכן ישנו צורך במתן עדיפות ותת עדיפות לפסיקות השונות.

```
/*
 * File:  INTERRUPT_timer4.c
 * Author: MenachemE
 *
 * Created on July 17, 2019, 2:20 PM
 */
//#include <xc.h>
#pragma config JTAGEN = OFF
#pragma config FWDTEN = OFF
#pragma config FNOSC =          FRCPLL
#pragma config FSOSCEN =        OFF
#pragma config POSCMOD =        EC
#pragma config OSCIOFNC =       ON
#pragma config FPBDIV =     DIV_1
#pragma config FPLLIDIV =       DIV_2
#pragma config FPLLMUL =        MUL_20
#pragma config FPLLODIV =       DIV_1
#include "timer.h"
 #include <xc.h>
#include <sys/attribs.h>
#include <string.h>
#include <stdlib.h>

 void __ISR(_TIMER_4_VECTOR, ipl2auto) Timer4SR(void);

       void __ISR(_TIMER_4_VECTOR, ipl2) Timer4SR(void)
       {

   PORTA ++;
   IFS0bits.T4IF = 0;
       }
```

```
 void main()
   { int j;
       TRISA &= 0xff00;
       PR4 = 0xffff;                    //          set period register, generates one interrupt every 1 ms
       TMR4 = 0;                        //          initialize count to 0

       T4CONbits.TCKPS0 = 1;            //          1:256 prescale value
       T4CONbits.TCKPS1 = 1;
       T4CONbits.TCKPS2 = 1;
       T4CONbits.TGATE = 0;             //          not gated input (the default)
       T4CONbits.TCS = 0;               //          PCBLK input (the default)
       T4CONbits.ON = 1;                //          turn on Timer1
       IPC4bits.T4IP = 2;               //          priority
       IPC4bits.T4IS = 0;               //          subpriority
       IFS0bits.T4IF = 0;               //          clear interrupt flag
       IEC0bits.T4IE = 1;
       INTCONbits.MVEC=1;//vector interrupt
IPTMR=0;//INTERRUPT PROXIMITY TIMER REGISTER
 asm("ei");//on interrupt

while(1);
   }
```

הפעלת פסיקות

TIMER 16bit-32bit

```
#pragma config JTAGEN = OFF
#pragma config FWDTEN = OFF
#pragma config FNOSC =          FRCPLL
#pragma config FSOSCEN =        OFF
#pragma config POSCMOD =        EC
#pragma config OSCIOFNC =       ON
#pragma config FPBDIV =     DIV_1
#pragma config FPLLIDIV =       DIV_2
#pragma config FPLLMUL =        MUL_20
#pragma config FPLLODIV =       DIV_1
//#include "timer.h"
 #include <xc.h>
#include <sys/attribs.h>
#include <string.h>
#include <stdlib.h>

void __ISR(_TIMER_4_VECTOR, ipl7auto) Timer4SR(void);
        void __ISR(_TIMER_4_VECTOR, ipl7) Timer4SR(void)
       {
PORTAbits.RA0^=1;
    IFS0bits.T4IF = 0;
        }
```

```
void __ISR(_TIMER_3_VECTOR, ipl6auto) Timer23SR(void);
        void __ISR(_TIMER_3_VECTOR, ipl6) Timer23SR(void)
       {
PORTAbits.RA1^=1;//sw0
    IFS0bits.T3IF = 0;
        }

 void main()
    { int j;
    TRISA&=0xff00;
        PR4 = 0xffff;                    //          set period register, generates one interrupt every 1 ms
        TMR4 = 0;                        //          initialize count to 0
        T4CONbits.TCKPS0 = 1;                //          1:256 prescale value
        T4CONbits.TCKPS1 = 1;
        T4CONbits.TCKPS2 = 1;
        T4CONbits.TGATE = 0;                //          not gated input (the default)
        T4CONbits.TCS = 0;                //          PCBLK input (the default)
        T4CONbits.ON = 1;                //          turn on Timer1
        IPC4bits.T4IP = 7;                //          priority
        IPC4bits.T4IS = 3;                //          subpriority
        IFS0bits.T4IF = 0;                //          clear interrupt flag
        IEC0bits.T4IE = 1;
```

```
T2CONbits.TGATE=0;
T2CONbits.TCS=0;
T2CONbits.T32=1;//mode 32bit
T2CONbits.TCKPS0=1;//256 חלוקה
T2CONbits.TCKPS1=1;
T2CONbits.TCKPS2=1;
T3CONbits.ON=0;
TMR3=0;//TMRy
TMR2=0;//TMRx
PR2=0Xffff;//PR2x
PR3=0x3;//PR2y
T2CONbits.ON=1;//start timer
IFS0bits.T3IF=0;//
        IPC3bits.T3IP = 6;              //          priority
        IPC3bits.T3IS = 0;              //          subpriority
        IFS0bits.T3IF = 0;              //          clear interrupt flag
        IEC0bits.T3IE = 1;
INTCONbits.MVEC=1;//vector interrupt
IPTMR=0;//INTERRUPT PROXIMITY TIMER REGISTER
 asm("ei");//on interrupt
  while(1);
  }
```

Fin