



1. Description

1.1. Project

| | |
|-----------------|-------------------|
| Project Name | h7-wake-on-lan |
| Board Name | NUCLEO-H745ZI-Q |
| Generated with: | STM32CubeMX 6.6.0 |
| Date | 07/04/2022 |

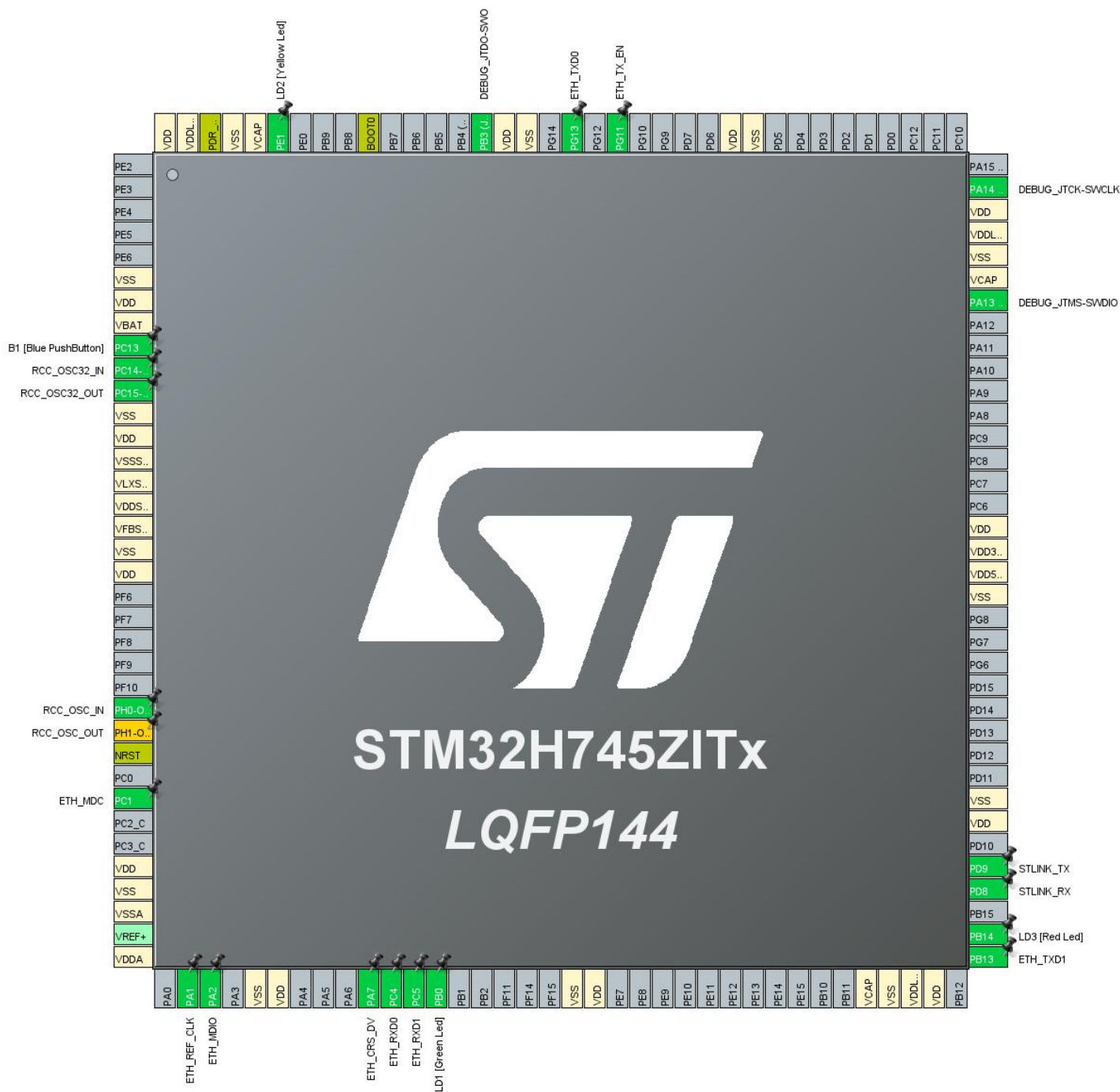
1.2. MCU

| | |
|----------------|---------------|
| MCU Series | STM32H7 |
| MCU Line | STM32H745/755 |
| MCU name | STM32H745ZITx |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

1.3. Core(s) information

| | |
|---------|--------------------------------|
| Core(s) | ARM Cortex-M7 ARM Cortex-M4 |
|---------|--------------------------------|

2. Pinout Configuration



3. Pins Configuration

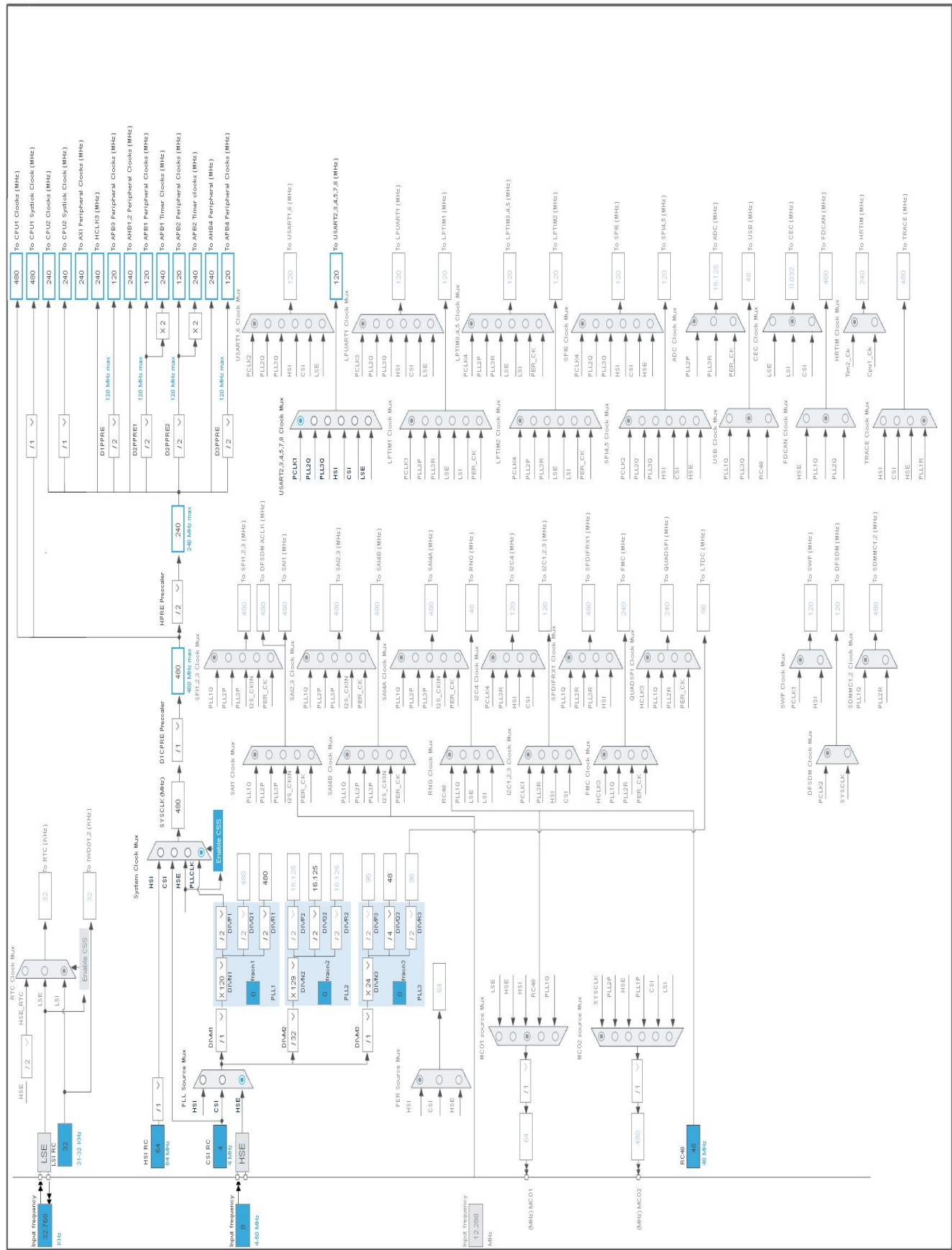
| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|----------------------|
| 6 | VSS | Power | | |
| 7 | VDD | Power | | |
| 8 | VBAT | Power | | |
| 9 | PC13 * | I/O | GPIO_Input | B1 [Blue PushButton] |
| 10 | PC14-OSC32_IN (OSC32_IN) | I/O | RCC_OSC32_IN | |
| 11 | PC15-OSC32_OUT (OSC32_OUT) | I/O | RCC_OSC32_OUT | |
| 12 | VSS | Power | | |
| 13 | VDD | Power | | |
| 14 | VSSSMPS | Power | | |
| 15 | VLXSMPS | Power | | |
| 16 | VDDSMPS | Power | | |
| 17 | VFBSMPS | Power | | |
| 18 | VSS | Power | | |
| 19 | VDD | Power | | |
| 25 | PH0-OSC_IN (PH0) | I/O | RCC_OSC_IN | |
| 26 | PH1-OSC_OUT (PH1) ** | I/O | RCC_OSC_OUT | |
| 27 | NRST | Reset | | |
| 29 | PC1 | I/O | ETH_MDC | |
| 32 | VDD | Power | | |
| 33 | VSS | Power | | |
| 34 | VSSA | Power | | |
| 36 | VDDA | Power | | |
| 38 | PA1 | I/O | ETH_REF_CLK | |
| 39 | PA2 | I/O | ETH_MDIO | |
| 41 | VSS | Power | | |
| 42 | VDD | Power | | |
| 46 | PA7 | I/O | ETH_CRS_DV | |
| 47 | PC4 | I/O | ETH_RXD0 | |
| 48 | PC5 | I/O | ETH_RXD1 | |
| 49 | PB0 * | I/O | GPIO_Output | LD1 [Green Led] |
| 55 | VSS | Power | | |
| 56 | VDD | Power | | |
| 68 | VCAP | Power | | |
| 69 | VSS | Power | | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|------------------|
| 70 | VDDLDO | Power | | |
| 71 | VDD | Power | | |
| 73 | PB13 | I/O | ETH_TXD1 | |
| 74 | PB14 * | I/O | GPIO_Output | LD3 [Red Led] |
| 76 | PD8 | I/O | USART3_TX | STLINK_RX |
| 77 | PD9 | I/O | USART3_RX | STLINK_TX |
| 79 | VDD | Power | | |
| 80 | VSS | Power | | |
| 89 | VSS | Power | | |
| 90 | VDD50_USB | Power | | |
| 91 | VDD33_USB | Power | | |
| 92 | VDD | Power | | |
| 102 | PA13 (JTMS/SWDIO) | I/O | DEBUG_JTMS-SWDIO | |
| 103 | VCAP | Power | | |
| 104 | VSS | Power | | |
| 105 | VDDLDO | Power | | |
| 106 | VDD | Power | | |
| 107 | PA14 (JTCK/SWCLK) | I/O | DEBUG_JTCK-SWCLK | |
| 118 | VSS | Power | | |
| 119 | VDD | Power | | |
| 124 | PG11 | I/O | ETH_TX_EN | |
| 126 | PG13 | I/O | ETH_TXD0 | |
| 128 | VSS | Power | | |
| 129 | VDD | Power | | |
| 130 | PB3 (JTDO/TRACESWO) | I/O | DEBUG_JTDO-SWO | |
| 135 | BOOT0 | Boot | | |
| 139 | PE1 * | I/O | GPIO_Output | LD2 [Yellow Led] |
| 140 | VCAP | Power | | |
| 141 | VSS | Power | | |
| 142 | PDR_ON | Reset | | |
| 143 | VDDLDO | Power | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

| Name | Value |
|-----------------------------------|------------------------------|
| Project Name | h7-wake-on-lan |
| Project Folder | D:\work\tests\h7-wake-on-lan |
| Toolchain / IDE | STM32CubeIDE |
| Firmware Package Name and Version | STM32Cube FW_H7 V1.10.0 |
| Application Structure | Advanced |
| Generate Under Root | Yes |
| Do not generate the main() | No |
| Minimum Heap Size | 0x00 |
| Minimum Stack Size | 0x400 |

5.2. Code Generation Settings

| Name | Value |
|---|---------------------------------------|
| STM32Cube MCU packages and embedded software | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Keep User Code when re-generating | Yes |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |
| Enable Full Assert | No |

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

| Rank | Function Name | Peripheral Instance Name |
|------|---------------------|--------------------------|
| 1 | SystemClock_Config | RCC |
| 2 | MX_GPIO_Init | GPIO |
| 3 | MX_USART3_UART_Init | USART3 |
| 4 | MX_FREERTOS_Init | FREERTOS_M7 |
| 5 | MX_LWIP_Init | LWIP |

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

| Rank | Function Name | Peripheral Instance Name |
|------|---------------|--------------------------|
| 1 | MX_GPIO_Init | GPIO |

6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|-----------|---------------|
| Series | STM32H7 |
| Line | STM32H745/755 |
| MCU | STM32H745ZITx |
| Datasheet | DS12923_Rev1 |

6.2. Parameter Selection

| | |
|-------------|-----|
| Temperature | 25 |
| Vdd | 3.0 |

6.3. Battery Selection

| | |
|-------------------|-------------------|
| Battery | Li-SOCL2(DD36000) |
| Capacity | 36000.0 mAh |
| Self Discharge | 0.08 %/month |
| Nominal Voltage | 3.6 V |
| Max Cont Current | 450.0 mA |
| Max Pulse Current | 1000.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

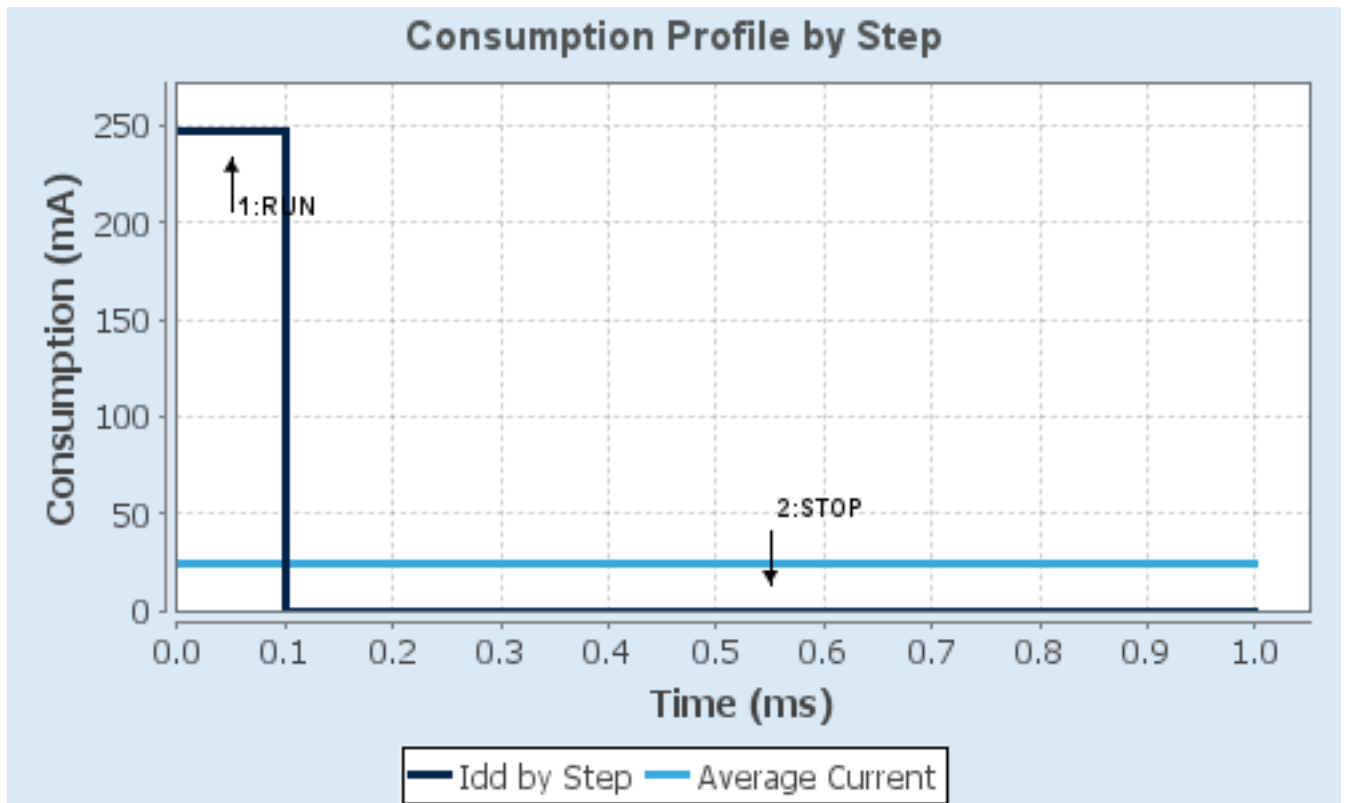
6.4. Sequence

| | | |
|-------------------------------|---------------------------------------|----------------------|
| Step | Step1 | Step2 |
| Mode | RUN | STOP |
| Vdd | 3.0 | 3.0 |
| Voltage Source | Battery | Battery |
| Range | VOS0: Scale0 | SVOS5: System-Scale5 |
| D1 Mode | DRUN/CRUN | DSTANDBY |
| D2 Mode | DRUN/CRUN | DSTANDBY |
| D3 Mode | DRUN | DSTOP |
| Fetch Type | CM7: ITCM/Cache / CM4: FLASH_B/ART | CM7: NA / CM4: NA |
| CM7 Frequency | 480 MHz | 0 Hz |
| Clock Configuration | HSE BYP PLL ALL IPs ON | LSE Flash-ON |
| CM4 Frequency | 240 MHz | 0 Hz |
| Clock Source Frequency | 25 MHz | 0 Hz |
| Peripherals | | |
| Additional Cons. | 0 mA | 0 mA |
| Average Current | 247 mA | 145 μ A |
| Duration | 0.1 ms | 0.9 ms |
| DMIPS | 1027.0 | 0.0 |
| Category | In DS Table | In DS Table |

6.5. Results

| | | | |
|---------------|-------------------------------|-----------------|--------------------|
| Sequence Time | 1 ms | Average Current | 24.83 mA |
| Battery Life | 1 month, 29 days, 21 hours | Average DMIPS | 1027.2001 DMIPS |

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. CORTEX_M7

7.1.1. Parameter Settings:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

Speculation default mode Settings:

| | |
|--------------------------|----------|
| Speculation default mode | Disabled |
|--------------------------|----------|

Cortex Interface Settings:

| | |
|------------|-----------|
| CPU ICache | Enabled * |
| CPU DCache | Enabled * |

Cortex Memory Protection Unit Control Settings:

| | |
|------------------|---|
| MPU Control Mode | Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers * |
|------------------|---|

Cortex Memory Protection Unit Region 0 Settings:

| | |
|-----------------------------|------------------------|
| MPU Region | Enabled * |
| MPU Region Base Address | 0x30044000 * |
| MPU Region Size | 16KB * |
| MPU SubRegion Disable | 0x0 * |
| MPU TEX field level | level 1 * |
| MPU Access Permission | ALL ACCESS PERMITTED * |
| MPU Instruction Access | ENABLE |
| MPU Shareability Permission | ENABLE * |
| MPU Cacheable Permission | DISABLE |
| MPU Bufferable Permission | DISABLE |

Cortex Memory Protection Unit Region 1 Settings:

| | |
|------------|----------|
| MPU Region | Disabled |
|------------|----------|

Cortex Memory Protection Unit Region 2 Settings:

| | |
|------------|----------|
| MPU Region | Disabled |
|------------|----------|

Cortex Memory Protection Unit Region 3 Settings:

| | |
|------------|----------|
| MPU Region | Disabled |
|------------|----------|

Cortex Memory Protection Unit Region 4 Settings:

| | |
|------------|----------|
| MPU Region | Disabled |
|------------|----------|

Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region Disabled

7.2. DEBUG

Debug: Trace Asynchronous Sw

7.2.1. Core(s) Settings:

| | |
|----------------------|------------------------|
| Context(s): | Cortex-M7 Cortex-M4 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | |

7.3. ETH

Mode: RMII

7.3.1. Parameter Settings:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D2 |

General : Ethernet Configuration:

| | |
|-----------------------------|---|
| Warning | The ETH can work only when RAM is pointing at 0x24000000 |
| Note | PHY Driver must be configured from the LwIP 'Platform Settings' top right tab |
| Ethernet MAC Address | 00:80:E1:00:00:00 |
| Tx Descriptor Length | 4 |
| First Tx Descriptor Address | 0x30040060 * |
| Rx Descriptor Length | 4 |
| First Rx Descriptor Address | 0x30040000 * |
| Rx Buffers Length | 1536 |

7.4. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

Core(s) Settings:

| | |
|----------------------|------------------------|
| Context(s): | Cortex-M7 Cortex-M4 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D3 |

Power Parameters:

| | |
|-------------------------------|---------------------------------|
| SupplySource | PWR_DIRECT_SMPS_SUPPLY |
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 0 |

RCC Parameters:

| | |
|--------------------------------|----------|
| TIM Prescaler Selection | Disabled |
| HSE Startup Timeout Value (ms) | 100 |
| LSE Startup Timeout Value (ms) | 5000 |
| CSI Calibration Value | 16 |
| HSI Calibration Value | 32 |

System Parameters:

| | |
|-----------------|-----|
| VDD voltage (V) | 3.3 |
|-----------------|-----|

| | |
|------------------------------|----------------------|
| Flash Latency(WS) | 4 WS (5 CPU cycle) |
| Product revision | rev.Y |
| PLL range Parameters: | |
| PLL1 clock Input range | Between 8 and 16 MHz |
| PLL1 clock Output range | Wide VCO range |

7.5. SYS

Timebase Source: TIM17

7.5.1. Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | |

7.6. SYS_M4

Timebase Source: SysTick

7.6.1. Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M4 |
| Initialized Context: | Cortex-M4 |
| Power Domain: | |

7.7. USART3

Mode: Asynchronous

7.7.1. Parameter Settings:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D2 |

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |

| | |
|-----------------------------|-----------------------------|
| Parity | None |
| Stop Bits | 1 |
| Advanced Parameters: | |
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |
| ClockPrescaler | 1 |
| Fifo Mode | Disable |
| Txfifo Threshold | 1 eighth full configuration |
| Rxfifo Threshold | 1 eighth full configuration |

Advanced Features:

| | |
|-------------------------------|---------|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

7.8. FREERTOS_M7

Interface: CMSIS_V2

7.8.1. Config parameters:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

API:

| | |
|--------------|----------|
| FreeRTOS API | CMSIS v2 |
|--------------|----------|

Versions:

| | |
|--------------------|--------|
| FreeRTOS version | 10.3.1 |
| CMSIS-RTOS version | 2.00 |

MPU/FPU:

| | |
|------------|----------|
| ENABLE_MPU | Disabled |
| ENABLE_FPU | Disabled |

Kernel settings:

| | |
|----------------|---------|
| USE_PREEMPTION | Enabled |
|----------------|---------|

| | |
|-----------------------------------|-----------------|
| CPU_CLOCK_HZ | SystemCoreClock |
| TICK_RATE_HZ | 1000 |
| MAX_PRIORITIES | 56 |
| MINIMAL_STACK_SIZE | 128 |
| MAX_TASK_NAME_LEN | 16 |
| USE_16_BIT_TICKS | Disabled |
| IDLE_SHOULD_YIELD | Enabled |
| USE_MUTEXES | Enabled |
| USE_RECURSIVE_MUTEXES | Enabled |
| USE_COUNTING_SEMAPHORES | Enabled |
| QUEUE_REGISTRY_SIZE | 8 |
| USE_APPLICATION_TASK_TAG | Disabled |
| ENABLE_BACKWARD_COMPATIBILITY | Enabled |
| USE_PORT_OPTIMISED_TASK_SELECTION | Disabled |
| USE_TICKLESS_IDLE | Disabled |
| USE_TASK_NOTIFICATIONS | Enabled |
| RECORD_STACK_HIGH_ADDRESS | Disabled |

Memory management settings:

| | |
|--------------------------|------------------|
| Memory Allocation | Dynamic / Static |
| TOTAL_HEAP_SIZE | 15360 |
| Memory Management scheme | heap_4 |

Hook function related definitions:

| | |
|------------------------------|----------|
| USE_IDLE_HOOK | Disabled |
| USE_TICK_HOOK | Disabled |
| USE_MALLOC_FAILED_HOOK | Disabled |
| USE_DAEMON_TASK_STARTUP_HOOK | Disabled |
| CHECK_FOR_STACK_OVERFLOW | Disabled |

Run time and task stats gathering related definitions:

| | |
|--------------------------------|----------|
| GENERATE_RUN_TIME_STATS | Disabled |
| USE_TRACE_FACILITY | Enabled |
| USE_STATS_FORMATTING_FUNCTIONS | Disabled |

Co-routine related definitions:

| | |
|---------------------------|----------|
| USE_CO_ROUTINES | Disabled |
| MAX_CO_ROUTINE_PRIORITIES | 2 |

Software timer definitions:

| | |
|------------------------|---------|
| USE_TIMERS | Enabled |
| TIMER_TASK_PRIORITY | 2 |
| TIMER_QUEUE_LENGTH | 10 |
| TIMER_TASK_STACK_DEPTH | 256 |

Interrupt nesting behaviour configuration:

| | |
|--|----|
| LIBRARY_LOWEST_INTERRUPT_PRIORITY | 15 |
| LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY | 5 |

Added with 10.2.1 support:

| | |
|----------------------------|----------|
| MESSAGE_BUFFER_LENGTH_TYPE | size_t |
| USE_POSIX_ERRNO | Disabled |

CMSIS-RTOS V2 flags:

| | |
|-------------------------------|---------|
| USE_OS2_THREAD_SUSPEND_RESUME | Enabled |
| USE_OS2_THREAD_ENUMERATE | Enabled |
| USE_OS2_EVENTFLAGS_FROM_ISR | Enabled |
| USE_OS2_THREAD_FLAGS | Enabled |
| USE_OS2_TIMER | Enabled |
| USE_OS2_MUTEX | Enabled |

7.8.2. Include parameters:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

Include definitions:

| | |
|------------------------------|----------|
| vTaskPrioritySet | Enabled |
| uxTaskPriorityGet | Enabled |
| vTaskDelete | Enabled |
| vTaskCleanUpResources | Disabled |
| vTaskSuspend | Enabled |
| vTaskDelayUntil | Enabled |
| vTaskDelay | Enabled |
| xTaskGetSchedulerState | Enabled |
| xTaskResumeFromISR | Enabled |
| xQueueGetMutexHolder | Enabled |
| xSemaphoreGetMutexHolder | Disabled |
| pcTaskGetTaskName | Disabled |
| uxTaskGetStackHighWaterMark | Enabled |
| xTaskGetCurrentTaskHandle | Enabled |
| eTaskGetState | Enabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall | Enabled |
| xTaskAbortDelay | Disabled |
| xTaskGetHandle | Disabled |
| uxTaskGetStackHighWaterMark2 | Disabled |

7.8.3. Advanced settings:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

Newlib settings (see parameter description first):

| | |
|----------------------|------------------|
| USE_NEWLIB_REENTRANT | Enabled * |
|----------------------|------------------|

Project settings (see parameter description first):

| | |
|-----------------------|---------|
| Use FW pack heap file | Enabled |
|-----------------------|---------|

7.9. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.9.1. General Settings:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

LwIP Version:

| | |
|--|-------|
| LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **) | 2.1.2 |
|--|-------|

IPv4 - DHCP Options:

| | |
|-------------------------|-------------------|
| LWIP_DHCP (DHCP Module) | Disabled * |
|-------------------------|-------------------|

IP Address Settings:

| | |
|-----------------------------------|--------------------------|
| IP_ADDRESS (IP Address) | 169.254.254.164 * |
| NETMASK_ADDRESS (Netmask Address) | 255.255.000.000 * |
| GATEWAY_ADDRESS (Gateway Address) | 169.254.000.001 * |

RTOS Dependency:

| | |
|--|----------|
| WITH_RTOS (Use FREERTOS ** CubeMX specific **) | Enabled |
| CMSIS_VERSION (CMSIS API Version used) | CMSIS v2 |
| RTOS_USE_NEWLIB_REENTRANT (RTOS used - 1) | Enabled |

Platform Settings:

| | |
|------------|----------------|
| PHY Driver | Choose/LAN8742 |
|------------|----------------|

Protocols Options:

| | |
|--|----------|
| LWIP_ICMP (ICMP Module Activation) | Enabled |
| LWIP_IGMP (IGMP Module) | Disabled |
| LWIP_DNS (DNS Module) | Disabled |
| LWIP_UDP (UDP Module) | Enabled |
| MEMP_NUM_UDP_PCB (Number of UDP Connections) | 4 |
| LWIP_TCP (TCP Module) | Enabled |
| MEMP_NUM_TCP_PCB (Number of TCP Connections) | 5 |

7.9.2. Key Options:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

Infrastructure - OS Awareness Option:

| | |
|-----------------------|---------|
| NO_SYS (OS Awareness) | OS Used |
|-----------------------|---------|

Infrastructure - Timers Options:

| | |
|---|---------|
| LWIP_TIMERS (Use Support For sys_timeout) | Enabled |
|---|---------|

Infrastructure - Core Locking and MPU Options:

| | |
|--|---------|
| SYS_LIGHTWEIGHT_PROT (Memory Functions Protection) | Enabled |
|--|---------|

Infrastructure - Heap and Memory Pools Options:

| | |
|--|--------------|
| MEM_SIZE (Heap Memory Size) | 1600 |
| LWIP_RAM_HEAP_POINTER (RAM Heap Pointer) | 0x30044000 * |

Infrastructure - Internal Memory Pool Sizes:

| | |
|--|----|
| MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs) | 16 |
| MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks) | 4 |
| MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections) | 8 |
| MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued) | 16 |
| MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List) | 1 |

Pbuf Options:

| | |
|--|-----|
| PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool) | 16 |
| PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool) | 592 |

IPv4 - ARP Options:

| | |
|------------------------------|---------|
| LWIP_ARP (ARP Functionality) | Enabled |
|------------------------------|---------|

Callback - TCP Options:

| | |
|--|----------|
| TCP_TTL (Number of Time-To-Live Used by TCP Packets) | 255 |
| TCP_WND (TCP Receive Window Maximum Size) | 2144 |
| TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets) | Enabled |
| LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements) | Disabled |

| | |
|--|------|
| TCP_MSS (Maximum Segment Size) | 536 |
| TCP_SND_BUF (TCP Sender Buffer Space) | 1072 |
| TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender) | 9 |

Network Interfaces Options:

| | |
|---|----------|
| LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes) | Disabled |
| LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif) | Disabled |
| LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes) | Enabled |

NETIF - Loopback Interface Options:

| | |
|--------------------------------------|----------|
| LWIP_NETIF_LOOPBACK (NETIF Loopback) | Disabled |
|--------------------------------------|----------|

Infrastructure - Threading Options:

| | |
|---|----------------|
| TCPIP_THREAD_NAME (TCPIP Thread Name) | "tcpip_thread" |
| TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size) | 1024 |
| TCPIP_THREAD_PRIO (TCPIP Thread Priority Level) | 24 |
| TCPIP_MBOX_SIZE (TCPIP Mailbox Size) | 6 |
| DEFAULT_THREAD_NAME (Default LwIP Thread Name) | "lwip" |
| DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size) | 1024 |
| DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level) | 3 |
| DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw) | 0 |
| DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP) | 6 |
| DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections) | 6 |

Thread Safe APIs - Netconn Options:

| | |
|----------------------------|---------|
| LWIP_NETCONN (NETCONN API) | Enabled |
|----------------------------|---------|

Thread Safe APIs - Socket Options:

| | |
|--|---------|
| LWIP_SOCKET (Socket API) | Enabled |
| LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names) | 1 |
| LWIP_SOCKET_OFFSET (Socket Offset Number) | 0 |
| LWIP_SOCKET_SELECT (Select for Socket) | Enabled |
| LWIP_SOCKET_POLL (Poll for Socket) | Enabled |

7.9.3. PPP:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

PPP Options:

| | |
|--------------------------|----------|
| PPP_SUPPORT (PPP Module) | Disabled |
|--------------------------|----------|

7.9.4. IPv6:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

IPv6 Options:

| | |
|---------------------------|----------|
| LWIP_IPV6 (IPv6 Protocol) | Disabled |
|---------------------------|----------|

7.9.5. HTTPD:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

HTTPD Options:

| | |
|---|------------------|
| LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **) | Enabled * |
|---|------------------|

7.9.6. SNMP:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

SNMP Options:

| | |
|-----------------------------|----------|
| LWIP_SNMP (LwIP SNMP Agent) | Disabled |
|-----------------------------|----------|

7.9.7. SNTP/SMTP:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)

Disabled

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)

Disabled

7.9.8. MDNS/TFTP:

Core(s) Settings:

Context(s):

Cortex-M7

Initialized Context:

Cortex-M7

Power Domain:

D1

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)

Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)

Disabled

7.9.9. Perf/Checks:

Core(s) Settings:

Context(s):

Cortex-M7

Initialized Context:

Cortex-M7

Power Domain:

D1

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)

Disabled

LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)

Disabled

Performance Options:

LWIP_PERF (Performance Testing for LwIP)

Disabled

7.9.10. Statistics:

Core(s) Settings:

Context(s):

Cortex-M7

Initialized Context:

Cortex-M7

Power Domain:

D1

Debug - Statistics Options:

LWIP_STATS (Statistics Collection)

Disabled

7.9.11. Checksum:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

Infrastructure - Checksum Options:

| | |
|--|----------|
| CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **) | Enabled |
| LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif) | Disabled |
| CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets) | Disabled |
| CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets) | Disabled |
| CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets) | Disabled |
| CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets) | Enabled |
| CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets) | Disabled |
| CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets) | Disabled |
| CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets) | Disabled |
| CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets) | Disabled |
| CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets) | Enabled |
| CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets) | Disabled |

7.9.12. Debug:

Core(s) Settings:

| | |
|----------------------|-----------|
| Context(s): | Cortex-M7 |
| Initialized Context: | Cortex-M7 |
| Power Domain: | D1 |

LwIP Main Debugging Options:

| | |
|--------------------------------------|------------------|
| LWIP_DBG_MIN_LEVEL (Minimum Level) | All |
| ETHARP_DEBUG (Debug in Ethernet ARP) | Enabled * |
| NETIF_DEBUG (Debug in NETIF) | Enabled * |
| ICMP_DEBUG (Debug in ICMP) | Enabled * |
| IP_DEBUG (Debug in IP) | Enabled * |
| TCP_DEBUG (Debug in TCP) | Enabled * |

7.9.13. Platform Settings:

Driver_PHY

LAN8742

*** User modified value**

8. System Configuration

8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label | Context | Power Domain |
|--------|------------------------|------------------|------------------------------|-----------------------------|-------------|------------|-------------------------|-------------------------|
| DEBUG | PA13 (JTMS/SWDIO) | DEBUG_JTMS-SWDIO | n/a | n/a | n/a | | Cortex-M7* Cortex-M4 | Cortex-M7* Cortex-M4 |
| | PA14 (JTCK/SWCLK) | DEBUG_JTCK-SWCLK | n/a | n/a | n/a | | Cortex-M7* Cortex-M4 | Cortex-M7* Cortex-M4 |
| | PB3 (JTDO/TRACESWO) | DEBUG_JTDO-SWO | n/a | n/a | n/a | | Cortex-M7* Cortex-M4 | Cortex-M7* Cortex-M4 |
| ETH | PC1 | ETH_MDC | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| | PA1 | ETH_REF_CLK | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| | PA2 | ETH_MDIO | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| | PA7 | ETH_CRS_DV | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| | PC4 | ETH_RXD0 | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| | PC5 | ETH_RXD1 | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| | PB13 | ETH_TXD1 | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| | PG11 | ETH_TX_EN | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| | PG13 | ETH_TXD0 | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | | Cortex-M7 | D2 |
| RCC | PC14-OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | | Cortex-M7* Cortex-M4 | D3 |
| | PC15-OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | | Cortex-M7* Cortex-M4 | D3 |
| | PH0-OSC_IN (PH0) | RCC_OSC_IN | n/a | n/a | n/a | | Cortex-M7* Cortex-M4 | D3 |
| USART3 | PD8 | USART3_TX | Alternate Function | No pull-up and no pull- | Low | STLINK_RX | Cortex-M7 | D2 |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label | Context | Power Domain |
|-----------------------|-------------------|-------------|------------------------------|-----------------------------|-----------|----------------------|-------------------------|-------------------------|
| | | | Push Pull | down | | | | |
| | PD9 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | Low | STLINK_TX | Cortex-M7 | D2 |
| Single Mapped Signals | PH1-OSC_OUT (PH1) | RCC_OSC_OUT | n/a | n/a | n/a | | | |
| GPIO | PC13 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | B1 [Blue PushButton] | Cortex-M7* Cortex-M4 | Cortex-M7* Cortex-M4 |
| | PB0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LD1 [Green Led] | Cortex-M7* Cortex-M4 | Cortex-M7* Cortex-M4 |
| | PB14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LD3 [Red Led] | Cortex-M7* Cortex-M4 | Cortex-M7* Cortex-M4 |
| | PE1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LD2 [Yellow Led] | Cortex-M7* Cortex-M4 | Cortex-M7* Cortex-M4 |

* Initialized context

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC1

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|--------|----------------------|-------------|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 15 | 0 |
| System tick timer | true | 15 | 0 |
| Ethernet global interrupt | true | 5 | 0 |
| TIM17 global interrupt | true | 15 | 0 |
| PVD and AVD interrupts through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| USART3 global interrupt | unused | | |
| Ethernet wake-up interrupt through EXTI line 86 | unused | | |
| CM4 send event interrupt for CM7 | unused | | |
| FPU global interrupt | unused | | |
| HSEM1 global interrupt | unused | | |
| RAM ECC diagnostic global interrupt | unused | | |
| Hold core interrupt | unused | | |

8.5.2. NVIC1 Code generation

| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|-----------------------------------|----------------------|------------------|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| Pre-fetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | false | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | false | false |
| System tick timer | false | false | true |
| Ethernet global interrupt | false | true | true |
| TIM17 global interrupt | false | true | true |

8.5.3. NVIC2

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|--------|----------------------|-------------|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 15 | 0 |
| PVD and AVD interrupts through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| CM7 send event interrupt for CM4 | unused | | |
| FPU global interrupt | unused | | |
| HSEM2 global interrupt | unused | | |
| RAM ECC diagnostic global interrupt | unused | | |
| Hold core interrupt | unused | | |

8.5.4. NVIC2 Code generation

| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|-----------------------------------|----------------------|------------------|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| Pre-fetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | true | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | true | false |
| System tick timer | false | true | true |

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Category view Context Execution view Context Initialization view Power Domain view

Choose filters ...

... by Context Execution: ☐ Cortex-M7 ☐ Cortex-M4

... by Context Initialization: ☐ Cortex-M7 ☐ Cortex-M4 ☒ None

... by Power Domain: ☐ D1 ☐ D2 ☐ D3 ☒ None

Middleware

FREERTOS_M7 ✓

LWIP ✓

| System Core | Analog | Timers | Connectivity | Multimedia | Security | Computing | Trace and Debug | Power and Thermal | Utilities |
|-------------|--------|--------|--------------|------------|----------|-----------|-----------------|-------------------|-----------|
|-------------|--------|--------|--------------|------------|----------|-----------|-----------------|-------------------|-----------|

BDMA

ETH ✓

DEBUG ✓

CORTEX_M4 ✓

USART3 ✓

CORTEX_M7 ✓

DMA

GPIO ⚠

MDMA

NVIC1 ✓

NVIC2 ✓

RCC ✓

SYS ✓

SYS_M4 ✓

9.1.2. Without filters

Category view Context Execution view Context Initialization view Power Domain view

Choose filters ...

... by Context Execution

☐ Cortex-M7 ☐ Cortex-M4

... by Context Initialization

☐ Cortex-M7 ☐ Cortex-M4 ☒ None

... by Power Domain

☐ D1 ☐ D2 ☐ D3 ☒ None

Middleware

FREERTOS_M7 ✓

LWIP ✓

System Core Analog Timers Connectivity Multimedia Security Computing Trace and Debug Power and Thermal Utilities

BDMA

ETH ✓

DEBUG ✓

CORTEX_M4 ✓

USART3 ✓

CORTEX_M7 ✓

DMA

GPIO ⚠

MDMA

IVVIC1 ✓

IVVIC2 ✓

RCC ✓

SYS ✓

SYS_M4 ✓

9.2. Context Execution view

Category view **Context Execution view** Context Initialization view Power Domain view

Cortex-M4

DEBUG ✓

GPI0 ⚠

RCC ✓

CORTEX_M4 ✓

HWIC2 ✓

SYS_M4 ✓

Cortex-M7

DEBUG ✓

GPI0 ⚠

RCC ✓

CORTEX_M7 ✓

ETH ✓

FREERTOS_M7 ✓

LWIP ✓

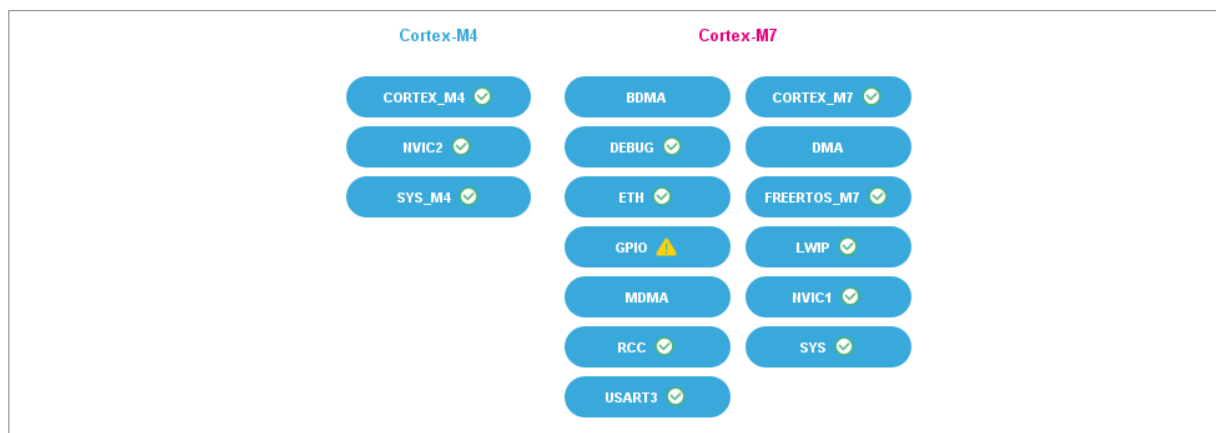
HWIC1 ✓

SYS ✓

USART3 ✓

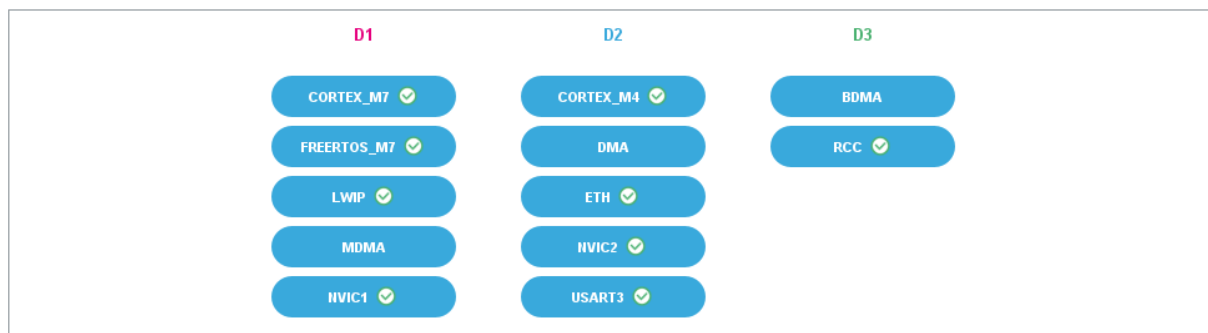
9.3. Context Initialization view

Category view Context Execution view Context Initialization view Power Domain view



9.4. Power Domain view

Category view Context Execution view Context Initialization view Power Domain view



10. Docs & Resources

| Type | Link |
|-------------------|---|
| Presentations | https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf |
| Training Material | https://www.st.com/resource/en/sales_guide/sg_sc2154.pdf |
| Training Material | https://www.st.com/resource/en/training_certification/faecp_stm32h7_dual_core_edr.pdf |
| Training Material | https://www.st.com/resource/en/training_certification/faecp_stm32h7_edr.pdf |
| Brochures | https://www.st.com/resource/en/brochure/brstm32h7.pdf |
| Brochures | https://www.st.com/resource/en/brochure/brstm32h7vl.pdf |
| Flyers | https://www.st.com/resource/en/flyer/flnucleolrwan.pdf |
| Flyers | https://www.st.com/resource/en/flyer/flstm32nucleo.pdf |
| Flyers | https://www.st.com/resource/en/flyer/flstm32trust.pdf |
| Application Notes | https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf |
| Application Notes | https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf |
| Application Notes | https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf |
| Application Notes | https://www.st.com/resource/en/application_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf |

Application Notes https://www.st.com/resource/en/application_note/an2834-how-to-get-the-best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf

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& Software

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& Software

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