LABORATÓRIO 2

Dupla:
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3.2

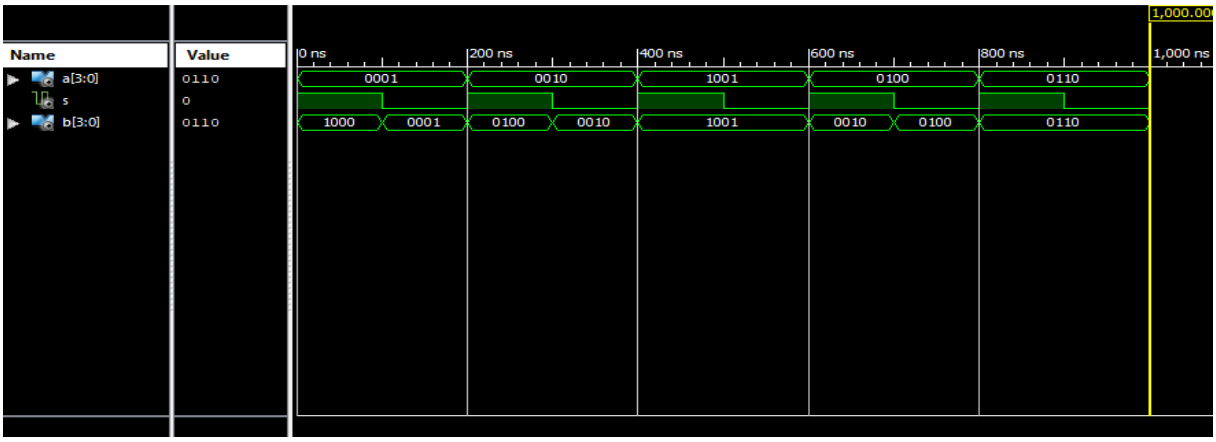
```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;


entity inversor is

    Port ( A : in  STD_LOGIC_VECTOR (3 downto 0);

           S : in  STD_LOGIC;

           B : out  STD_LOGIC_VECTOR (3 downto 0) );

end inversor;


architecture rtl of inversor is


begin

B(0) <= A(3) when S = '1' else A(0);

B(1) <= A(2) when S = '1' else A(1);

B(2) <= A(1) when S = '1' else A(2);

B(3) <= A(0) when S = '1' else A(3);

end rtl;
```

3.3

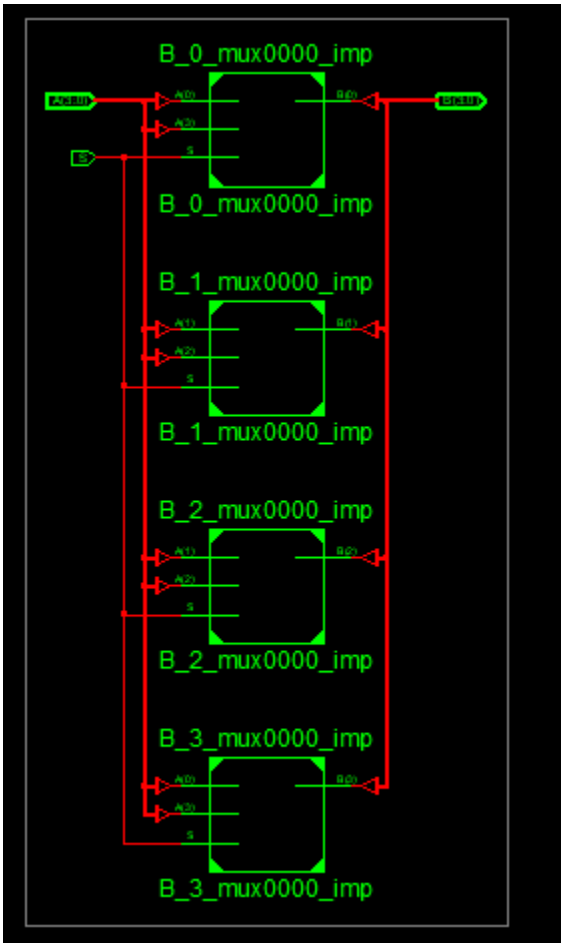
```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;


ENTITY inversor_tb IS

END inversor_tb;
```

```
ARCHITECTURE behavior OF inversor_tb IS
  --Inputs
  signal A : std_logic_vector(3 downto 0);
  signal S : std_logic;
--Outputs
  signal B : std_logic_vector(3 downto 0);

BEGIN
-- Instantiate the Unit Under Test (UUT)
  uut: entity work.inversor PORT MAP (
        A => A,
        S => S,
        B => B
       );

  -- Stimulus process
A <= "0001", "0010" after 200 ns, "1001" after 400 ns, "0100" after 600 ns, "0110" after 800 ns;
S <= '1', '0' after 100 ns ,  '1' after 200 ns,  '0' after 300 ns,  '1' after 400 ns , '0' after 500 ns,  '1' after 600 ns, '0' after 700 ns,  '1' after 800 ns, '0' after 900 ns;

END;
```

3.4


Name
Value
a[3:0]
0110
s
0
b[3:0]
0110
0 ns
200 ns
400 ns
600 ns
800 ns
1,000 ns
0001
0010
1001
0100
0110
1000
0001
0100
0010
1001
0010
0100
0110

3.5


B_0_mux0000_imp
B_0_mux0000_imp
B_1_mux0000_imp
B_1_mux0000_imp
B_2_mux0000_imp
B_2_mux0000_imp
B_3_mux0000_imp
B_3_mux0000_imp

O circuito funciona tendo 4 multiplexadores, a saída de cada um deles é um bit do vetor de saída. Esse bit do vetor de saída é escolhido entre o bit do vetor de entrada da mesma posição ou da posição invertida dependendo do valor do seletor, se ele for 1 escolhe o bit da posição invertida se for 0 o bit da mesma posição.