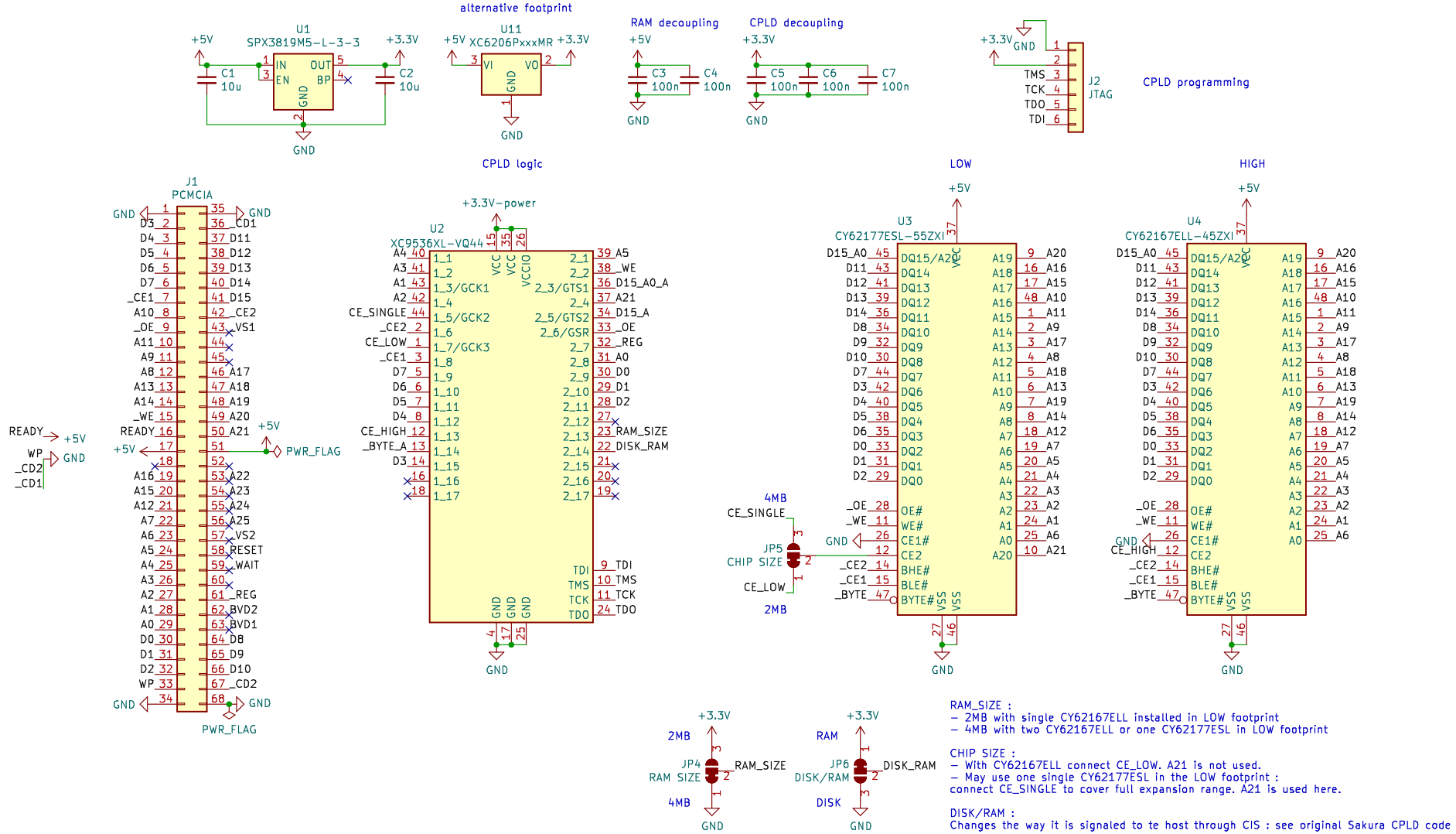
alternative footprint
U1
SPX3819M5-L-3-3
U11
XC6206PxxxMR
RAM decoupling
CPLD decoupling
CPLD programming
J2
JTAG
CPLD logic
+3.3V-power
J1
PCMCIA
U2
XC9536XL-VQ44
LOW
HIGH
U3
CY62177ESL-55ZXI
U4
CY62167ELL-45ZXI
4MB
2MB
JP5
CHIP SIZE
JP4
RAM SIZE
JP6
DISK/RAM
RAM_SIZE :
– 2MB with single CY62167ELL installed in LOW footprint
– 4MB with two CY62167ELL or one CY62177ESL in LOW footprint
CHIP SIZE :
– With CY62167ELL connect CE_LOW. A21 is not used.
– May use one single CY62177ESL in the LOW footprint :
connect CE_SINGLE to cover full expansion range. A21 is used here.
DISK/RAM :
Changes the way it is signaled to te host through CIS : see original Sakura CPLD code
FID2
Logo
FID1
License
Odd-byte-low feature:
The PCMCIA 8bit feature, which makes the "Odd byte" available on D7:D0, is not necessary for Amiga computers.
– To bypass the 8bit feature, close "D15 direct", open the two other links, and tie _BYTE to 5V. This is the default.
For other systems:
Not sure if dynamically changing the BYTE# signal will work, and if the IO15_Axx signal will effectively select the correct bytes. According to Cypress this should not work : https://community.cypress.com/message/231471
– To try the workaround, open "D15 direct" and close the other links, and connect _BYTE to the CPLD
When processed by the CPLD :
– In 8 bit mode (_CE1=0 & _CE2=1 & A0=1), _BYTE=0, D15_A0=1, and D15=Z
– In 16 bit mode,
– _BYTE=1,
– D15 is output to D15_A0 when _WE=0,
– D15_A0 is output to D15 when _OE=0 & CE_SINGLE=1 & _CE2=0
JP2
D15 direct
JP1
D15 pcmia
JP3
D15 A0
JP7
Simplified to use 5v parts available in 2020
Inspired by Sakura designs https://github.com/Sakura-IT/ppa-pcmcia-sram
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Sheet: /
File: PCMCIA_SRAM.kicad_sch
Title: PCMCIA SRAM
Size: A4
Date: 2020-04-19
Rev: v1.0
KiCad E.D.A. kicad 6.0.8-f2edbf62ab~116~ubuntu22.04.1
Id: 1/1