GameBoy Cartridges
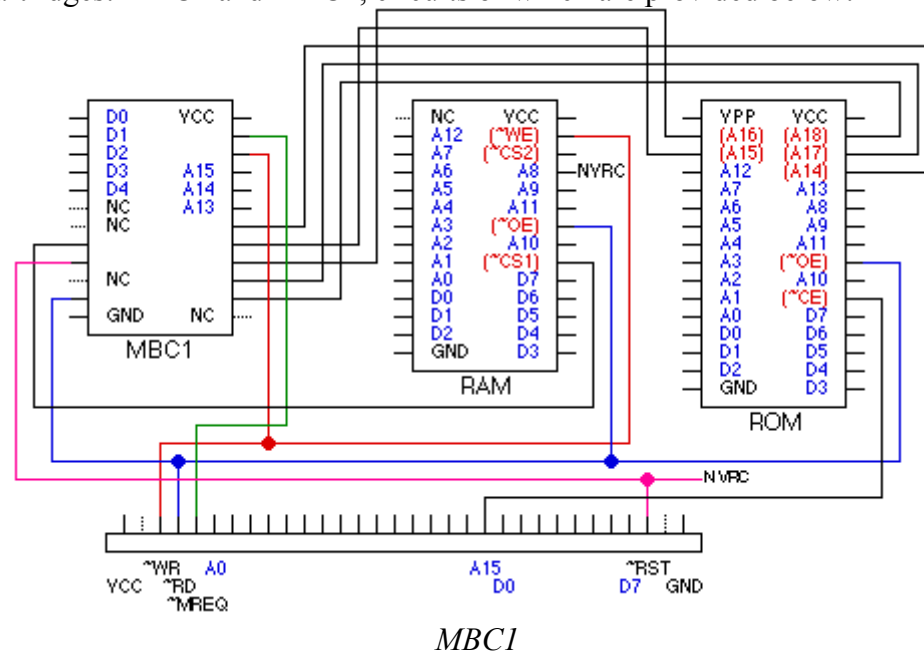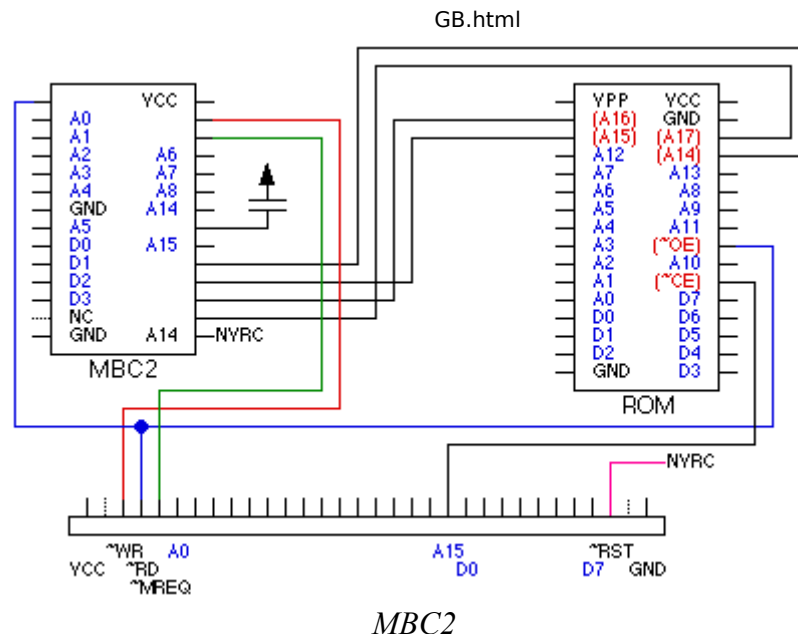
There are two different types of GB cartridges: MBC1 and MBC2, circuits of which are provided below:

MBC1

MBC2

Memory Bank Controllers

Memory bank controllers (MBCs) allow to switch banks and control backup RAM. MBCs contain registers (5 bits for MBC1, 4 bits for MBC2) in which you load the value of a memory bank before accessing it.

MBC1 is controlled by the A15..A13 address lines, MBC2 by A15,A14,A8. Banks are written in D0..D4 (D0..D3 for MBC2). When controlling both RAM and ROM, ROM is selected when A15 is low (addresses 0000h to 7FFFh).

The back-up memory is preserved by a 3V lithium battery together with a NV-RAM controller. The ~MREQ line is low each time the processor makes a memory access (e.g. with the LD operation), but not when it fetches instructions.

MBC1

A15	A14	A13	~RD	~WR	~MREQ	
0	0	×	0	1	×	Read ROM bank 0 (A13..A0)
0	1	×	0	1	×	Read ROM bank 1..31 (A13..A0)
1	0	1	0	1	0	Read RAM (A12..A0)
1	0	1	1	0	0	Write RAM (A12..A0)
0	0	1	1	0	×	Load ROM bank register (1..31)
0	1	0	1	0	×	Load RAM bank register
0	0	0	1	0	×	Initialize MBC (D4..D0 = 0x0A)

MBC1 can control up to 4 MBits (32 banks * 128kBits) of ROM together with several pages of RAM. Games which need more RAM that the limited internal RAM use MBC1. The first page of RAM may be backed up with a battery.

MBC2

A15	A14	A8	~RD	~WR	~MREQ	
0	0	×	0	1	×	Read ROM bank 0 (A13..A0)
0	1	×	0	1	×	Read ROM bank 1..15 (A13..A0)
1	0	×	0	1	0	Read RAM (A7..A0)
1	0	×	1	0	0	Write RAM (A7..A0)
0	0	1	1	0	×	Load bank register (1..15)
0	0	0	1	0	×	Initialize MBC (D3..D0 = 0x0A)

MBC2 has 512 * 4 bit of internal memory used as back-up memory. It is accessed using A8..A0 and D3..D0.

If you have have any question or remark, send mail to *felber@di.epfl.ch*.