blue ones have their explanation below

| encoding | state | outputs | | | | | | | | | | | state | outputs | | | | | | | state | outputs | | | internal signals | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | done | error | ar_valid | r_ready | aw_valid | w_valid | b_ready | sl_1_incd_to_i | ld_i | sl_i_m1_j_m1_to_j | ld_j | | ld_elem2insert | ld_elem2compare | sl_i_j_to_read_addr | ld_arg_read_addr | ld_return_read_data | sl_j_j_p1_to_wr_addr | ld_arg_write_addr | | sl_e2ins_e2cmp_to_w | ld_arg_write_data | sl_to_return_state | ld_arg_return_state | sl_to_state |
| | wait_start | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | wait_start | x | 0 | x | 0 | 0 | x | 0 | wait_start | x | 0 | x | 0 | 0 |
| | assign_i | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | 0 | assign_i | x | 0 | x | 0 | 0 | x | 0 | assign_i | x | 0 | x | 0 | 0 |
| | outer_loop_check | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | outer_loop_check | x | 0 | x | 0 | 0 | x | 0 | outer_loop_check | x | 0 | x | 0 | 0 |
| | done | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | done | x | 0 | x | 0 | 0 | x | 0 | done | x | 0 | x | 0 | 0 |
| | read_arr_i | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | read_arr_i | x | 0 | 0 | 1 | 0 | x | 0 | read_arr_i | x | 0 | ASSGN_E2INS | 1 | 0 |
| | assign_elem2insert | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | assign_elem2insert | 1 | 0 | x | 0 | 0 | x | 0 | assign_elem2insert | x | 0 | x | 0 | 0 |
| | assng_j | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | 0 | 1 | assng_j | x | 0 | x | 0 | 0 | x | 0 | assng_j | x | 0 | x | 0 | 0 |
| | inner_loop_check | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | inner_loop_check | x | 0 | x | 0 | 0 | x | 0 | inner_loop_check | x | 0 | x | 0 | 0 |
| | inc_i | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | x | 0 | inc_i | x | 0 | x | 0 | 0 | x | 0 | inc_i | x | 0 | x | 0 | 0 |
| | read_arr_j | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | read_arr_j | x | 0 | 1 | 1 | 0 | x | 0 | read_arr_j | x | 0 | ASSGN_E2CMP | 1 | 0 |
| | assign_elem2compare | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | assign_elem2compare | x | 1 | x | 0 | 0 | x | 0 | assign_elem2compare | x | 0 | x | 0 | 0 |
| | check_if_correct_place | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | check_if_correct_place | x | 0 | x | 0 | 0 | x | 0 | check_if_correct_place | x | 0 | x | 0 | 0 |
| | shift_elem2insert_left | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | shift_elem2insert_left | x | 0 | x | 0 | 0 | 0 | 1 | shift_elem2insert_left | 0 | 1 | SR_E2CMP | 1 | 0 |
| | | done | error | ar_valid | r_ready | aw_valid | w_valid | b_ready | sl_1_incd_to_i | ld_i | sl_i_m1_j_m1_to_j | ld_j | state | ld_elem2insert | ld_elem2compare | sl_i_j_to_read_addr | ld_arg_read_addr | ld_return_read_data | sl_j_j_p1_to_wr_addr | ld_arg_write_addr | state | sl_e2ins_e2cmp_to_w | ld_arg_write_data | sl_to_return_state | ld_arg_return_state | sl_to_state |
| | shif_elem2compare_right | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | shif_elem2compare_right | x | 0 | x | 0 | 0 | 1 | 1 | shif_elem2compare_right | 1 | 1 | DECRMT_J | 1 | 0 |
| | decrmt_j | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | 1 | 1 | decrmt_j | x | 0 | x | 0 | 0 | x | 0 | decrmt_j | x | 0 | x | 0 | 0 |
| | read_function | 0 | 0 | 1 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | read_function | x | 0 | x | 0 | 0 | x | 0 | read_function | x | 0 | x | 0 | 0 |
| | wait_ar_ready | 0 | 0 | 1 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | wait_ar_ready | x | 0 | x | 0 | 0 | x | 0 | wait_ar_ready | x | 0 | x | 0 | 0 |
| | complete_ar | 0 | 0 | 0 | 1 | 0 | 0 | 0 | x | 0 | x | 0 | complete_ar | x | 0 | x | 0 | 0 | x | 0 | complete_ar | x | 0 | x | 0 | 0 |
| | wait_r_valid | 0 | 0 | 0 | 1 | 0 | 0 | 0 | x | 0 | x | 0 | wait_r_valid | x | 0 | x | 0 | 0 | x | 0 | wait_r_valid | x | 0 | x | 0 | 0 |
| | process_r_data_resp | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | process_r_data_resp | x | 0 | x | 0 | 1 | x | 0 | process_r_data_resp | x | 0 | x | 0 | 0 |
| | return_read_fn | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | return_read_fn | x | 0 | x | 0 | 0 | x | 0 | return_read_fn | x | 0 | x | 0 | 1 |
| | write_function | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | write_function | x | 0 | x | 0 | 0 | x | 0 | write_function | x | 0 | x | 0 | 0 |
| | send_addr_and_data | 0 | 0 | 0 | 0 | 1 | 1 | 0 | x | 0 | x | 0 | send_addr_and_data | x | 0 | x | 0 | 0 | x | 0 | send_addr_and_data | x | 0 | x | 0 | 0 |
| | wait_aw_ready_or_w_ready | 0 | 0 | 0 | 0 | 1 | 1 | 0 | x | 0 | x | 0 | wait_aw_ready_or_w_ready | x | 0 | x | 0 | 0 | x | 0 | wait_aw_ready_or_w_ready | x | 0 | x | 0 | 0 |
| | complete_w_wait_aw_ready | 0 | 0 | 0 | 0 | 1 | 0 | 0 | x | 0 | x | 0 | complete_w_wait_aw_ready | x | 0 | x | 0 | 0 | x | 0 | complete_w_wait_aw_ready | x | 0 | x | 0 | 0 |
| | complete_aw | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | 0 | x | 0 | complete_aw | x | 0 | x | 0 | 0 | x | 0 | complete_aw | x | 0 | x | 0 | 0 |
| | complete_aw_wait_w_ready | 0 | 0 | 0 | 0 | 0 | 1 | 0 | x | 0 | x | 0 | complete_aw_wait_w_ready | x | 0 | x | 0 | 0 | x | 0 | complete_aw_wait_w_ready | x | 0 | x | 0 | 0 |
| | complete_w | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | 0 | x | 0 | complete_w | x | 0 | x | 0 | 0 | x | 0 | complete_w | x | 0 | x | 0 | 0 |
| | complete_aw_and_w | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | 0 | x | 0 | complete_aw_and_w | x | 0 | x | 0 | 0 | x | 0 | complete_aw_and_w | x | 0 | x | 0 | 0 |
| | wait_b_valid | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | 0 | x | 0 | wait_b_valid | x | 0 | x | 0 | 0 | x | 0 | wait_b_valid | x | 0 | x | 0 | 0 |
| | process_b_resp | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | process_b_resp | x | 0 | x | 0 | 0 | x | 0 | process_b_resp | x | 0 | x | 0 | 0 |
| | return_write_fn | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | return_write_fn | x | 0 | x | 0 | 0 | x | 0 | return_write_fn | x | 0 | x | 0 | 1 |
| | err | 0 | 1 | 0 | 0 | 0 | 0 | 0 | x | 0 | x | 0 | err | x | 0 | x | 0 | 0 | x | 0 | err | x | 0 | x | 0 | 0 |

| abbreviation | actual form in the circuit |
|---|---|
| sl_i_m1_j_m1_to_j | sl_i_minus_1_decrd_to_j |
| sl_i_j_to_read_addr | sl_i_j_to_arg_read_addr |
| sl_j_j_p1_to_wr_addr | sl_j_j_plus_1_to_arg_write_addr |
| sl_e2ins_e2cmp_to_w | sl_elem2insert_elem2compare_to_arg_write_data |
| sl_to_return_state | sl_to_arg_return_state |

| those symbols below represents the encoding of the state of their same name |
|---|
| DECRMT_J |
| SR_E2CMP |
| ASSGN_E2CMP |
| ASSGN_E2INS |