EXPERIMENT NO. 1 FLAT TOP SAMPLING

Aim

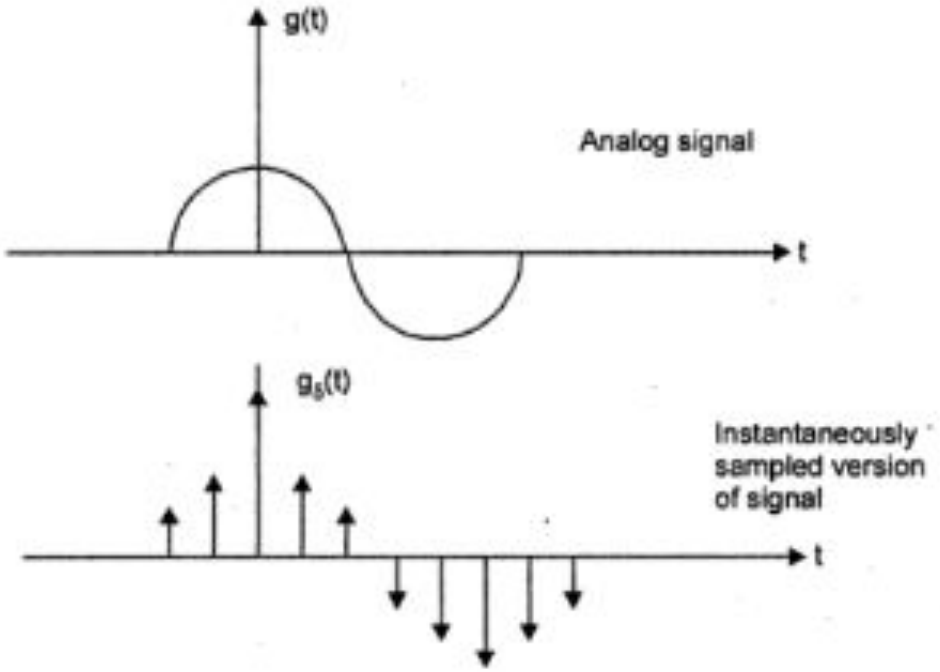
To design and demonstrate the working of the flat top sampling circuit for a ..... Hz. message signal. Demonstrate the effect of (*a*) under sampling (*b*) over sampling (*c*) right sampling.

Components Required

Transistor (SL 100, SK 100), Resistors (10 kΩ, 1kΩ), Capacitor (0.1 μF), Opamp (μA 741).

Theory

In the sampling process, an analog signal is converted into a corresponding sequence of samples that are usually spaced uniformly in time. $g(t)$ is necessary so that we can choose the sampling rate properly, so that the sequence of samples uniquely defines the original analog signal.



Consider a segment of arbitrary signal $g(t)$ as shown in figure. Suppose we sample the signal $g(t)$ instantaneously and at a uniform rate, once every T_S seconds. Consequently, we obtain an infinite sequence if samples spaced 'T_s' seconds apart and denoted by $\{g(nT_S)\}$

T_S = Sampling period

$$F_S = \text{Sampling rate} = \frac{1}{T_S}$$

$$g_\delta(t) = \sum_{n=-\infty}^{\infty} g(nT_S)\,\delta(t - nT_S)$$

Sampling Theorem

A band limited signal of finite energy, which has no frequency components higher than 'W' hertz, may be completely recovered from the knowledge of its samples taken at the rate of 2W samples per second.

Quantizing

Representing the analog sampled values by a finite set of levels is called quantizing *i.e.*, it converts continuous amplitude sample to a discrete amplitude samples.

Sampling

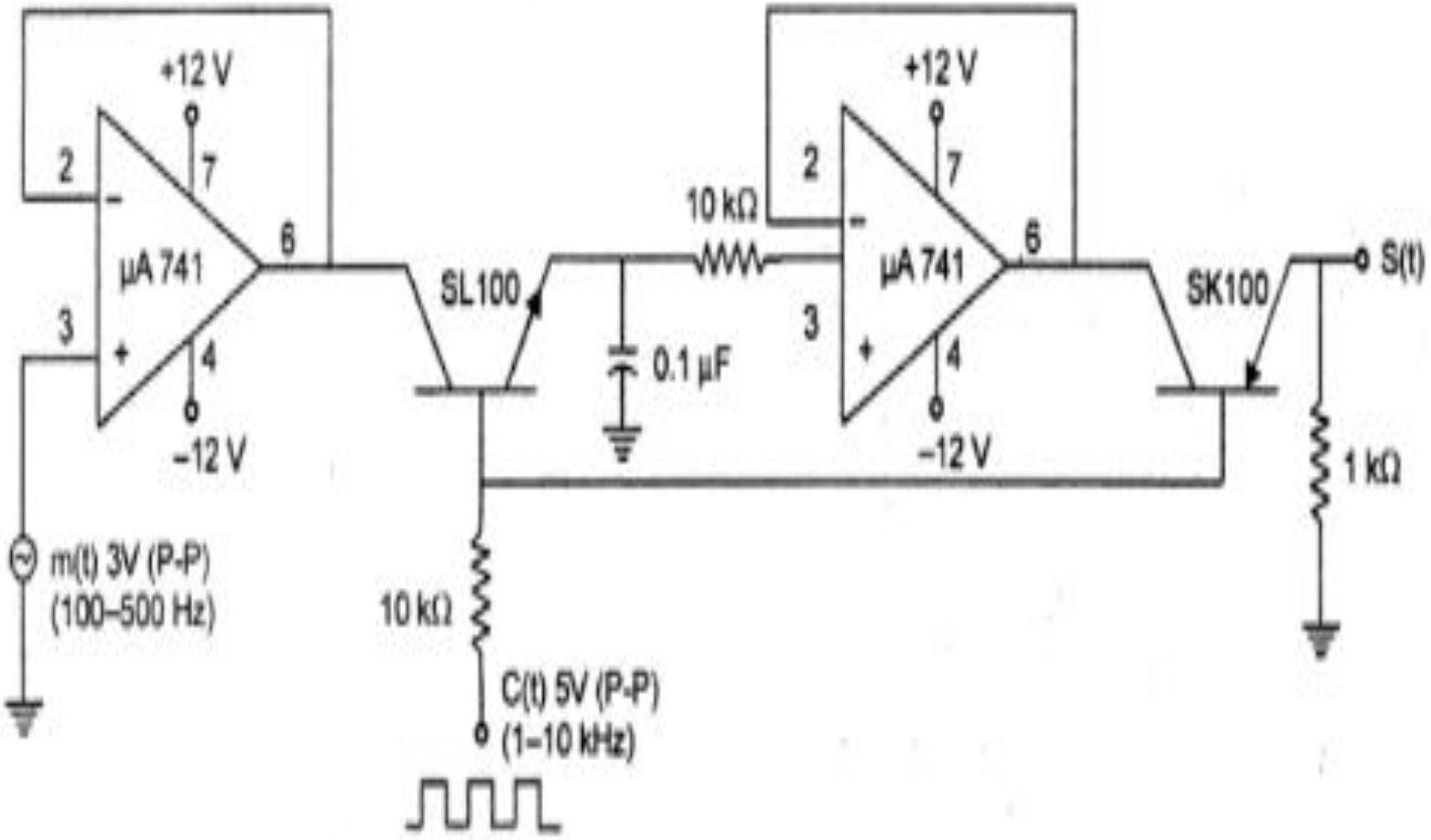
Converting a continuous time signal to a discrete time signal.

Application

Sampling theorem serves as the basic for the interchangeability of analog signals and digital sequences, which is so valuable in digital signal processing, and digital communications.

Circuit-Diagram

Modulator



Demodulator

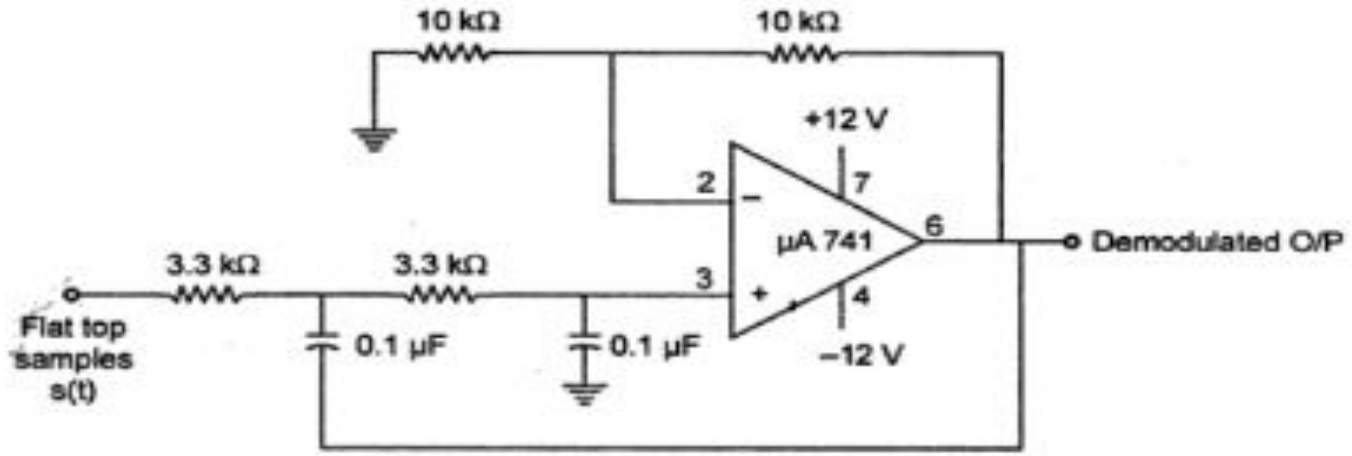


Figure 1.2: Demodulator

Design

(1) Flat top sampling

$$RC << T_m$$

where $T_m = 3.3$ ms

Assume $f_m = 300$ Hz

Let $RC = 1$ ms

Let $R = 10\ k\Omega$

$\therefore$ $C = 0.1\ \mu F$

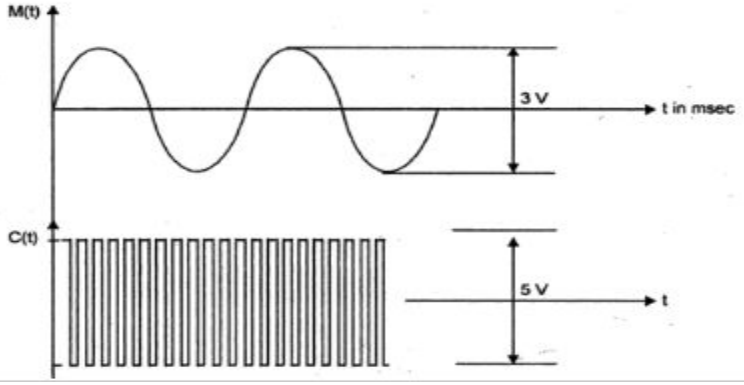
(2) Demodulation

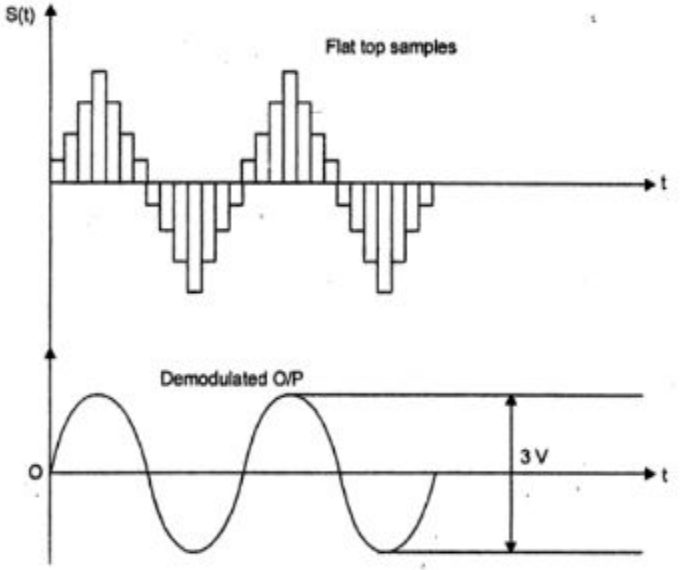
$$f = \frac{1}{2\pi RC} = 500 \text{ Hz}$$

Let $C_1 = 0.1\ \mu F,$

then $R_1 = 3.1\ k\Omega$

$\simeq 3.3\ k\Omega$





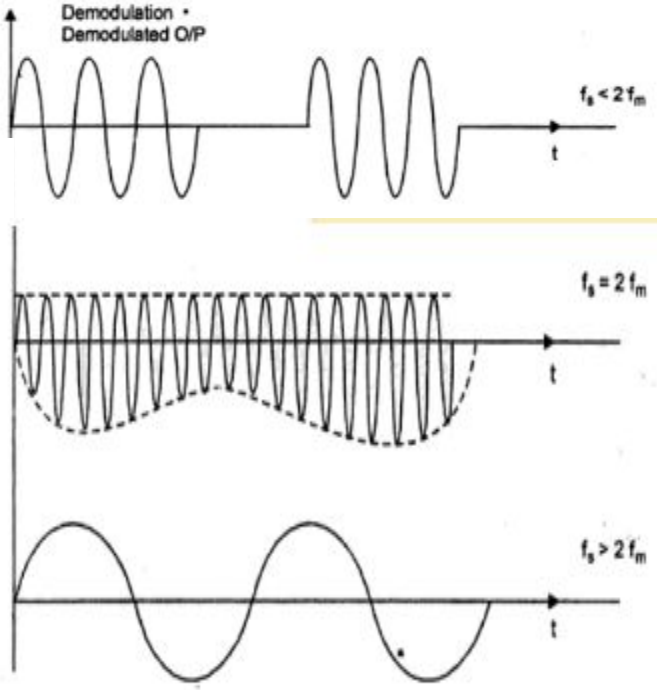
Procedure

Modulation

1. Rig up the circuit as per the circuit-diagram.
2. Select $m(t)$ = 3 V, 100–500 Hz (sine-wave).
3. Select C(t) = 5 V, 1–10 kHz (f_s – square wave).
4. Observe the flat top sampling output.

Demodulation

1. Connect the demodulator circuit to flat top sampling circuit.
2. Observe the output for $f_s < 2f_m$, $f_s = 2f_m$ and $f_s > 2f_m$.



Result

The sampling of the signal is achieved and sampling theorem is verified.

EXPERIMENT NO. 2 TIME DIVISION MULTIPLEXING (TDM)

Aim

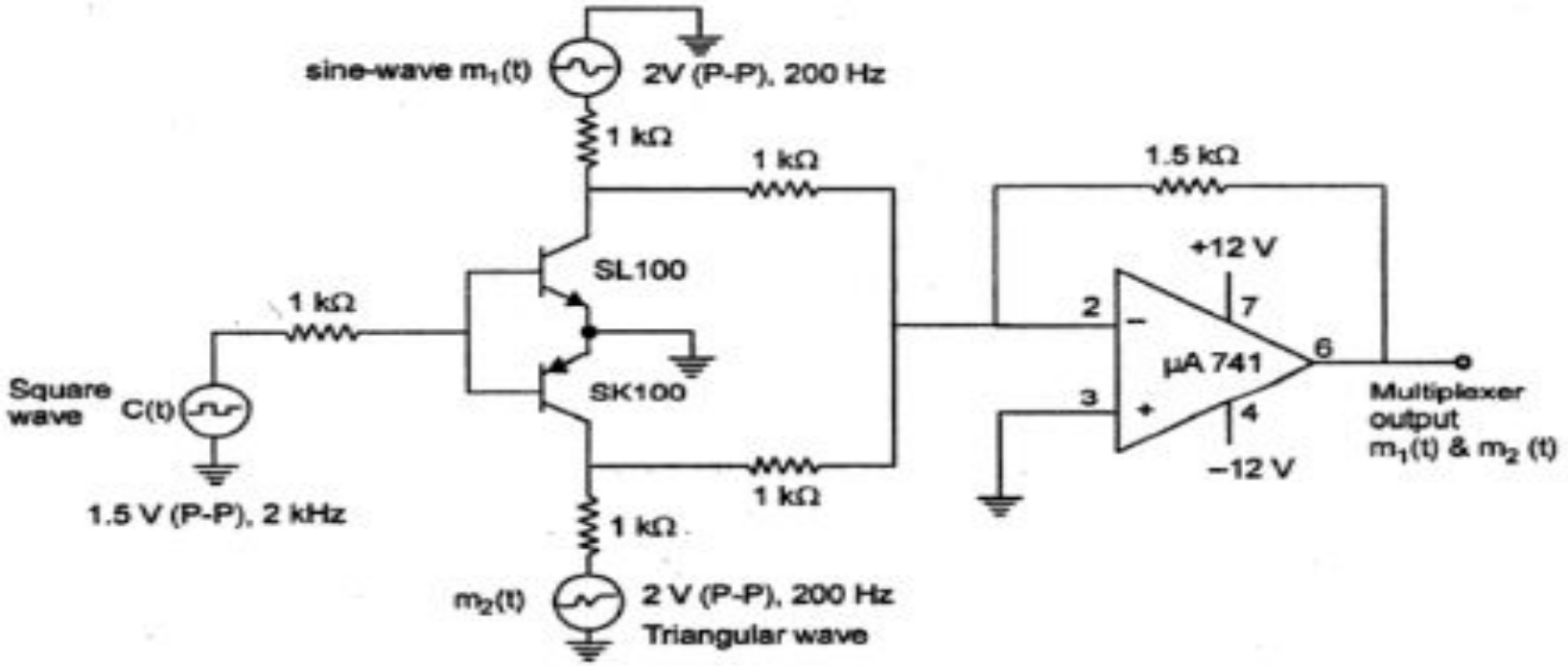
To design and demonstrate the working of TDM and recovery of two band limited signals of PAM signals.

Components Required

Transistors—SL100, SK100, Resistors—1 kΩ, 1.5 kΩ, Opamp μA 741.

Circuit-Diagram

Multiplexer



Demultiplexer

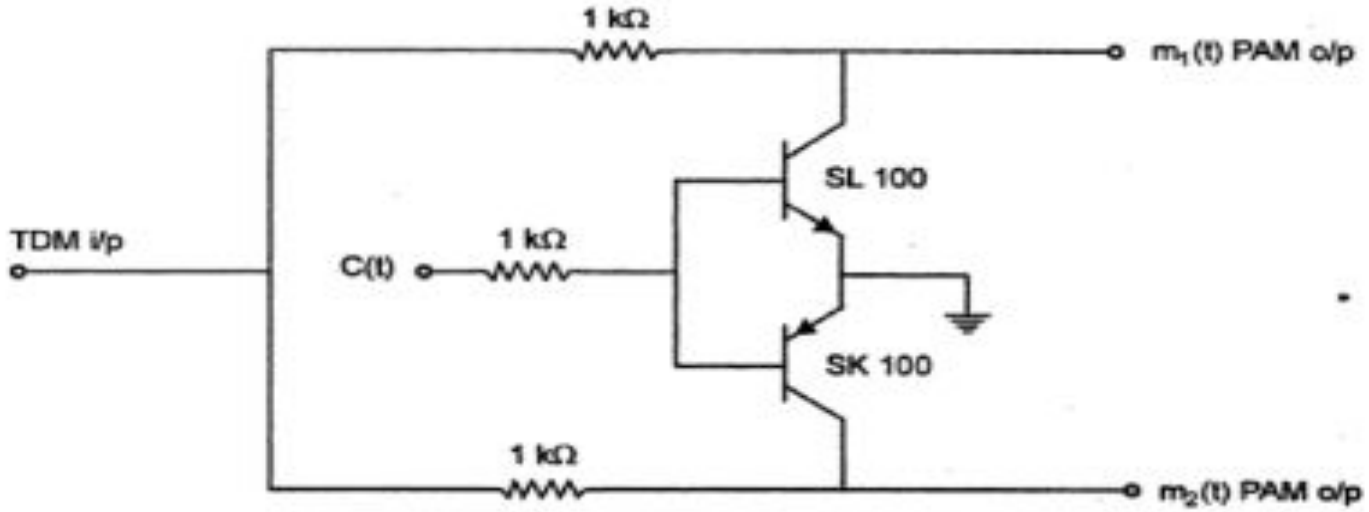


Figure 2.2: Demultiplexer

Theory

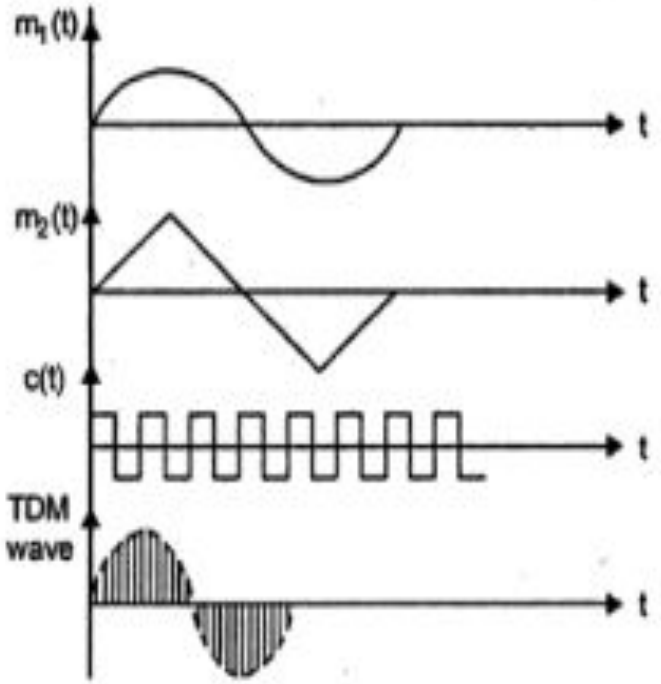
TDM is a technique used for transmitting several message signals over a communication channel by dividing the time frame into slots, one slot for each message signal. This is a digital technique in which the circuit is highly modular in nature and provides reliable and efficient operation. There is no cross talk in TDM due to circuit non-linearities since the pulses are completely isolated. But it also has its disadvantages, which include timing jitter and synchronization is required.

In pulse-amplitude modulation, the amplitude of a periodic train of pulses is varied in proportion to a message signal. TDM provides an effective method for sharing a communication channel.

Procedure

1. Rig up the circuit as shown in the circuit-diagram for multiplexer.
2. Feed the input message signals m_1 and m_2 of 2 volts P-P at 200 Hz.
3. Feed the high frequency carrier signal of 2V (P–P) at 2 kHz.
4. Observe the multiplexed output.
5. Rig up the circuit for demultiplexer.
6. Observe the demultiplexed output in the CRO.

Waveforms



Result

TDM circuit using PAM signals (both multiplexer and demultiplexer) has been designed and demonstrated.

EXPERIMENT NO. 3 AMPLITUDE SHIFT KEYING (ASK)

Aim

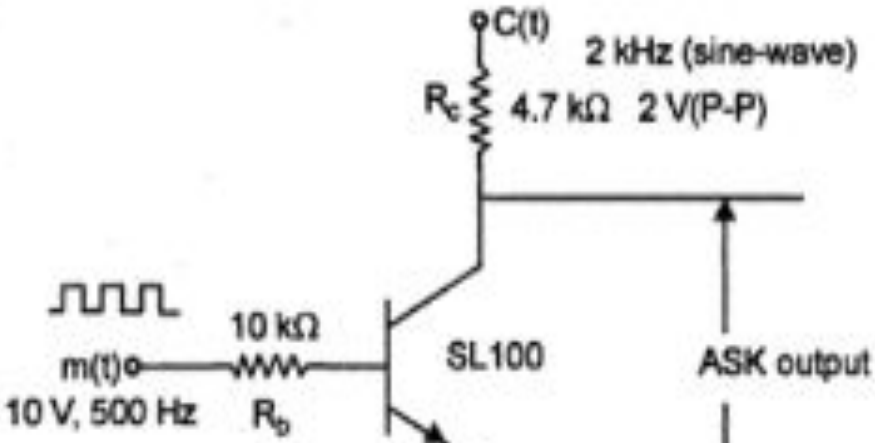
To design and verify the operation of ASK generator and demodulator.

Components Required

Transistor SL100, Resistors—4.7 kΩ, 20 kΩ (pot), 10 kΩ (pot), Opamp μA 741, Diode-By127.

Circuit-Diagram

Modulator



Demodulator

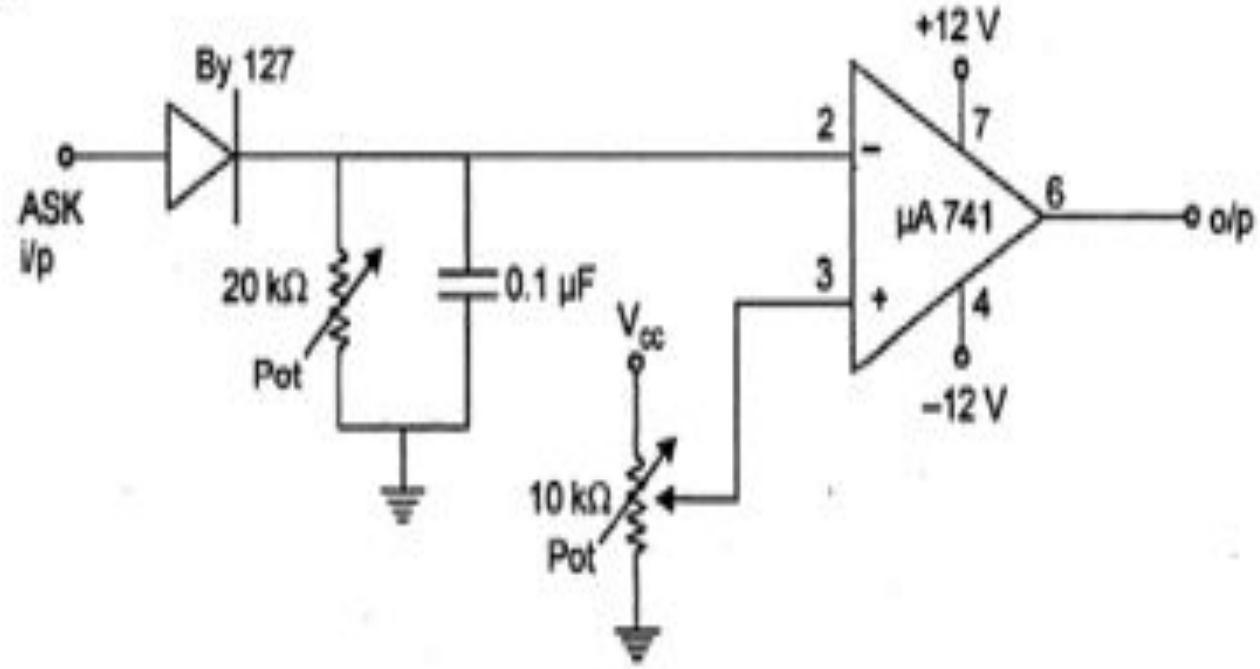


Figure 3.2: Demodulator

Design

1. Modulator

Let $C(t) = 2$ V, $I_c = 0.4\ mA$, $I_b = 0.9\ mA$

$$R_c = \frac{C(t) - V_{ce}(sat)}{I_c} = \frac{2 - 0.3}{0.4 \times 10^{-3}} = 4.25\ k\Omega$$

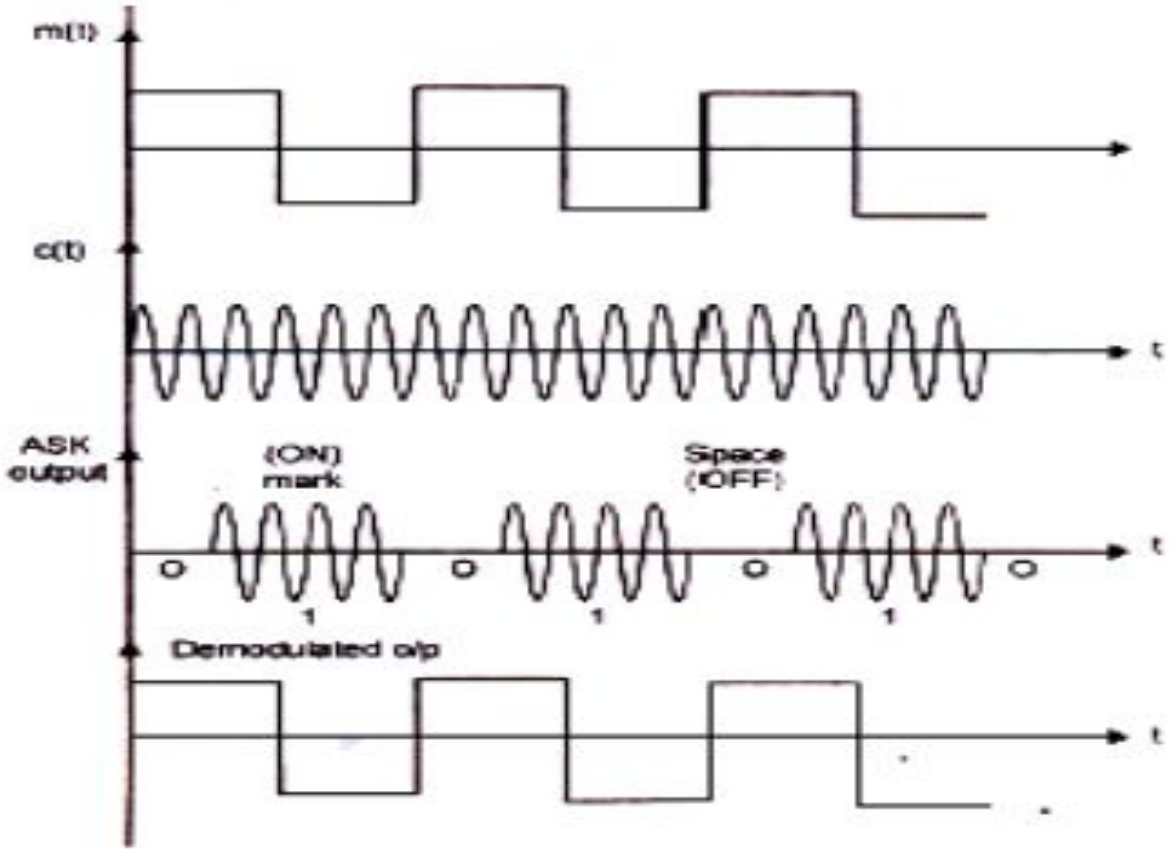
2. Demodulator (Envelope Detector)

$$\frac{1}{\omega_c} < RC < \frac{1}{\omega}$$

Let $C = 0.1\ \mu F$, $RC = 1ms$

$$R = \frac{10^{-3}}{0.1 \times 10^{-6}} = 10\ k\Omega.$$

EXPECTED WAVEFORMS:



FREQUENCY SHIFT KEYING

AIM:

To set up FSK modulator and demodulator circuits and to observe the waveforms.

OBJECTIVES:

After completing this experiment, the students will be able to a) Set up FSK modulator and demodulator circuits and b) Identify FSK waveform.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No.	Item & Specification	Quantity
1	Transistor- BC 177	1No.
2	Resistor- 47K, 47K pot, 10K pot 10K	1No. each 7Nos.
3	Capacitor- 0.01μF 0.02μF 0.047μF, 0.001μF	3Nos. 4Nos. 1No.each
4	IC LM311	1No.
5	IC 555, IC 565	1No. each
6	Signal Generator	1Nos.
7	CRO	1No.
8	Power Supply- +/- 5V	1No.

THEORY:

Frequency Shift Keying (FSK) is a digital modulation scheme where the digital data is transmitted using a high frequency carrier signal. For logic '0' and '1' the carrier signal switches between two preset frequencies, hence the name FSK.

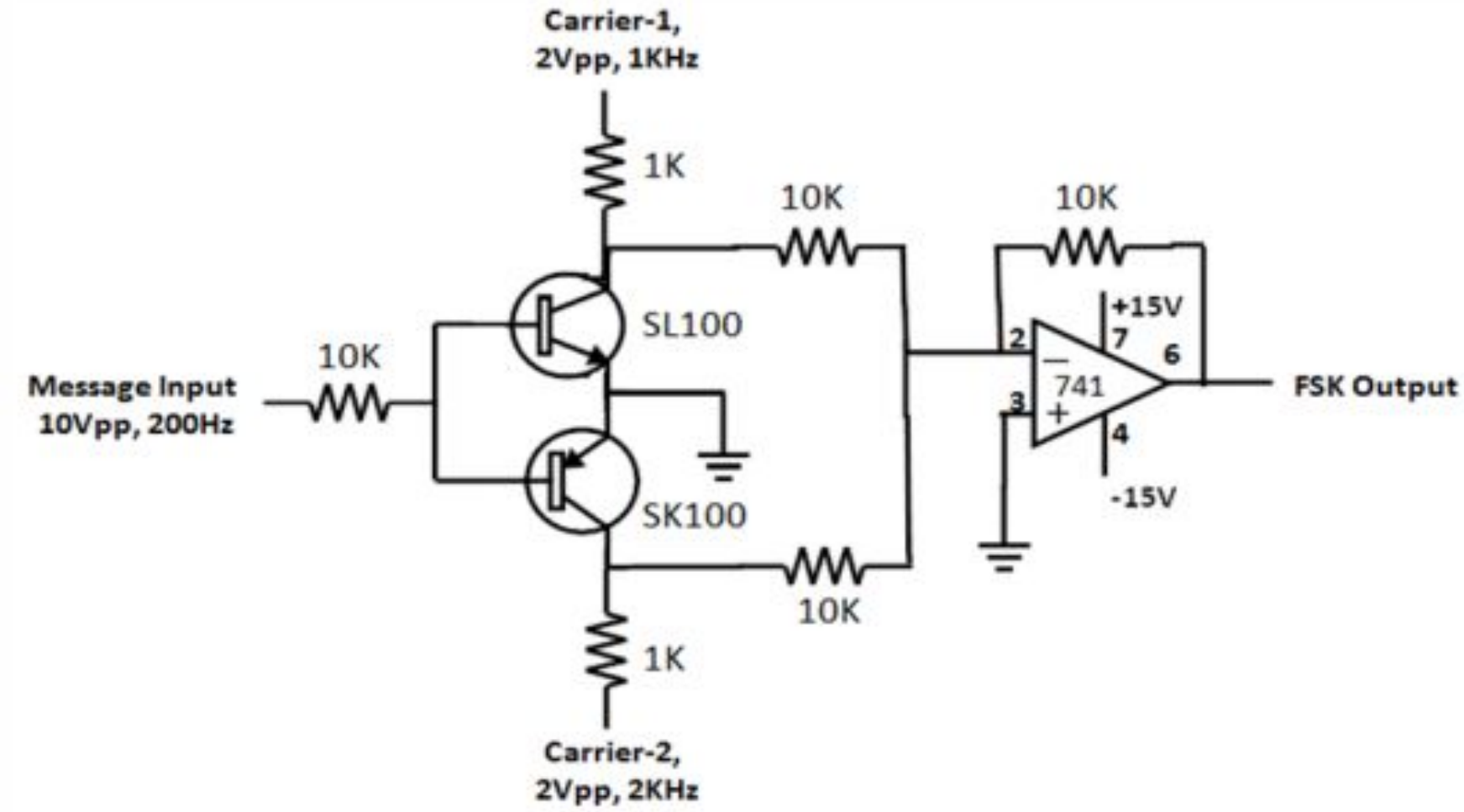
A frequency shift keying modulator circuit made up of 555 timer is shown in figure. The 555 works in monostable mode. For logic '1' transistor BC 177 is OFF and the monostable works in normal mode and capacitor C1 charges through R_A and R_B and the output frequency is at the first preset level. For logic '0' the transistor is ON and the resistor R_C comes in parallel with R_A and reduces its effective resistance. The charging rate of the capacitor increases and a higher frequency signal is obtained at the output. This is the second preset frequency level. Thus the output signal switches between the two preset frequencies for logic '0' and '1'. The resulting signal is FSK modulated.

PLL IC 565 is used to demodulate the FSK signal. As the signal appears at the input of 565 PLL, the PLL locks to the input frequency and tracks it between the two possible frequencies with a corresponding dc shift at the output. A three stage RC ladder filter is employed for removing the sum frequency component from the output. The demodulated output is applied to the comparator to restore the required logic levels.

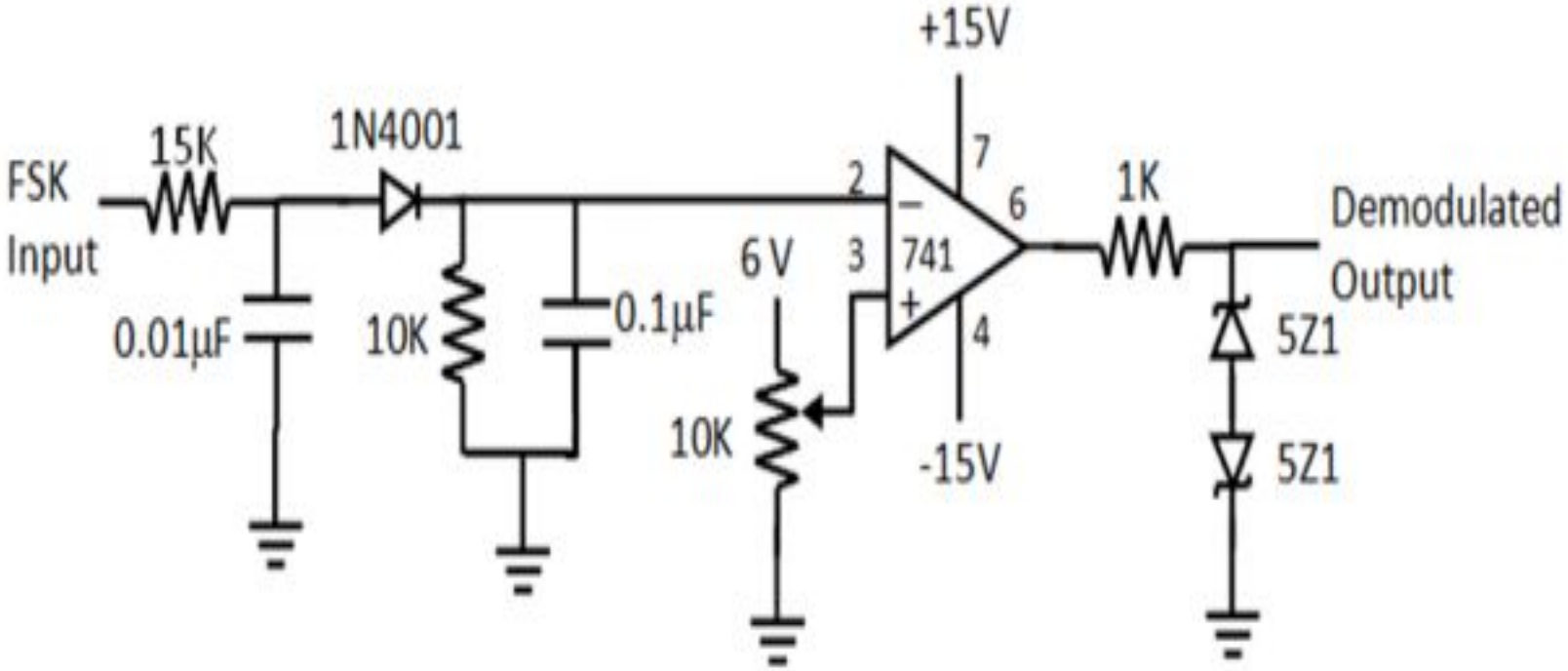
PROCEDURE:

1. Test all the components and probes.
2. Set up the FSK modulator and demodulator circuits on the bread board. Switch on the power supplies.
3. Feed 5V, 100Hz (10Vpp, 100Hz) square wave as the data input. Vary the pot R_C to adjust the output frequencies if needed.
4. Observe both the input and output waveforms on CRO and plot. The waveform of the FSK output will be rectangular in nature for 555 modulator.
5. Apply the FSK output of the modulator to the input of the demodulator, and observe the output. Vary the 10K pot to get the PLL locked with the input signal. Plot the waveforms.

CIRCUIT DIAGRAM:

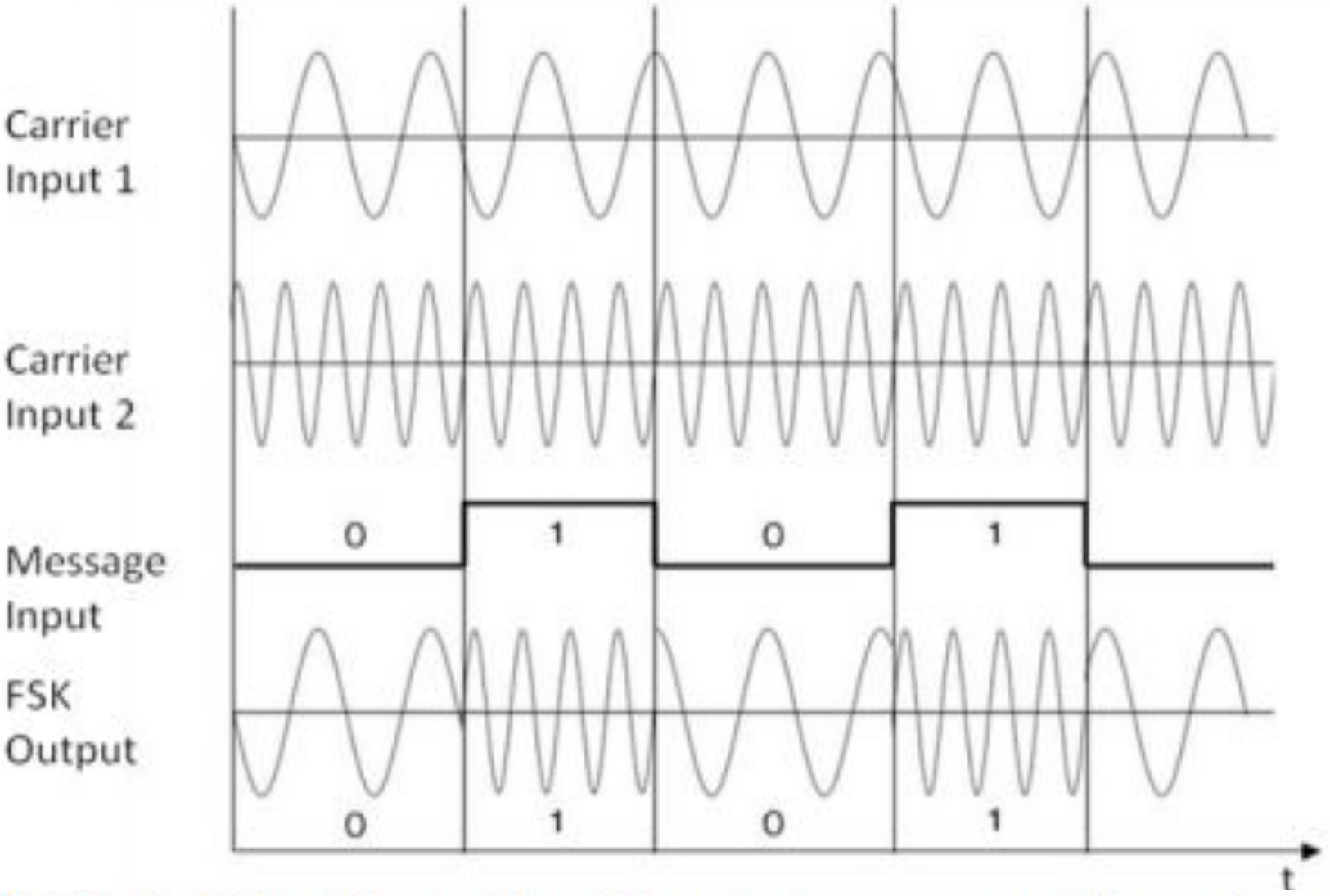


FSK Modulator



FSK Demodulator

WAVEFORM:



RESULT: The FSK modulator and demodulator circuits were set up and the waveforms were plotted.

INFERENCE: Studied the usage of IC 555 as FSK modulator and LM 565 as FSK demodulator.

BINARY PHASE SHIFT KEYING

AIM: To set up Binary Phase Shift Keying (BPSK) modulator and demodulator circuits and to observe the waveforms.

OBJECTIVES: After completing this experiment, the students will be able to a) Set up BPSK modulator and demodulator circuits and b) Identify BPSK waveform.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No.	Item & Specification	Quantity
1	Transistor- SL100, SK100	1No. each
2	Resistor- 10K pot, 100K 1K 10K	1No. each 3No. 7Nos.
3	Capacitor- 0.01μF	1No.
4	IC 741	3No.
5	Diode- 1N4001 Zener Diode- 5Z1	1No. 2Nos.
6	Signal Generator	2Nos.
7	CRO	1No.
8	Power Supply- +/- 15V, 2V	1No.each
9	Bread Board	1No.

THEORY:

Binary Phase Shift Keying (BPSK) is digital transmission scheme where the binary data is transmitted using out of phase signals. During logic '0' a preset number of cycles of a sinusoidal carrier signal is transmitted and during logic '1' the same number of cycles of the carrier signal is transmitted but with 180^{o} phase shift.

Modulator

A simple BPSK modulator circuit using an NPN-PNP transistor pair and an Op amp is shown in figure. The transistors work as switches and the Op amp works as inverting/non-inverting amplifier. The carrier signal is fed to the collectors and the message signal is fed to the bases of the two transistors simultaneously. The emitters of the transistors are grounded. When the message signal is at logic '1' (+5V), the NPN transistor is ON and works as a closed switch. The PNP transistor is OFF and works as an open switch. The Op amp now works as a non-inverting amplifier with the carrier signal fed to its non-inverting input. The carrier signal reaches the output without any phase shift. When the message signal is at logic '0' (-5V), the NPN transistor is OFF and the PNP transistor ON. The Op amp works as an inverting amplifier with the carrier signal fed to its inverting pin. The carrier signal now reaches the output with 180^{o} phase shift. Thus the carrier signal switches its phase as the message signal switches between '0' and '1'. The resulting output is BPSK modulated.

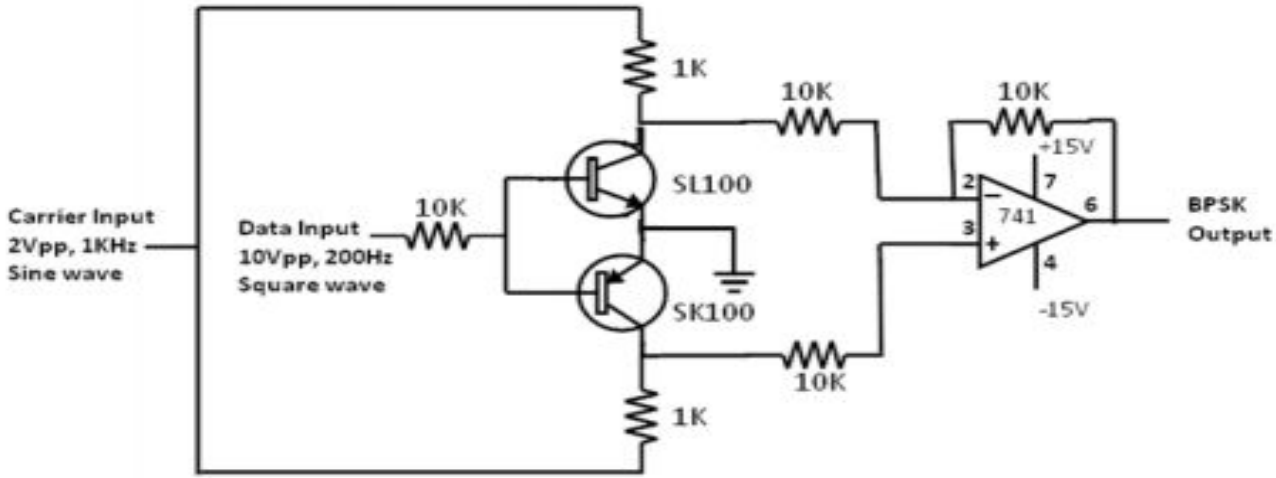
Demodulator

The BPSK demodulator circuit shown in figure consists of an Op Amp difference amplifier, a rectifier, an envelope detector and a comparator. The difference amplifier which is fed with the unmodulated carrier signal at the non-inverting input and the BPSK modulated signal at the inverting input passes only the phase shifted signal to the output. The in phase signals get subtracted completely. The envelope detector removes the carrier content and recovers the data information. The comparator inverts and level limits the signal to regain the correct logic level.

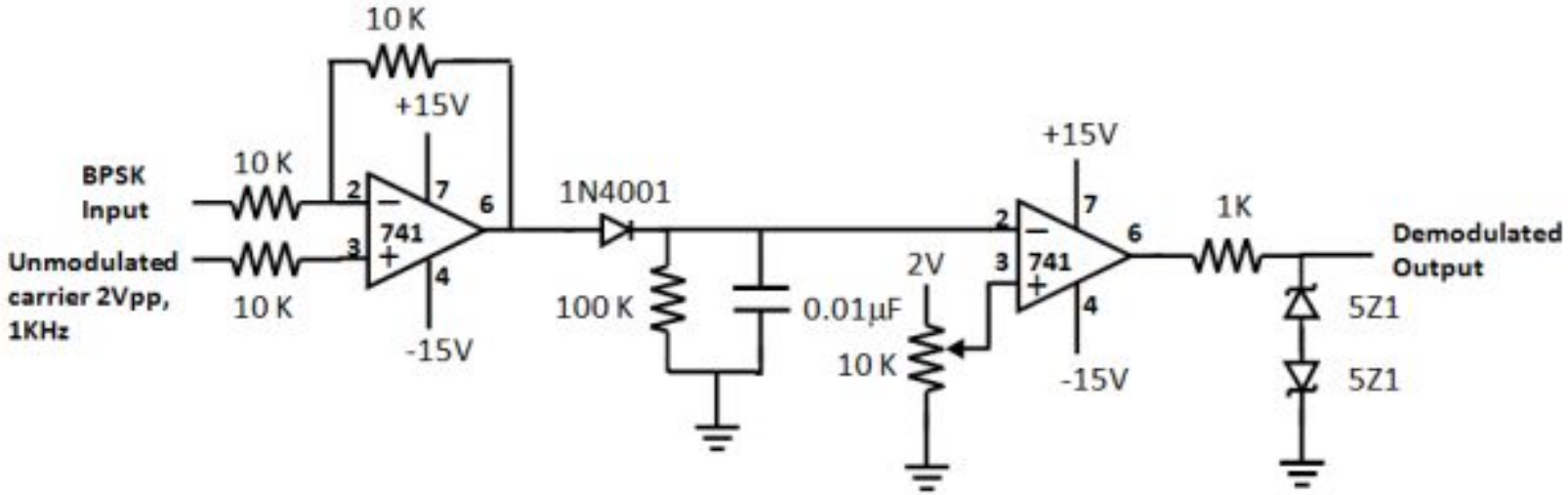
PROCEDURE:

1. Test all the components and probes.
2. Set up the circuits on the bread board as shown in figure.
3. Feed 2Vpp, 1KHz sine wave as carrier input and 10Vpp, 200Hz square wave signal as the message input.
4. Observe the BPSK output on CRO and plot the waveforms.
5. Feed this BPSK modulated signal to the inverting input of the demodulator. Also feed the unmodulated carrier signal (2Vpp, 1KHz) to the non-inverting input.
6. Observe waveforms on CRO. Adjust the potentiometer to obtain the correct output (if needed).
7. Plot the waveforms.

CIRCUIT DIAGRAM:

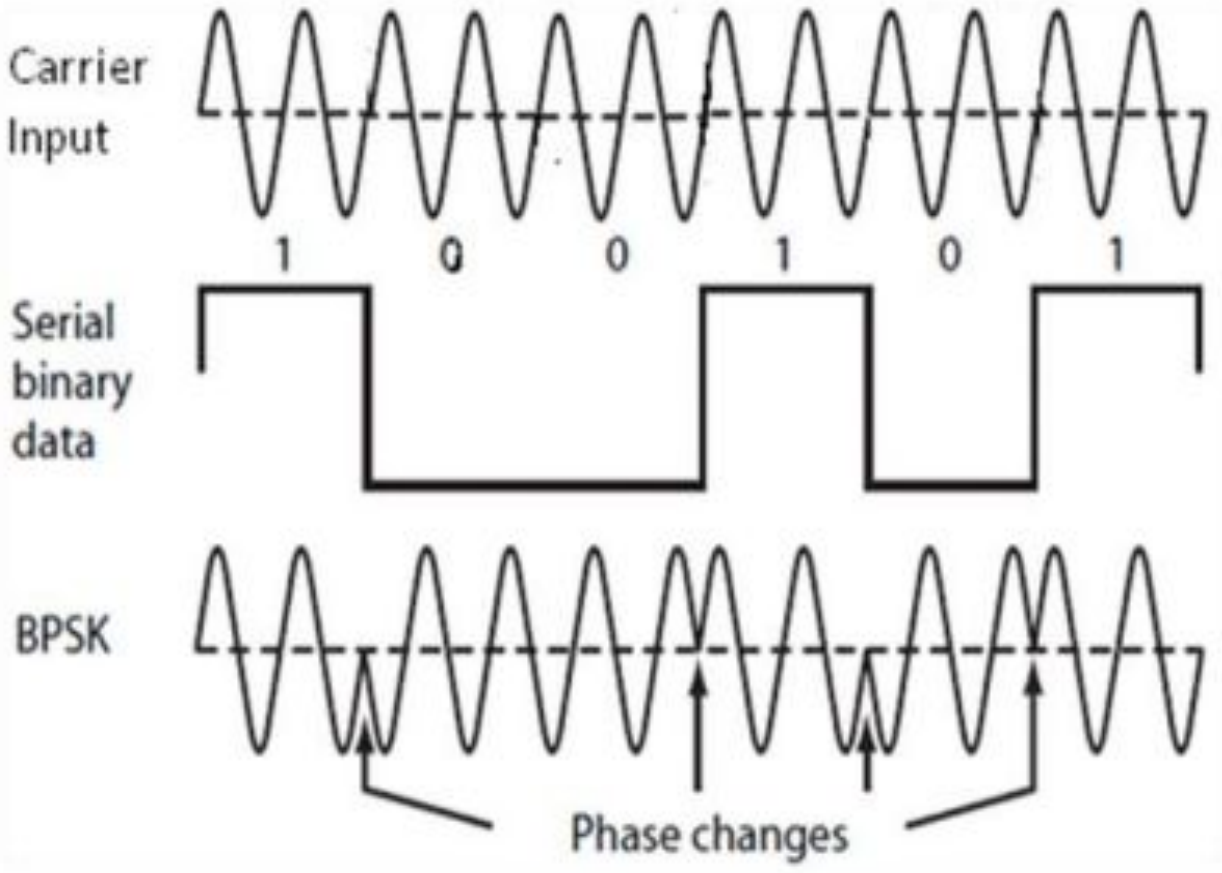


BPSK Modulator



BPSK Demodulator

WAVEFORMS:



RESULT:

BPSK modulator and demodulator circuits were set up and the waveforms were plotted.

INFERENCE: Studied how digital data is transmitted using BPSK.

PRE-EMPHASIS AND DE-EMPHASIS

AIM:

To design and set up pre-emphasis and de-emphasis circuits using Op amp and to plot the gain Vs frequency characteristics.

OBJECTIVES: After completing this experiment, the students will be able to a) design and set up pre-emphasis and de-emphasis circuits and to b) plot the response curve.

COMPONENTS AND EQUIPMENTS REQUIRED:

Sl. No.	Item & Specification	Quantity
1	IC 741	1No.
2	Resistor- 4.7K, 1K, 560Ω	1No.
3	Capacitor- 0.01μF	1No.
4	Signal Generator	1No.
5	CRO	1No.
6	Power Supply- +/- 15V	1No.
7	Bread Board	1No.

THEORY:

In FM Broadcasting, the effect of noise is more intense on higher frequencies than on low frequencies. Therefore, in order to have high signal-to-noise ratio(low noise), the high frequencies are amplified at the transmitter side (pre-emphasis) and for compensation, de-emphasis (decreasing the amplitude of those boosted frequencies) is done at receiver.

The pre-emphasis circuit is actually a high pass filter and de-emphasis circuit a low pass filter. The amount of pre-emphasis and de-emphasis used is defined by the time constant of a simple RC filter circuit. As per European standards 50μS is the time constant. In North America, 75 μS is the standard value. Simple pre-emphasis and de-emphasis circuits using Op Amp are given in the diagram.

DESIGN:

Time constant chosen, T = 50 μS

Therefore the time constant RC = 50 μS

Take C = 0.01μF, then R = 4.7KΩ

For Butterworth filters, Gain A = 1.586

Gain of non-inverting amplifier = 1+Rf/R1

$$1.586 = 1+Rf/R1$$

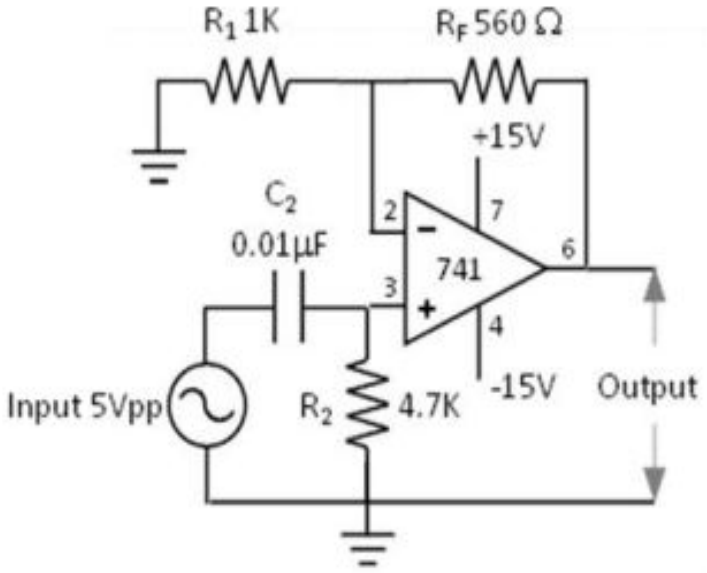
$$Rf/R1 = 0.586$$

Take R1 = 1K, then Rf = 560 Ω

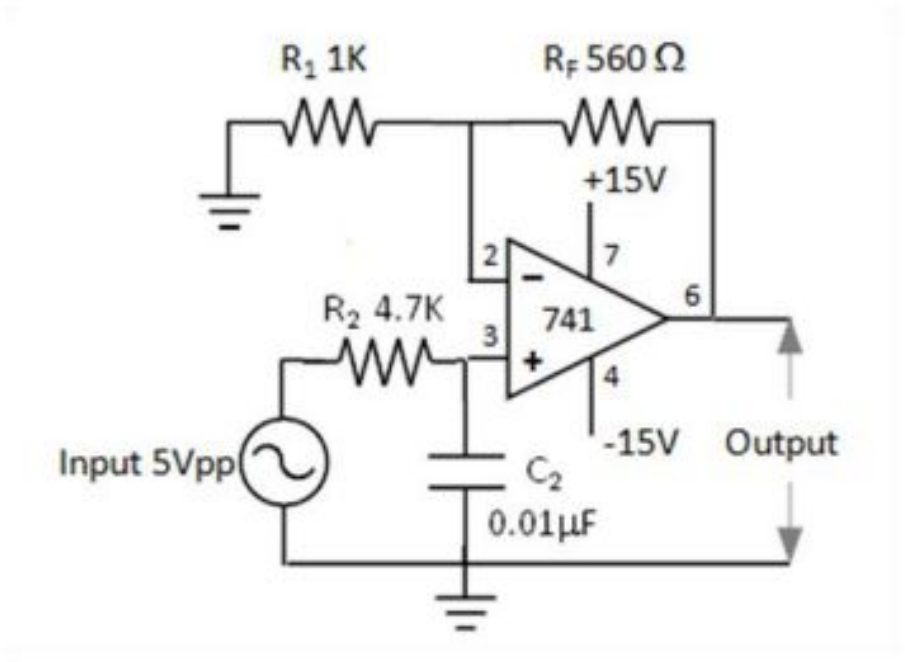
PROCEDURE:

1. Test all the components and probes.
2. Set up the pre- emphasis circuit on a bread board as shown in figure.
3. Feed 5Vpp sine wave as input. Vary the frequency from 50Hz to 3MHz and note down the values of the corresponding output voltage on a tabular column.
4. Plot frequency response on a graph sheet with log f on x-axis and gain in dB on y-axis. Mark the cut-off frequencies corresponding to 3dB points.
5. Repeat the above steps for de-emphasis circuit.

CIRCUIT DIAGRAM:



Pre-emphasis Circuit

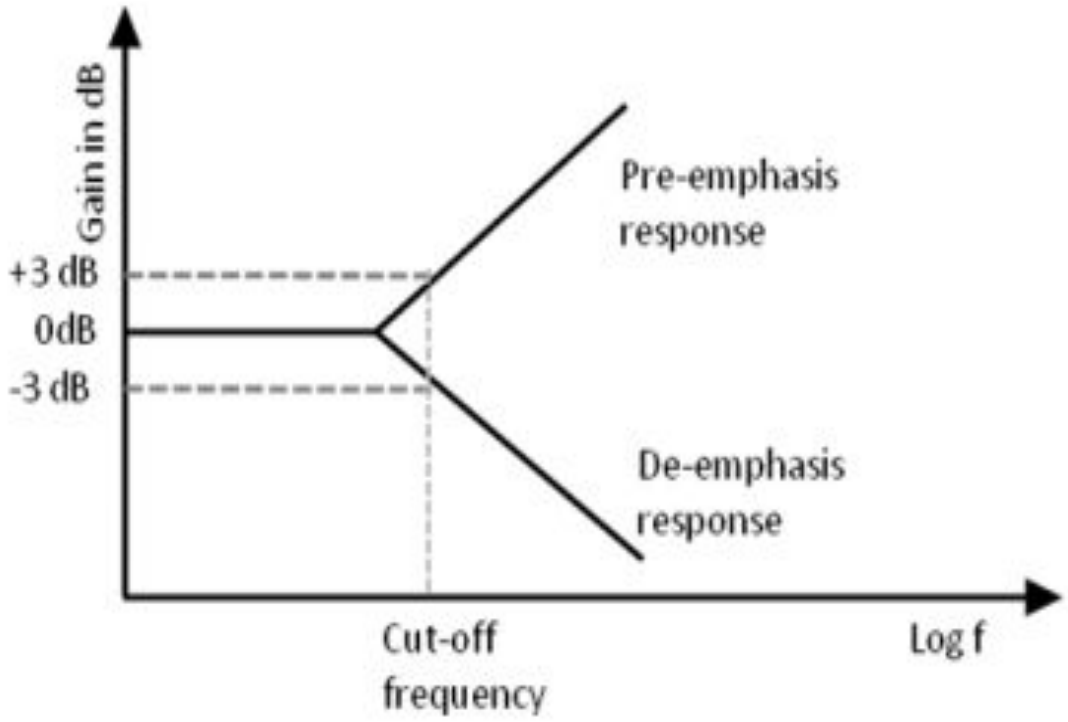


De-emphasis circuit

TABULAR COLUMN:

f (Hz)	Vo	log f	Gain in dB (20logVo/Vi)

FREQUENCY RESPONSE:



RESULT:

Pre-emphasis and de-emphasis circuits were set up and frequency response curves were drawn.

Cut-off frequency (3dB) for pre-emphasis circuit =.....

Cut-off frequency (3dB) for de-emphasis circuit =.....

INFERENCE: Signal to noise ratio at high frequencies can be considerably improved by employing pre-emphasis and de-emphasis.

https://www.youtube.com/watch?v=d2-1ioMaF58

COMMUNICATION LINK SIMULATIONS

AIM:

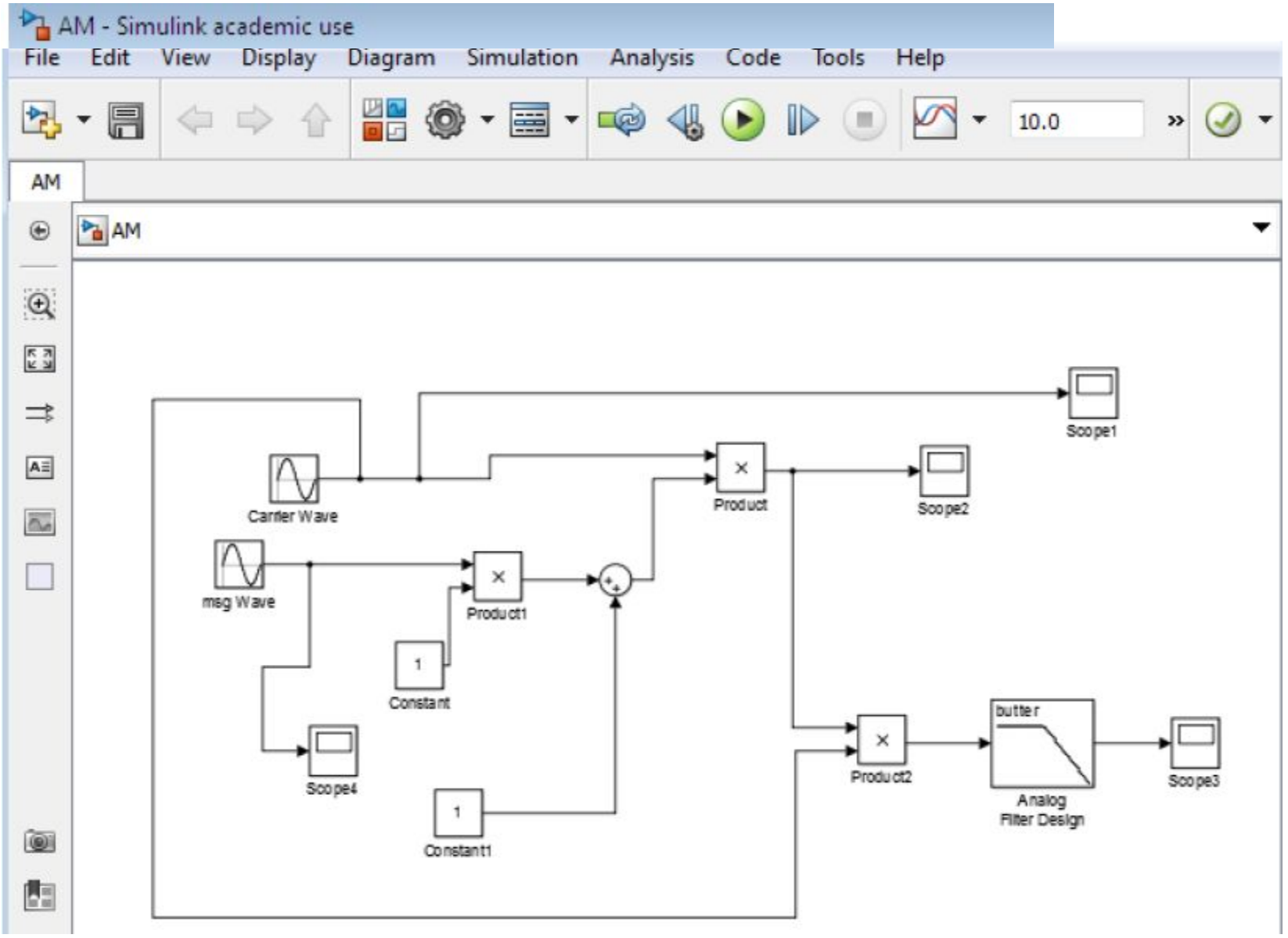
To generate modulation and demodulation of AM, ASK, DM and PAM using Simulink.

APPARATUS REQUIRED:

PC with MATLAB Software with Simulink tool

PROCEDURE:

1. Start simulink section
2. Select file→ New Model in the simulink library to construct a new model
3. Go to simulink library select appropriate module and add to model
4. Connect all the inserted models
5. Set the simulation parameters
6. Run the simulation and observe and save all the plots and values.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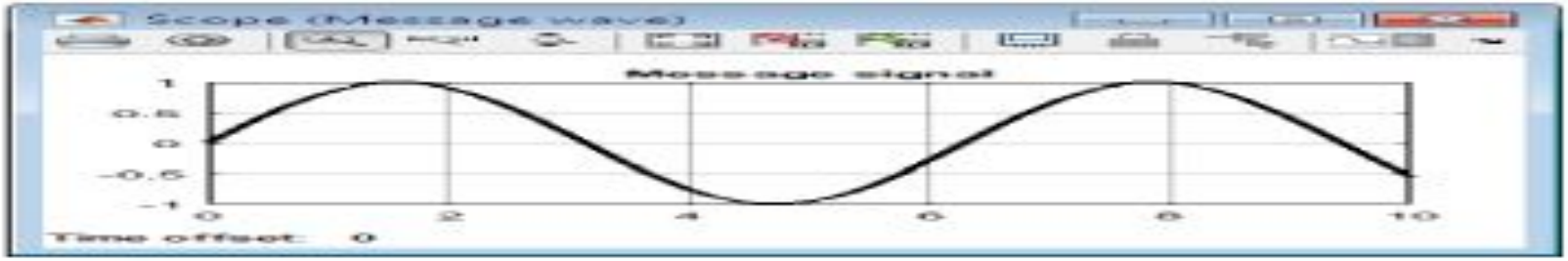
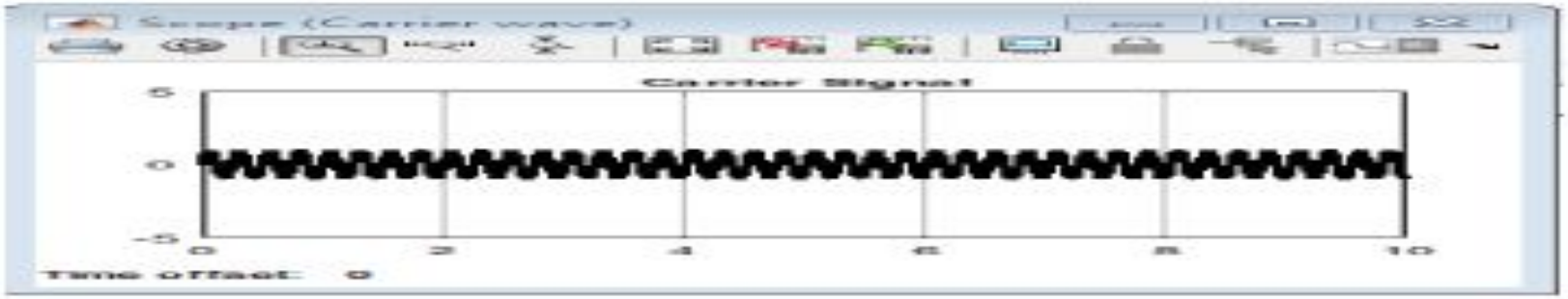
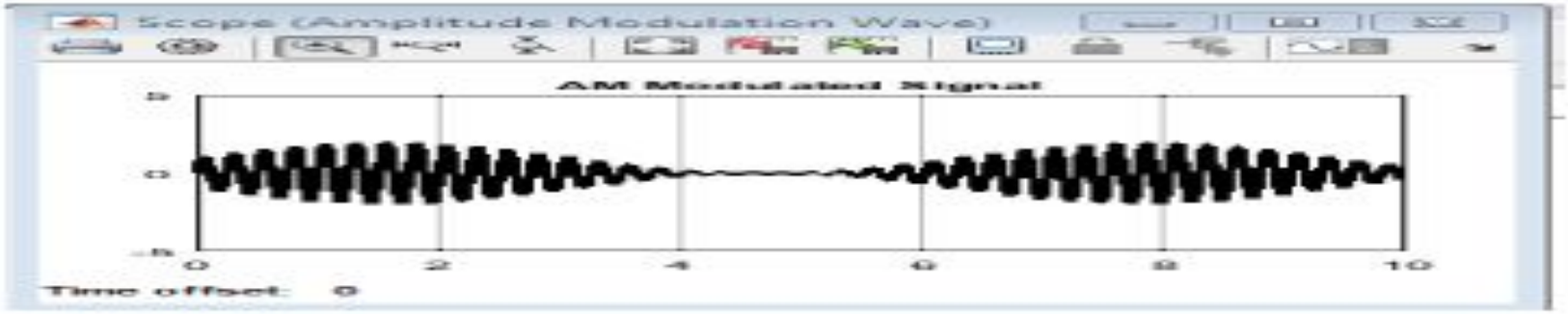
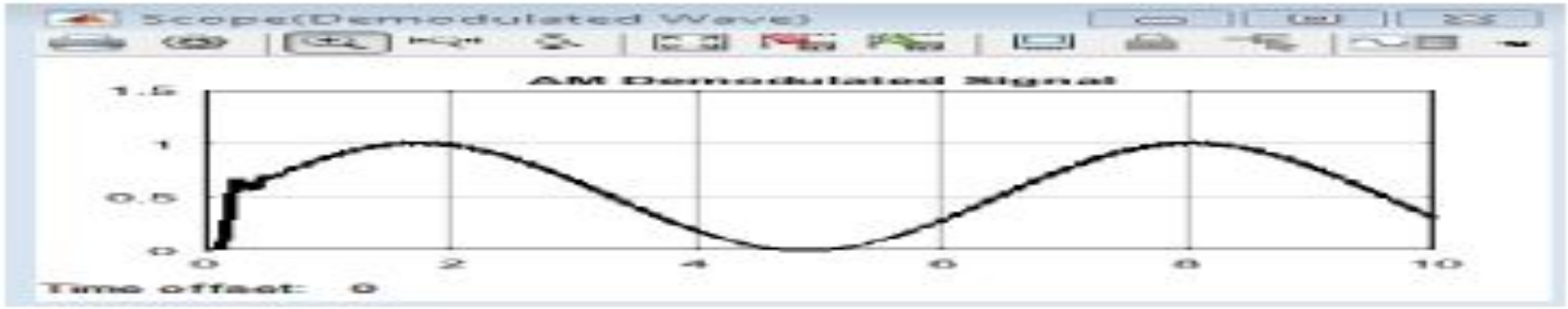
File Edit View Display Diagram Simulation Analysis Code Tools Help
10.0
AM
AM
Carrier Wave
msg Wave
Product
Product1
Product2
Constant
Constant1
Scope1
Scope2
Scope3
Scope4
butter
Analog
Filter Design

OUTPUT (AM)

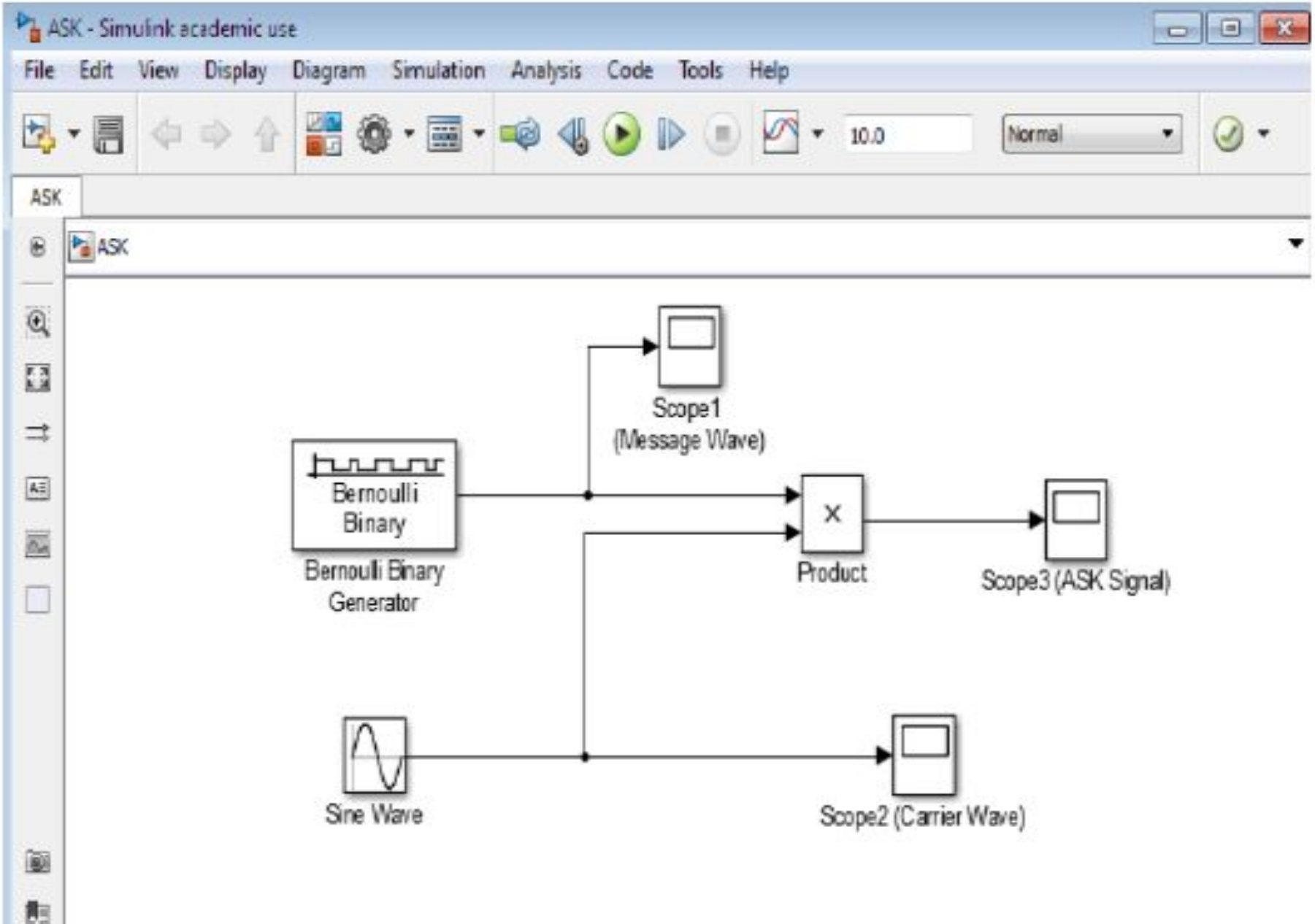

Scope (Message wave)
Message signal
1
0.5
0
−0.5
−1
0
2
4
6
8
10
Time offset: 0


Scope (Carrier wave)
Carrier Signal
5
0
−5
0
2
4
6
8
10
Time offset: 0


Scope (Amplitude Modulation Wave)
AM Modulated Signal
5
0
−5
0
2
4
6
8
10
Time offset: 0


Scope(Demodulated Wave)
AM Demodulated Signal
1.5
1
0.5
0
0
2
4
6
8
10
Time offset: 0

ASK MODULE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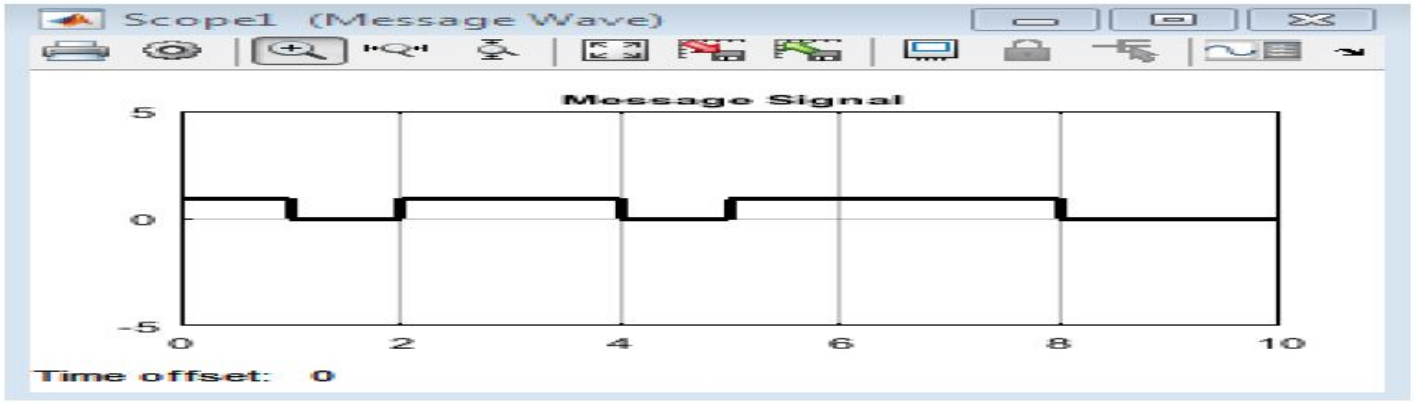
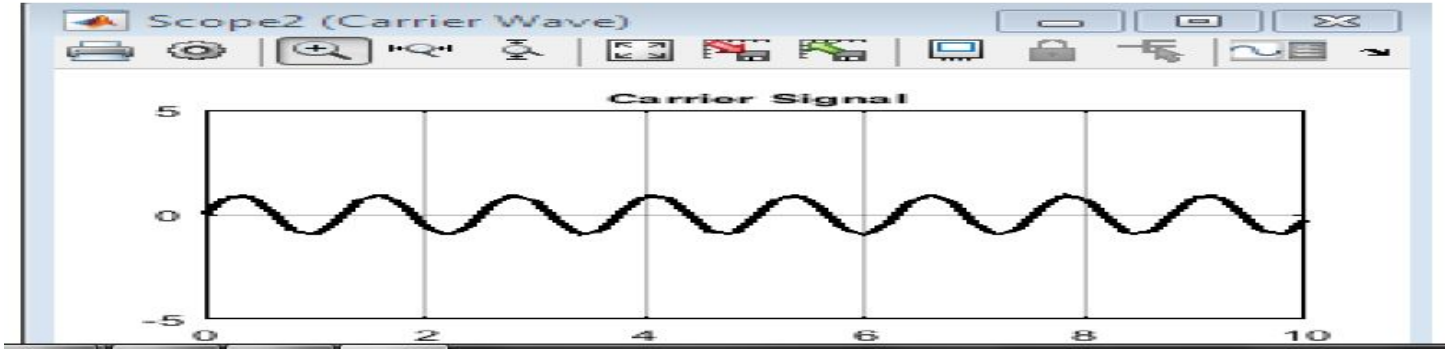
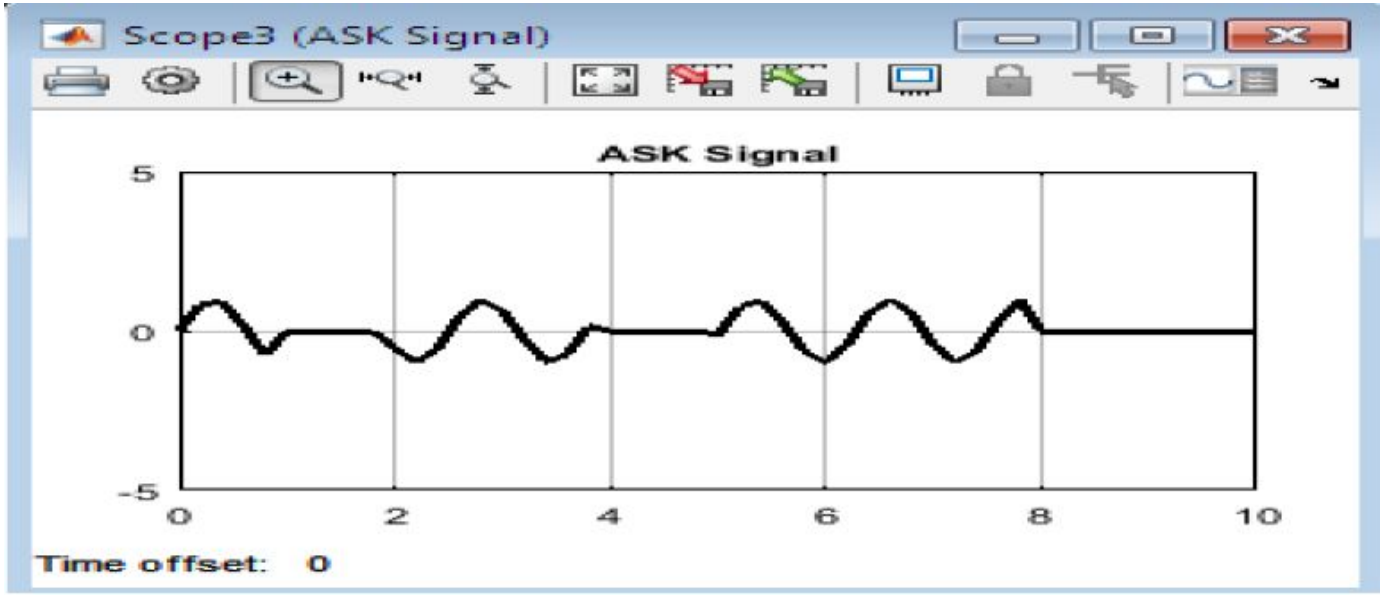
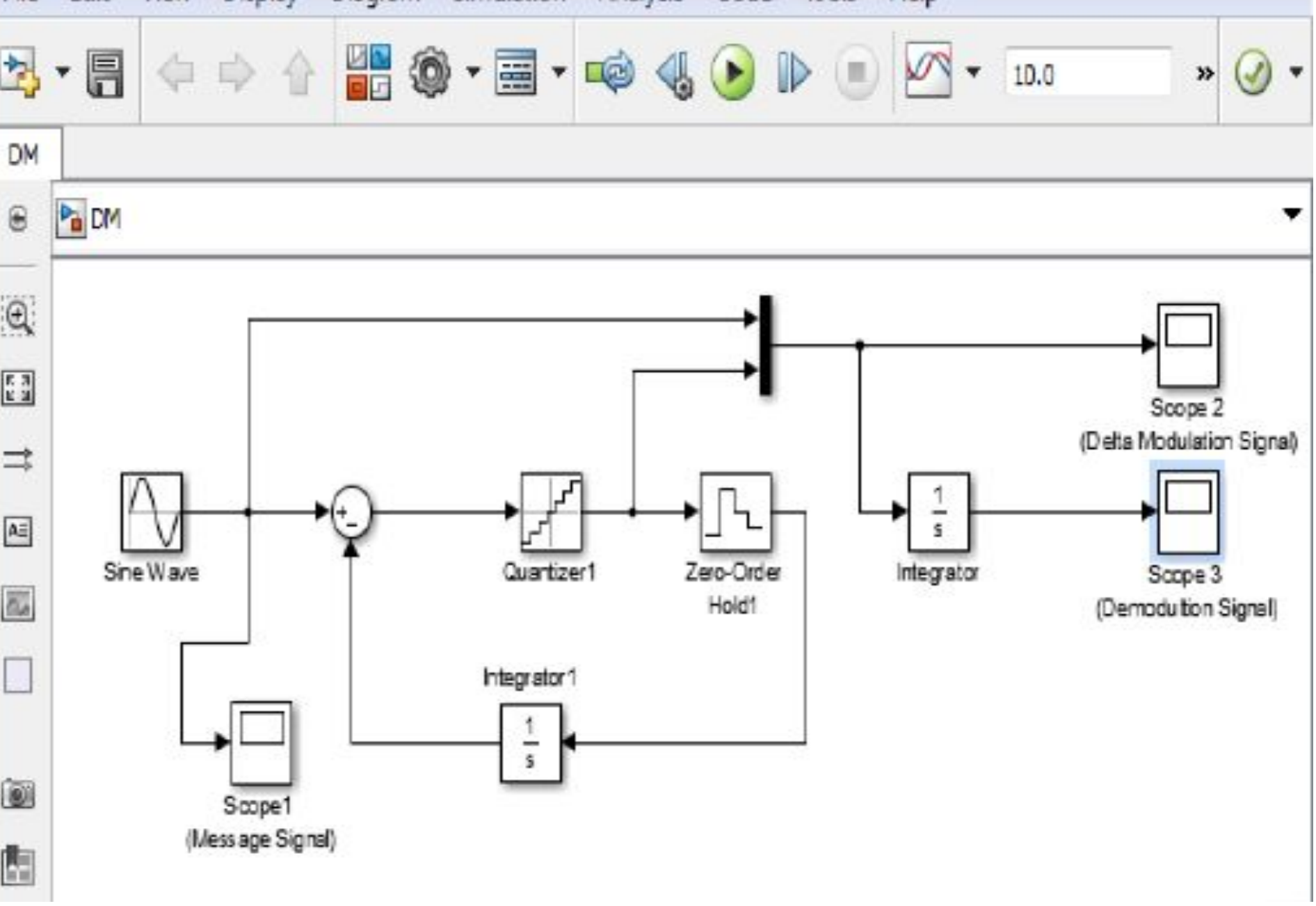
Generator
X
Product
Scope3 (ASK Signal)
Sine Wave
Scope2 (Carrier Wave)

OUTPUT

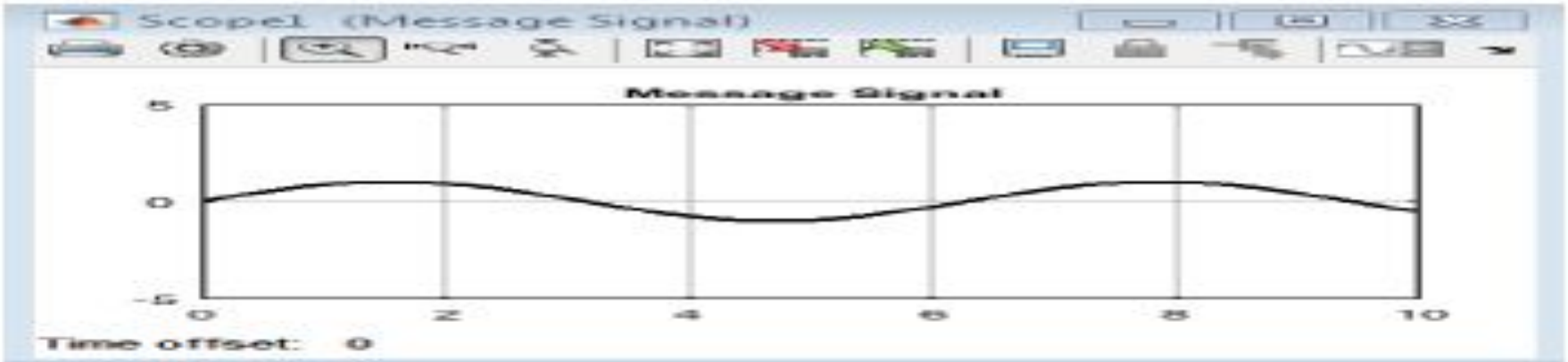

Scope1 (Message Wave)
Message Signal
5
0
-5
0
2
4
6
8
10
Time offset: 0

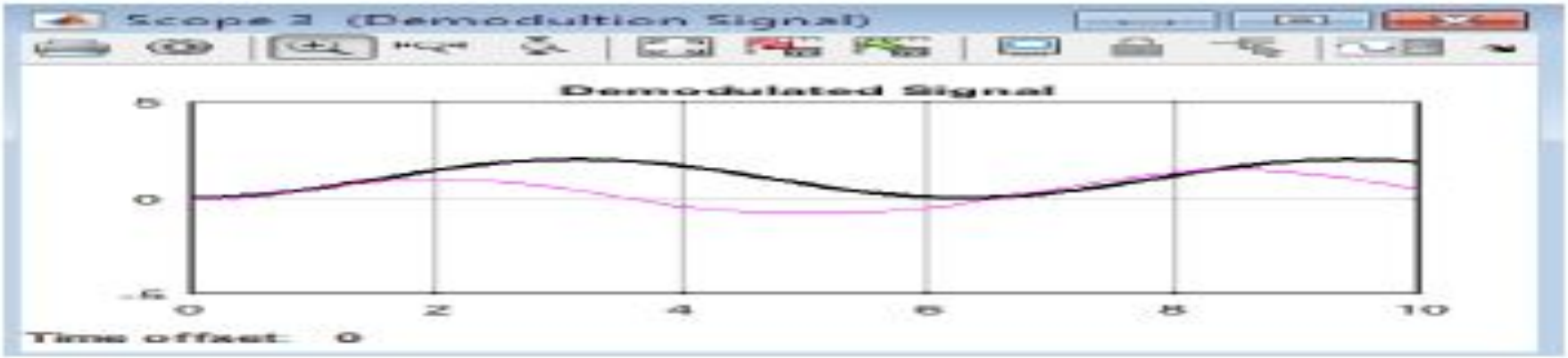

Scope2 (Carrier Wave)
Carrier Signal
5
0
-5
0
2
4
6
8
10

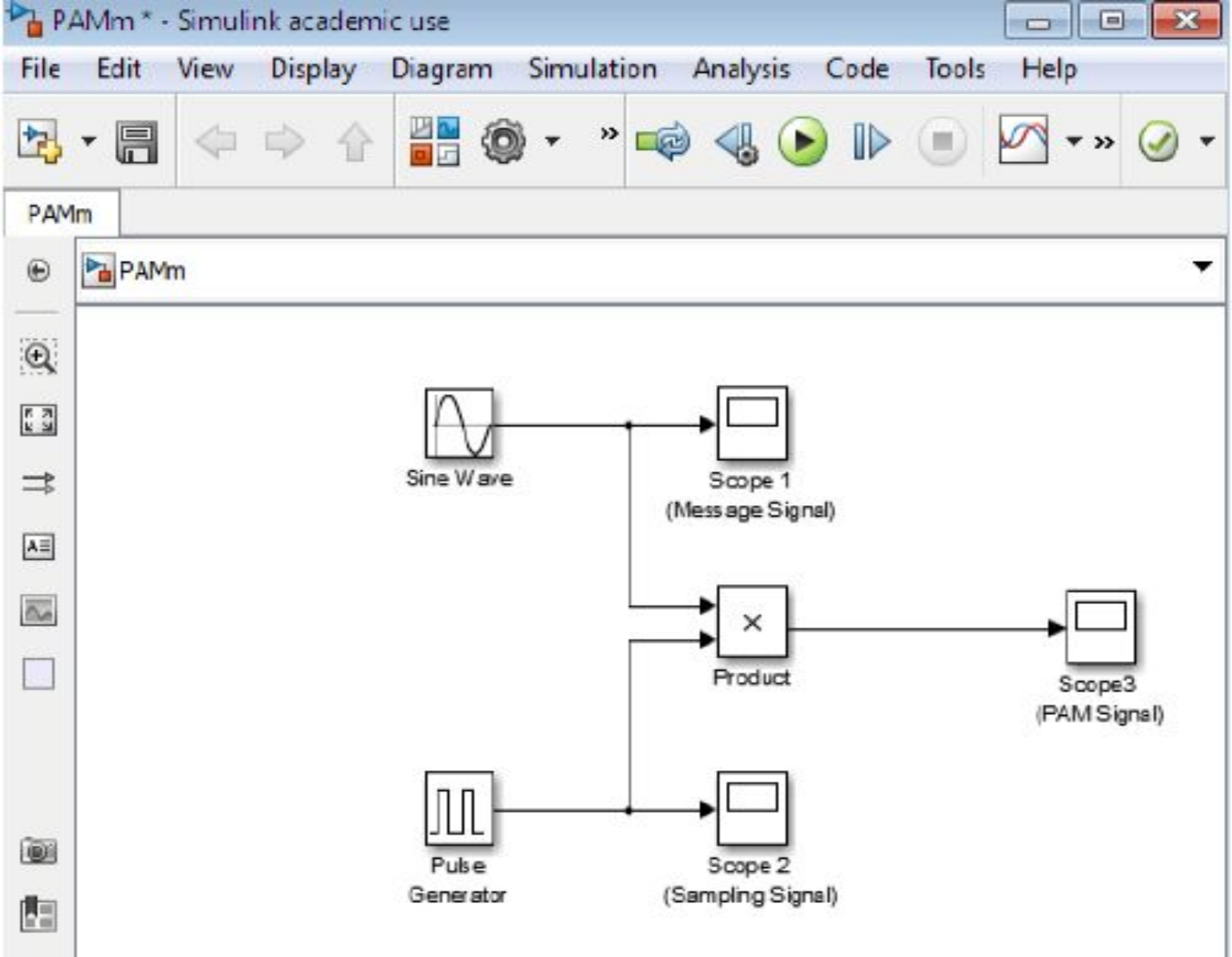

Scope3 (ASK Signal)
ASK Signal
5
0
-5
0
2
4
6
8
10
Time offset: 0


10.0
DM
DM
Sine Wave
Quantizer1
Zero-Order
Hold1
Integrator
Scope 2
(Delta Modulation Signal)
Scope 3
(Demodulation Signal)
Integrator1
Scope1
(Message Signal)

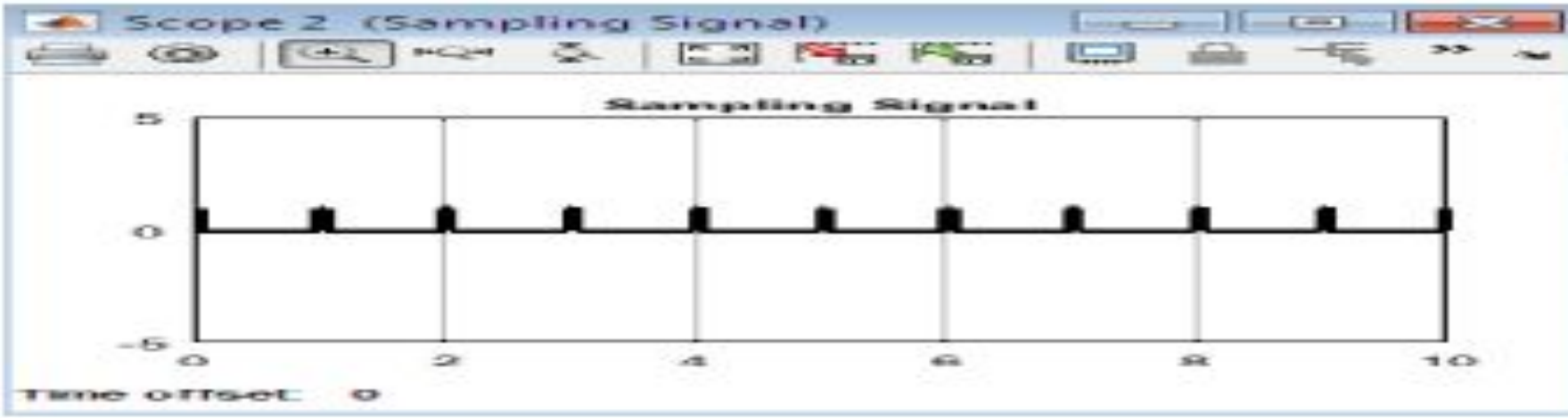
SIMULATION OUTPUT

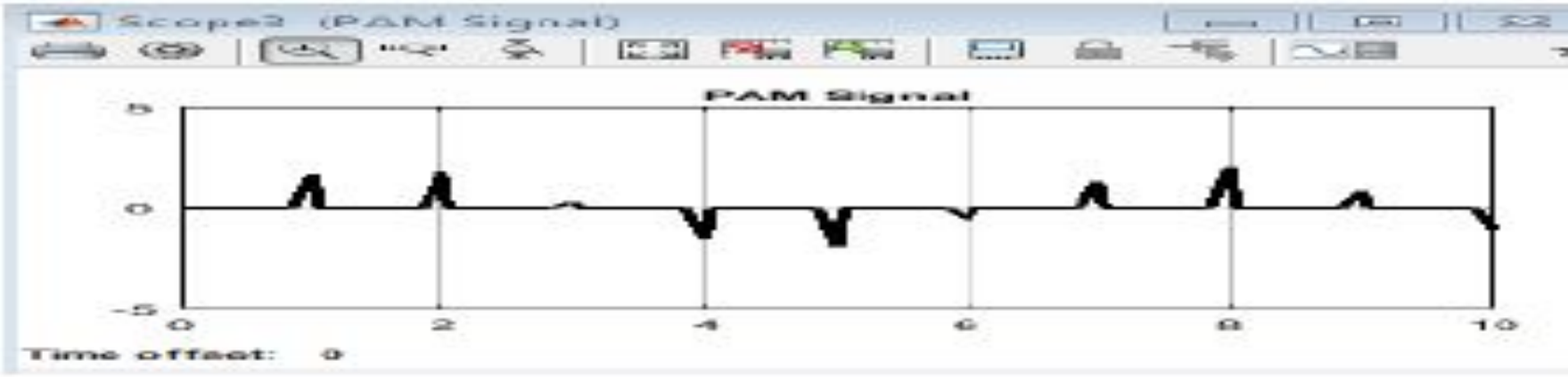




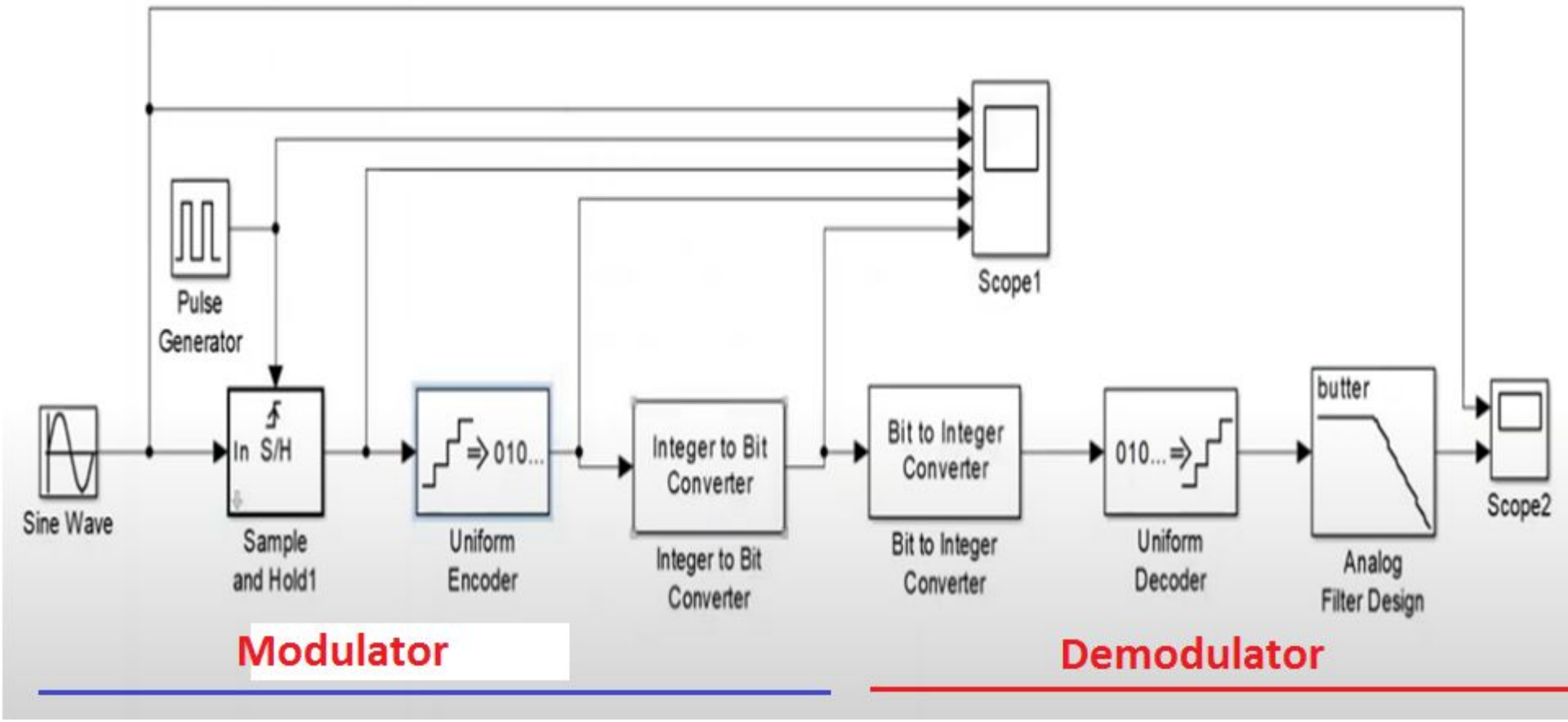

PAMm * - Simulink academic use
File Edit View Display Diagram Simulation Analysis Code Tools Help
PAMm
PAMm
Sine Wave
Scope 1
(Message Signal)
Product
Scope3
(PAM Signal)
Pulse
Generator
Scope 2
(Sampling Signal)

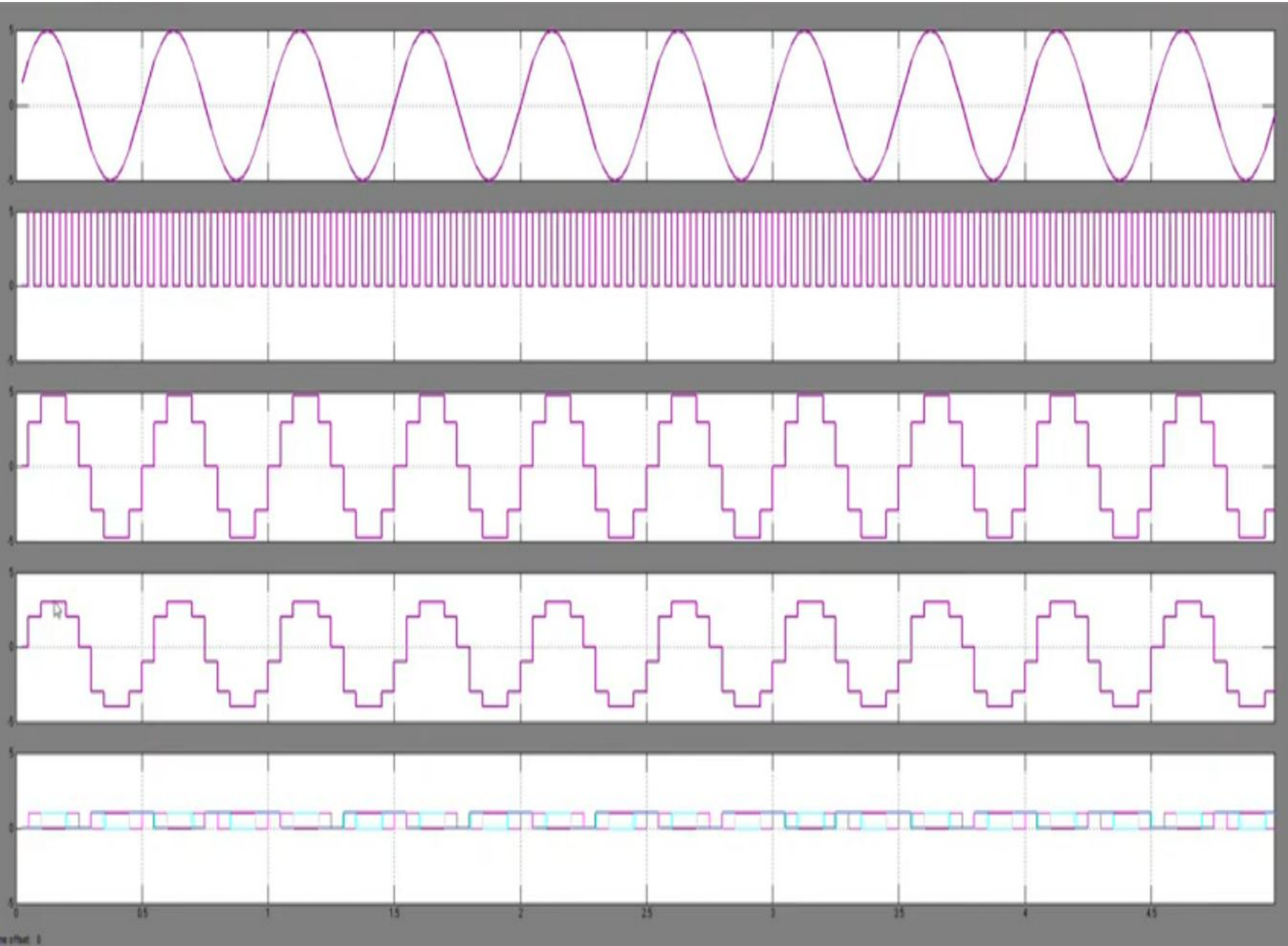

Scope 1 (Meccage Signal)
Message Signal
5
0
-5
0
2
4
6
8
10
Time offset: 0


Scope 2 (Sampling Signal)
Sampling Signal
5
0
-5
0
2
4
6
8
10
Time offset: 0


Scope2 (PAM Signal)
PAM Signal
5
0
-5
0
2
4
6
8
10
Time offset: 0

PCM Modulation / Demodulation using Simulink
https://www.youtube.com/watch?v=cp40kS1nMUI




5
0
-5
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5

Delta Modulation and Demodulation using Simulink®

Aim: To build and analyse Delta modulation scheme using Simulink ® software and demodulate the DM signal to get back the original message signal.

Software used: Simulink ®

Introduction: A delta modulation (DM or Δ-modulation) is an analog-to-digital and digital-to-analog signal conversion technique used for transmission of voice information where quality is not of primary importance. DM is the simplest form of differential pulse-code modulation (DPCM) where the difference between successive samples are encoded into n-bit data streams. In delta modulation, the transmitted data are reduced to a 1-bit data stream. Its main features are:

- The analog signal *x(t)* is approximated with a series of segments.
- Each segment of the approximated signal is compared to the preceding bits and the successive bits are determined by this comparison.
- Only the change of information is sent, that is, only an increase or decrease of the signal amplitude from the previous sample is sent whereas a no-change condition causes the modulated signal to remain at the same 0 or 1 state of the previous sample.

To achieve high signal-to-noise ratio, delta modulation must use oversampling techniques, that is, the analog signal is sampled at a rate several times higher than the Nyquist rate.

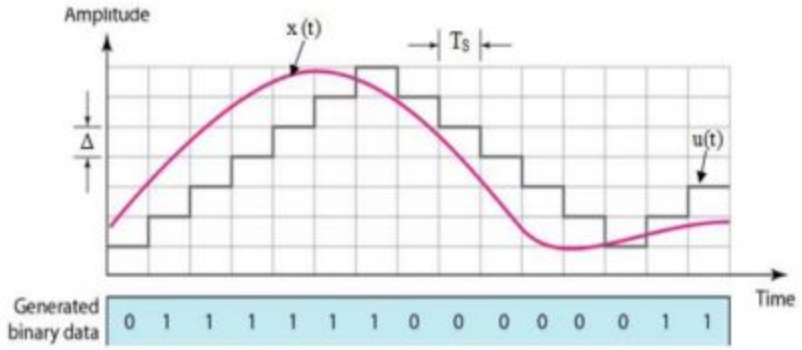


Figure 1: Delta modulation

$x(t)$ represents the analog signal and $x_q(t)$ represents the staircase approximation. Following discrete relations explain the construcion of the staircase waveform which forms the basis of delta modulation.

$$e(nT_s) = x_q(nT_s) - x_q(nT_s - T_s)$$

$$e_q(nT_s) = \delta \, sgn[e_q(nT_s)]$$

$$x_q(nT_s) = x_q(nT_s - T_s) + e_q(nT_s)$$

Where T_s is the sampling instant, $e(nT_s)$ is the error signal and $e_q(nT_s)$ is the quantized version of error signal.

Block Diagram:

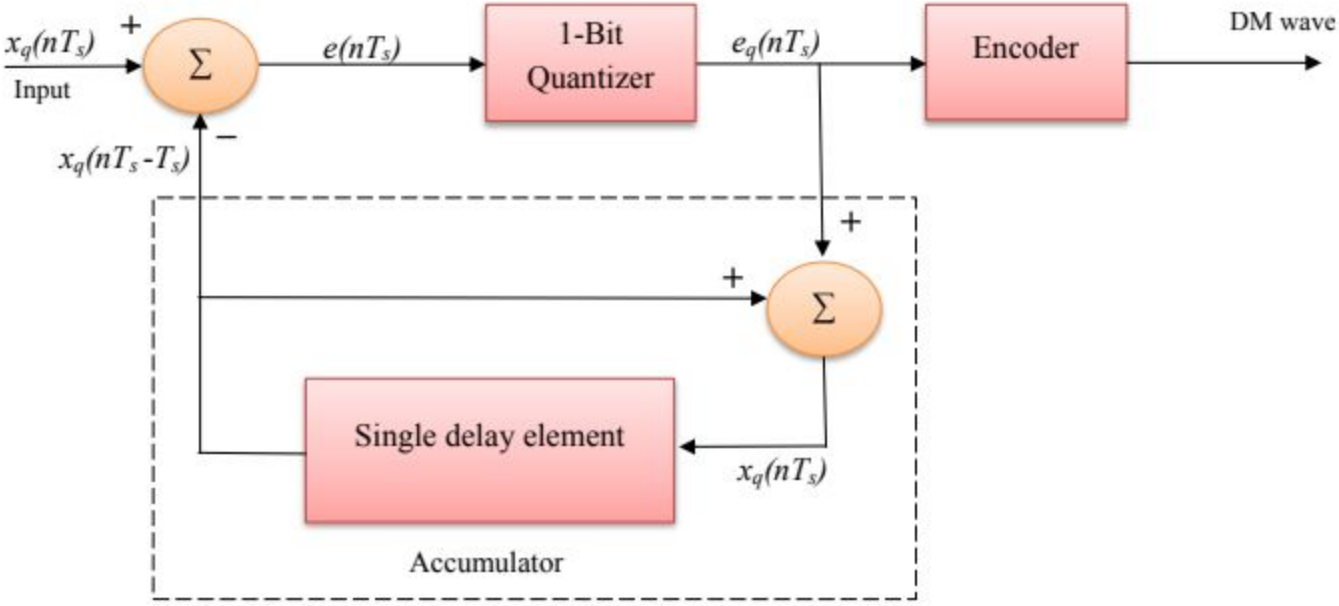


Figure 2: Block diagram of the DM transmitter

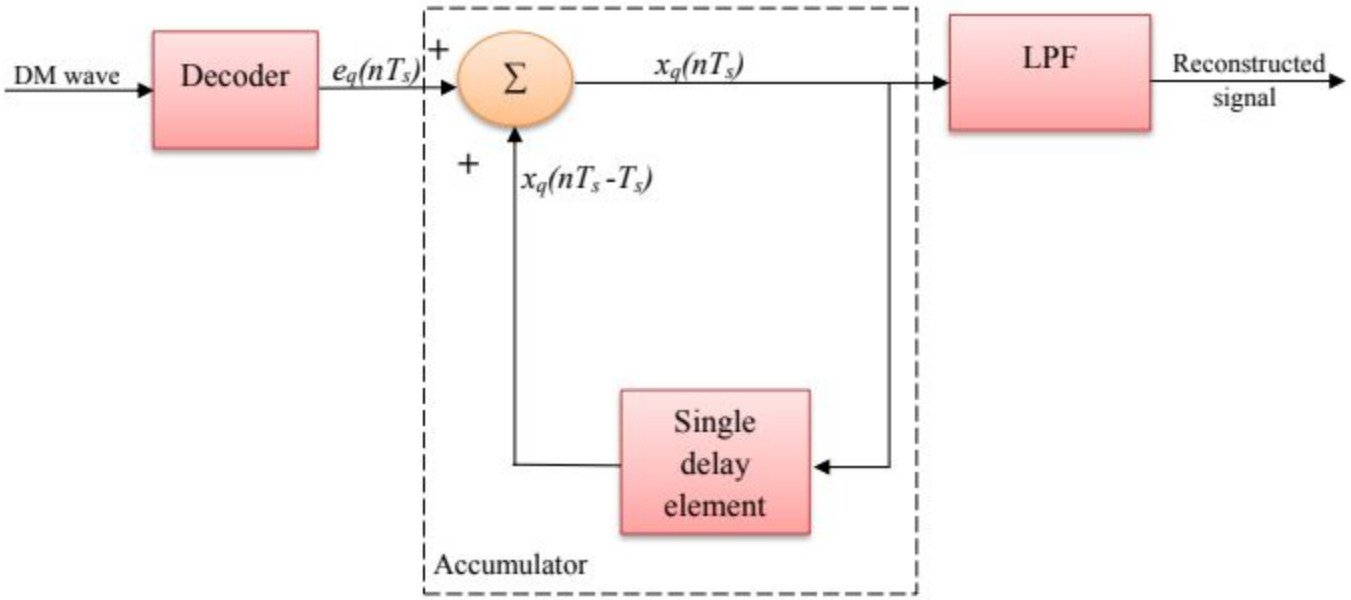


Figure 3: Block diagram of the DM receiver

Simulink model of Delta modulation:

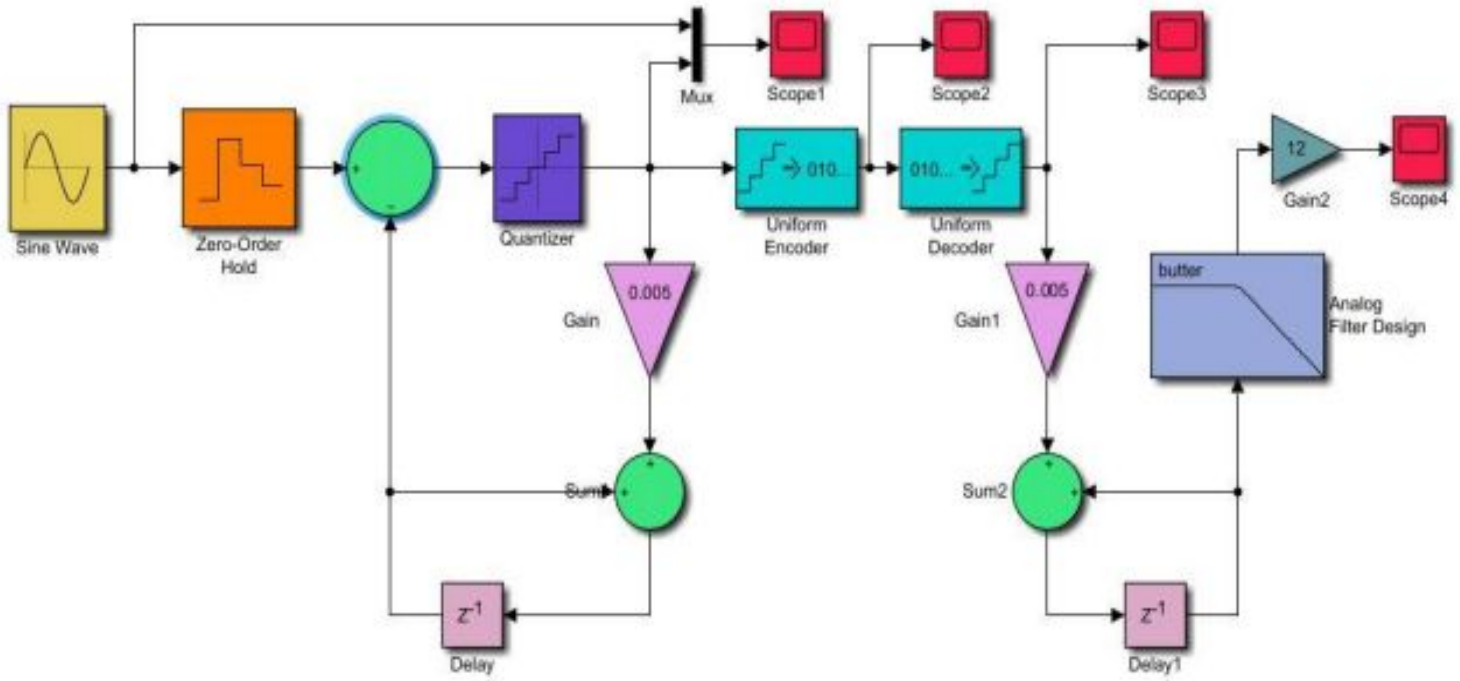


Figure 4: Simulink Model of delta modulation

Description:

- Initially an analog sine wave of frequency 80Hz is sampled at a frequency of 8000Hz using the block "Zero-Order Hold" as shown in Figure 4.
- The DM transmitter involves a comparator, a quantizer and an accumulator as shown in Figure-1 and the same is implemented in the model shown in Figure 4. The block "Gain" with the value 0.005 specifies the step size of quantization.
- The comparator gives difference between input signal and the delayed signal called error signal $e(nT_s)$.
- The output of the quantizer is one of the two levels depending on the output of the comparator.
- Output of the quantizer is applied to the accumulator and accumulator constructs staircase waveform that keeps track of input signal as close as possible.
- A uniform 8-bit encoder with peak value 2, is used to encode the quantized data. Similarly, an 8-bit decoder with peak value 2, is used to decode the encoded data at receiver side.
- In demodulator section, the staircase approximation is reconstructed by passing the error sequence of positive and negative pulses at the decoder output through an accumulator.
- An LPF (Low pass filter) is used to remove step variations and to get smooth reconstructed message signal. The LPF constructed is an analog Butterworth LPF of 8^{th} order.
- Also, the lowpass filter does a favor in rejecting the out of band quantizing noise in the high frequency staircase approximation.
- A variable gain block at the end of the receiver section is used to amplify the signal since the amplitude of the received signal is small compared to the message signal.

Output Waveforms:

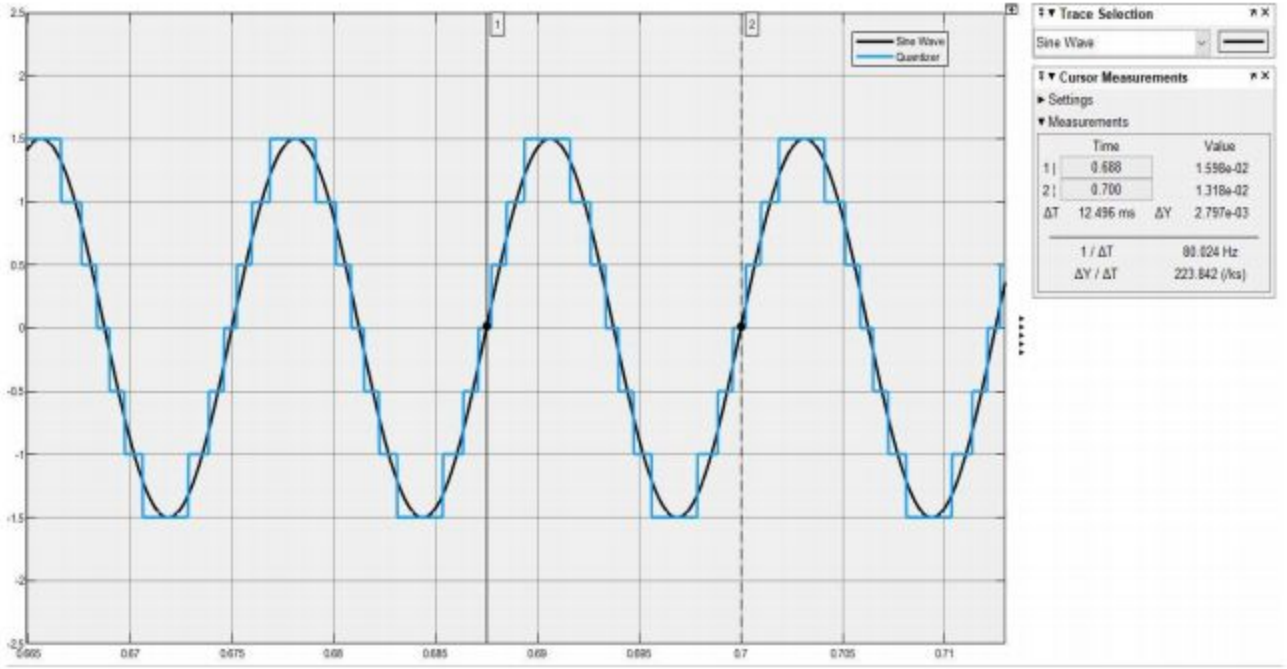


Figure 5: Waveform consisting of message signal and DM signal