DSD LAB

Week 7 Assignment Submission

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Batch B1

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1. Design and simulate the following counters

a) 4 bit synchronous up counter

Verilog code:

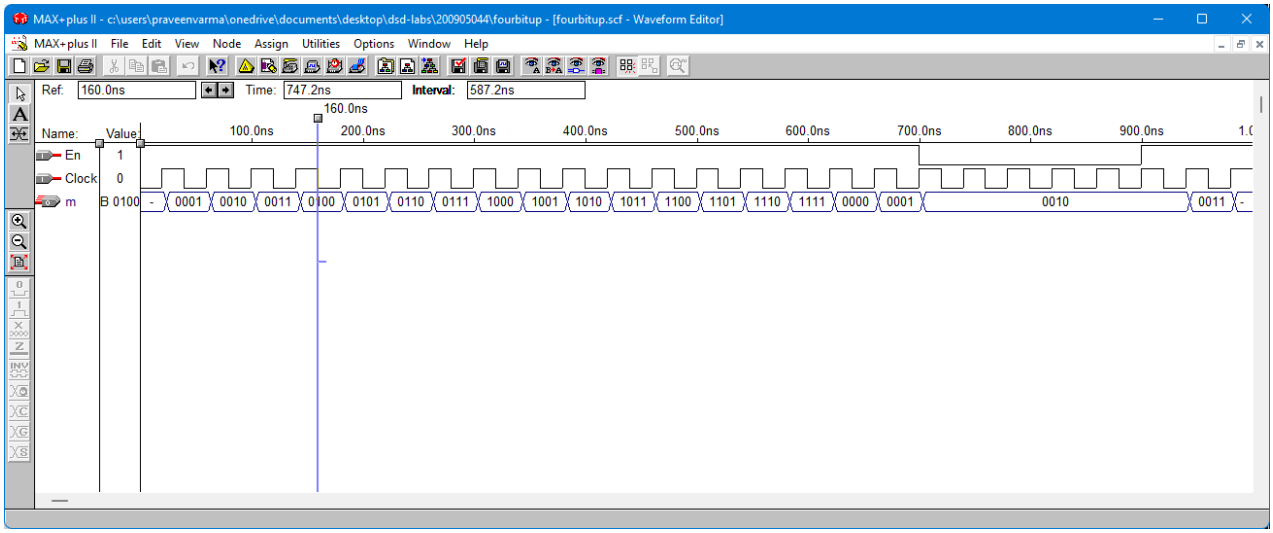
```
module fourbitup(m,Clock,En);
input En;
input Clock;
output [3:0]m;
trial stage1(En,Clock,m[0]);
trial stage2(En&m[0],Clock,m[1]);
trial stage3(En&m[0]&m[1],Clock,m[2]);
trial stage4(En&m[0]&m[1]&m[2],Clock,m[3]);
endmodule



module trial(T,Clock,Q);
input T,Clock;
output Q;
reg Q;
always@(posedge Clock)
```

if(T)

Q<=~Q;

endmodule

Output Waveform:



b) 3 bit synchronous up/down counter with a control input up/$\overline{down}$. If up/$\overline{down}$ = 1, then the circuit should behave as an up counter. If up/$\overline{down}$ = 0, then the circuit should behave as a down counter.

Verilog code:

module threebitupdown(clk,UD,Q);

input UD;

input clk;

output [2:0] Q;

wire control;

trial stage1(1,clk,Q[0]);

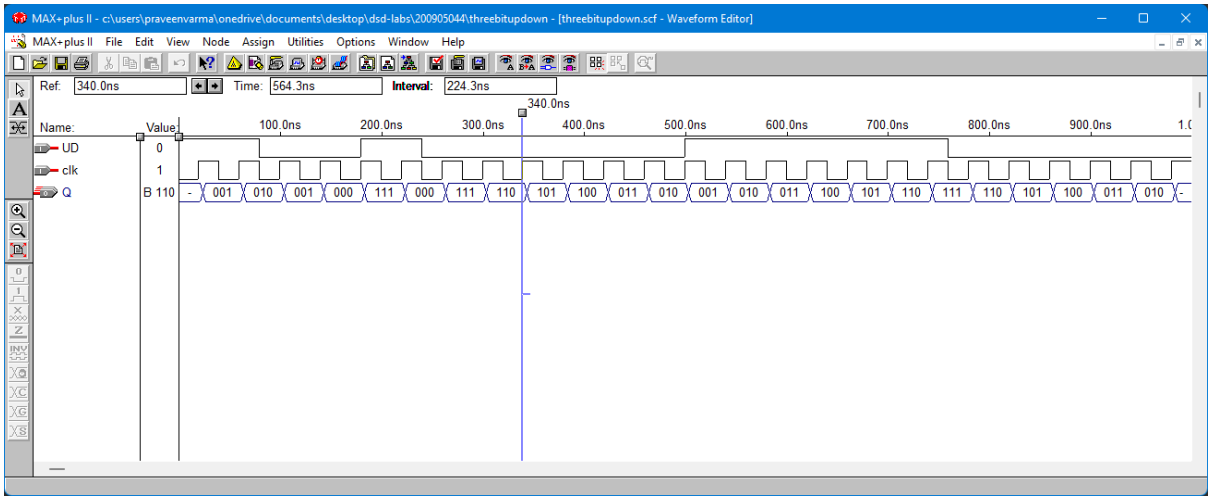
trial stage2(UD & Q[0] | (~UD & ~Q[0]),clk,Q[1]);

trial stage3(UD & Q[0] & Q[1] | (~UD & ~Q[0] & ~Q[1]),clk,Q[2]);

endmodule

```
module trial(T,clock,Q);
input T,clock;
output Q;
reg Q;
always@ (posedge clock)
if(T)
Q <= ~Q;
endmodule
```

Output waveform:



THANK YOU!