DSD LAB

WEEK2- ASSIGNMENT SUBMISSION

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SECTION B

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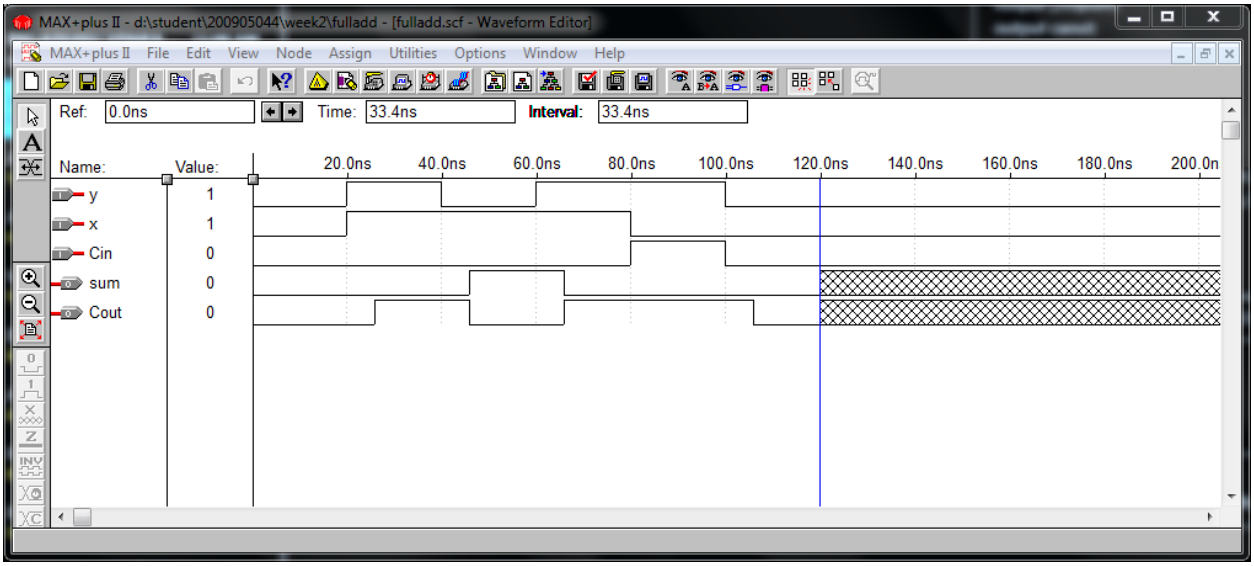
Write behavioral Verilog code to implement the following and simulate:

1. Full adder

Verilog code:

```
module fulladd(Cin,x,y,sum,Cout);
input Cin,x,y;
output sum,Cout;
assign sum = x^y^Cin;
assign Cout = (x&y)|(x&Cin)|(y&Cin);
endmodule
```

Output waveform:



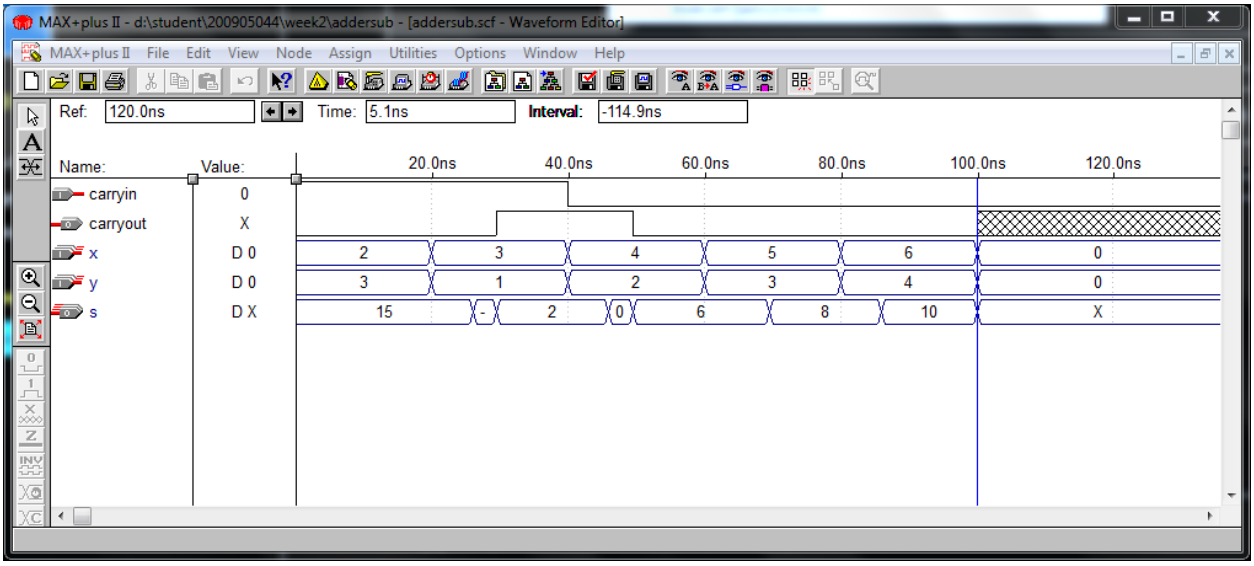
2. Four-bit adder/ subtractor

Verilog code:

```
module full_adder(Cin,x,y,s,Cout);
input Cin,x,y;
output s,Cout;
assign s = x^y^Cin;
assign Cout = (x&y)|(x&Cin)|(y&Cin);
endmodule
```

```
module addersub(carryin,x,y,s,carryout);
input carryin;
input[3:0] x,y;
output[3:0] s;
output carryout;
wire[3:1] C;
full_adder stage0(carryin,x[0],y[0]^carryin,s[0],C[1]);
full_adder stage1(C[1],x[1],y[1]^carryin,s[1],C[2]);
full_adder stage2(C[2],x[2],y[2]^carryin,s[2],C[3]);
full_adder stage3(C[3],x[3],y[3]^carryin,s[3],carryout);
endmodule
```

Output waveform:



3. Single-digit BCD adder using a four-bit adder(s).

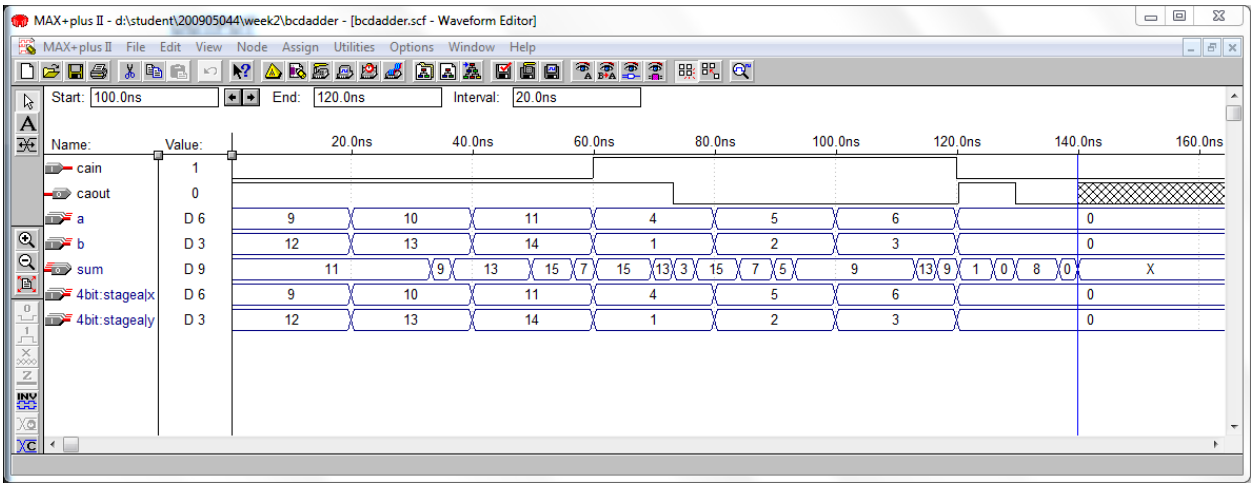
Verilog code:

```
module fulladd(Cin,x,y,s,Cout);
input Cin,x,y;
output s,Cout;
assign s = x ^ y ^ Cin;
assign Cout = (x & y) | (x & Cin) | (y & Cin);
endmodule

module adder4bit(Cin,x,y,s,Cout);
input Cin;
input [3:0]x;
input [3:0]y;
output [3:0]s;
output Cout;
wire [3:1]c;
fulladd stage0(Cin,x[0],y[0],s[0],c[1]);
fulladd stage1(c[1],x[1],y[1],s[1],c[2]);
fulladd stage2(c[2],x[2],y[2],s[2],c[3]);
fulladd stage3(c[3],x[3],y[3],s[3],Cout);
endmodule

module bcdadder(cain,a,b,sum,caout);
input [3:0] a,b;
input cain;
output [3:0]sum;
output caout;
wire [3:0]z;
wire m,k;
wire [3:0]h;
wire j;
adder4bit stagea(cain,a,b,z,m);
assign k = (m|(z[3] & z[2])|(z[3] & z[1]));
assign h[0] = 0, h[1] = k, h[2] = k, h[3] = 0;
adder4bit stageb(cain,z,h,sum,j);
assign caout = m | j;
endmodule
```

Output waveform:


MAX+plus II - d:\student\200905044\week2\bcdadder - [bcdadder.scf - Waveform Editor]
MAX+plus II File Edit View Node Assign Utilities Options Window Help
Start: 100.0ns
End: 120.0ns
Interval: 20.0ns
Name:
Value:
20.0ns
40.0ns
60.0ns
80.0ns
100.0ns
120.0ns
140.0ns
160.0ns
cain 1
caout 0
a D 6 9 10 11 4 5 6 0
b D 3 12 13 14 1 2 3 0
sum D 9 11 9 13 15 7 15 13 3 15 7 5 9 13 9 1 0 8 0 X
4bit:stageax D 6 9 10 11 4 5 6 0
4bit:stageay D 3 12 13 14 1 2 3 0

Thank you!