DSD LAB

WEEK1- ASSIGNMENT SUBMISSION

SWAMIRAJU SATYA PRAVEEN VARMA

200905044

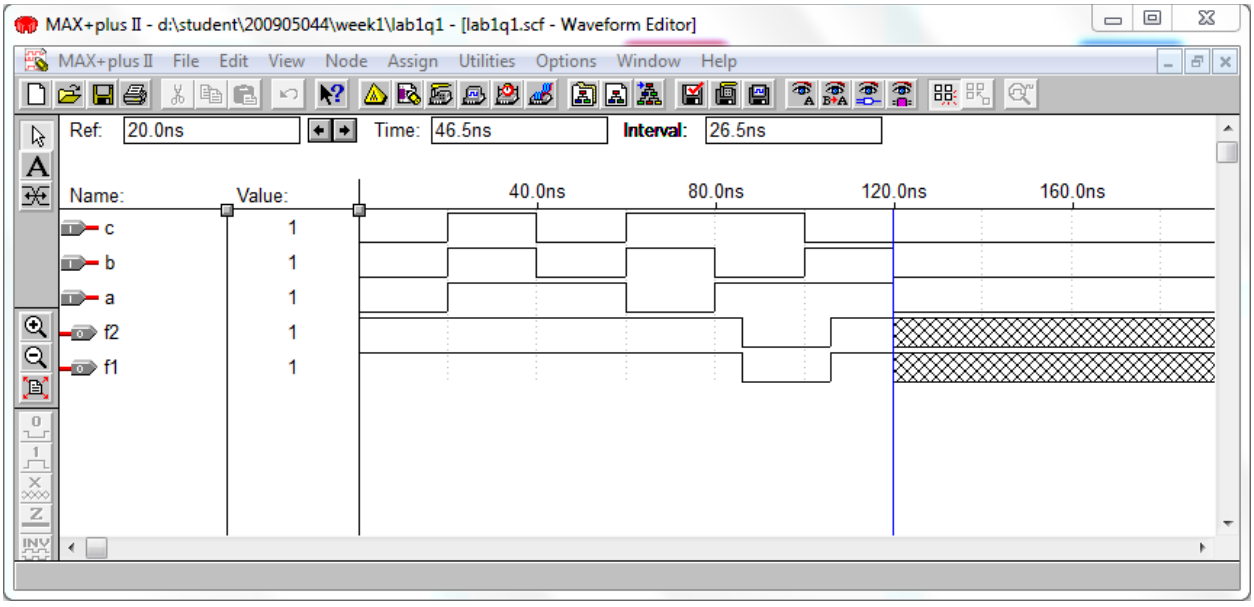
SECTION B

10

1) **Verilog code:**

```
// f1 = ac' + bc + b'c'
module lab1q1(a,b,c,f1,f2);
input a,b,c;
output f1,f2;
not(k1,c);
not(k2,b);
and(h1,a,k1);
and(h2,b,c);
and(h3,k2,k1);
or(f1,h1,h2,h3);
assign f2 = (a|~b|c) & (a|b|~c) & (~a|b|~c);
endmodule
```

Output Wave Form:

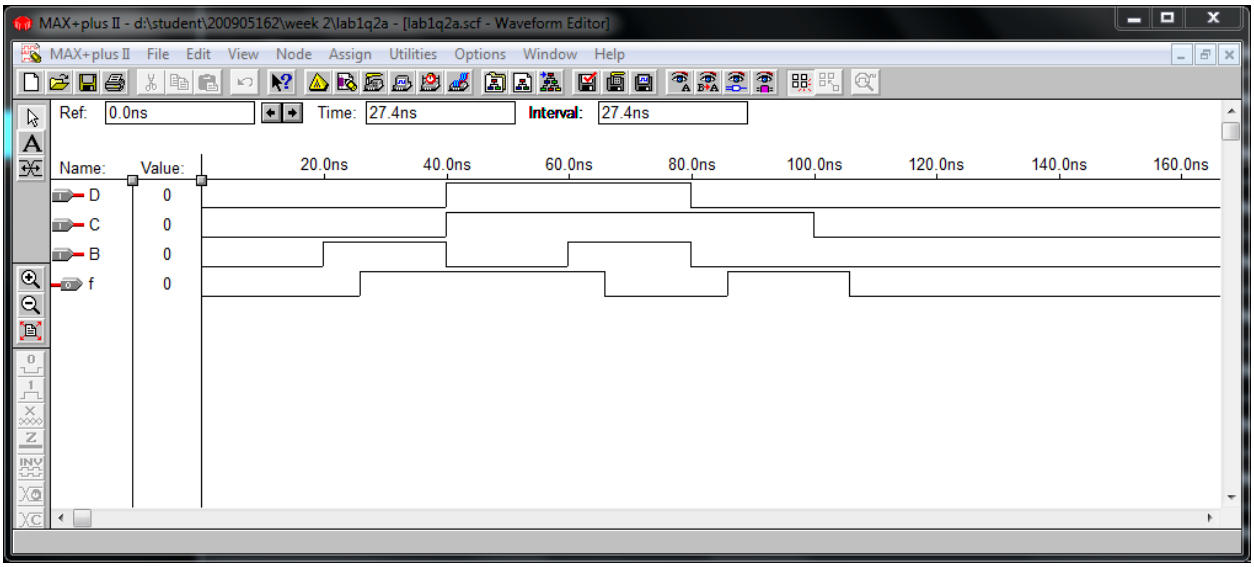


2a)

Verilog code:

```
module lab1q2a(A,B,C,D,f);

input A,B,C,D;

output f;

assign f=(~B&C) | (~B&D) | (B&~C&~D);

endmodule
```

Output Wave Form:

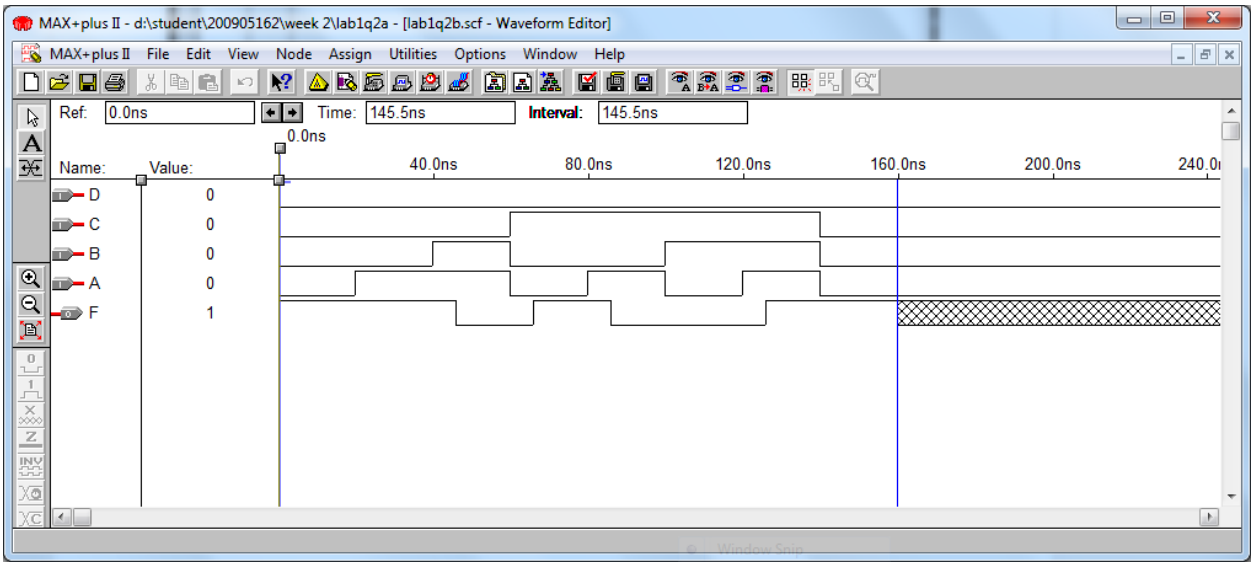


2b)

Verilog code:

```
module lab1q2b(A,B,C,D,F);

input A,B,C,D;

output F;

assign F=(A | ~B | ~C) & (~A | B | ~C) & (~A | B | ~D) & (~B | C | D);

endmodule
```

Output Wave Form:

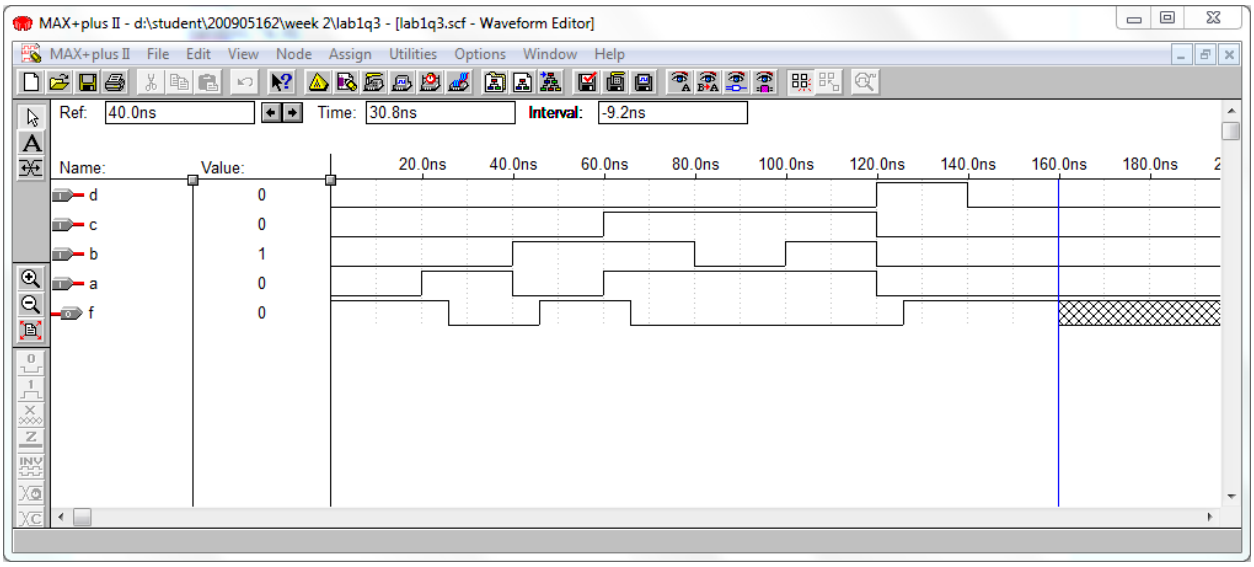


3)

Verilog code:

```
module l1q3(a, b, c, d, f);

input a, b, c, d;

output f;

nand(x1, ~a, ~c);

nand(x2, ~a, d);

nand(x3, b, ~c);

nand(x4, b, d);

nand(f, x1, x2, x3, x4);

endmodule
```

Output Wave Form:


MAX+plus II - d:\student\200905162\week 2\lab1q3 - [lab1q3.scf - Waveform Editor]
MAX+plus II File Edit View Node Assign Utilities Options Window Help
Ref: 40.0ns
Time: 30.8ns
Interval: -9.2ns
Name:
Value:
20.0ns
40.0ns
60.0ns
80.0ns
100.0ns
120.0ns
140.0ns
160.0ns
180.0ns
d 0
c 0
b 1
a 0
f 0

THANK YOU!