DSD LAB

Week 7 Assignment Submission

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Batch B1

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1. **Design and simulate the following counters**

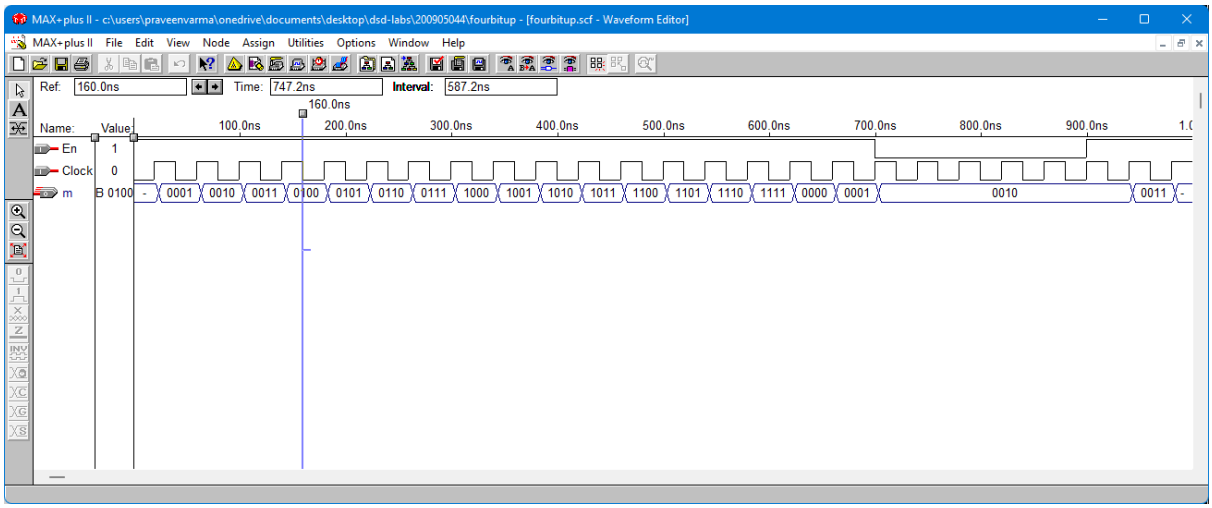
   a) 4 bit synchronous up counter

   Verilog code:

```
module fourbitup(m,Clock,En);
input En;
input Clock;
output [3:0]m;
trial stage1(En,Clock,m[0]);
trial stage2(En&m[0],Clock,m[1]);
trial stage3(En&m[0]&m[1],Clock,m[2]);
trial stage4(En&m[0]&m[1]&m[2],Clock,m[3]);
endmodule


module trial(T,Clock,Q);
input T,Clock;
output Q;
reg Q;
always@(posedge Clock)
if(T)
Q<=~Q;
endmodule
```

Output Waveform:



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(1) Synchronous 4 bit up Counter.

Present state				New state				FF Inputs			
A	B	C	D	A	B	C	D	T_A	T_B	T_C	T_D
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1

State Table for 4-bit up counter.

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Expression

i) for T_A

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	0	1	0
10	0	0	0	0

$T_A = BCD$

ii) for T_B

AB \ CD	00	01	11	10
00			1	
01			1	
11			1	
10			1	

$T_B = CD$

iii) for T_C

AB \ CD	00	01	11	10
00			1	
01			1	
11			1	
10			1	

$T_C = D$

iv) for T_D

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$T_D = 1$

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Circuit diagram:-

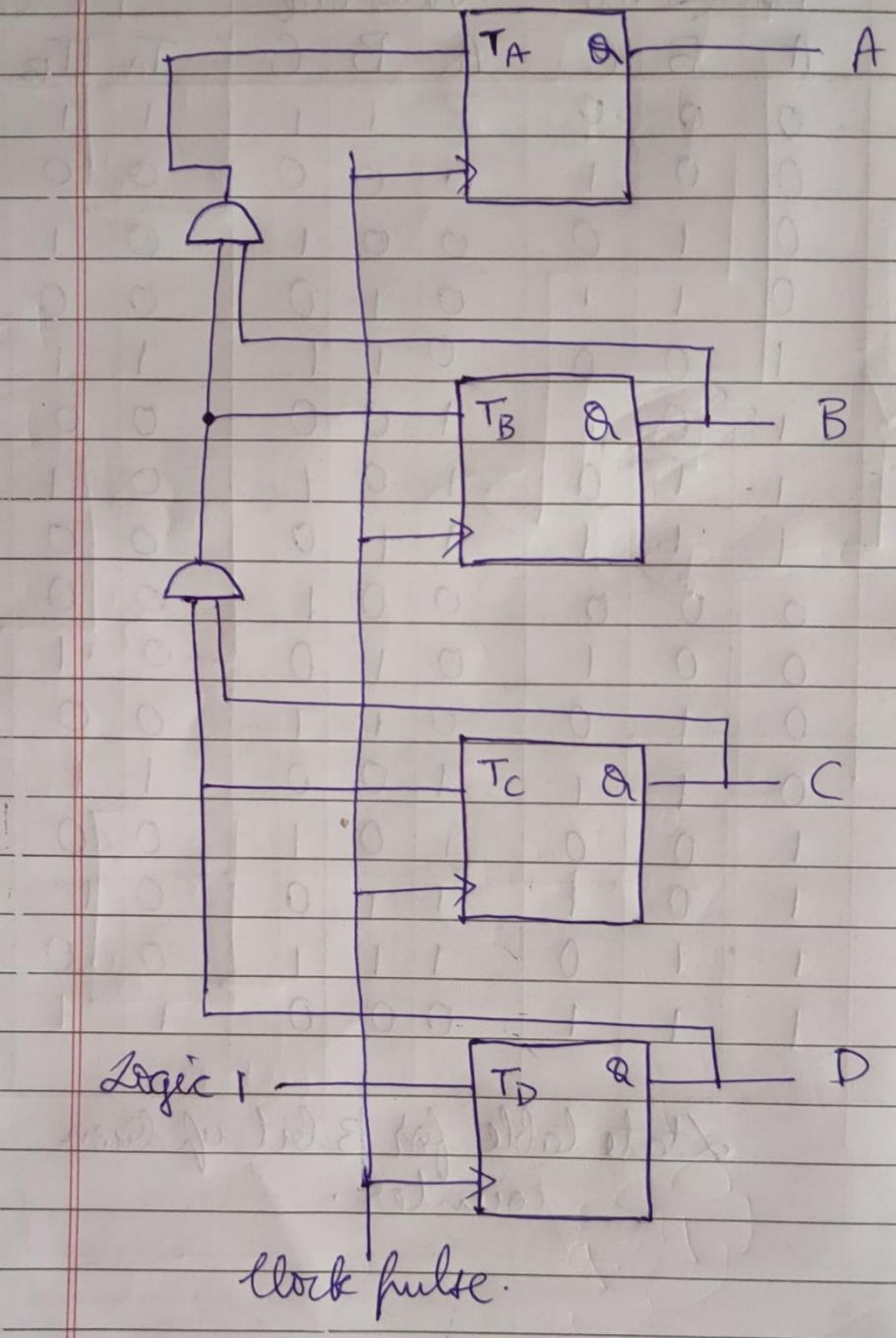


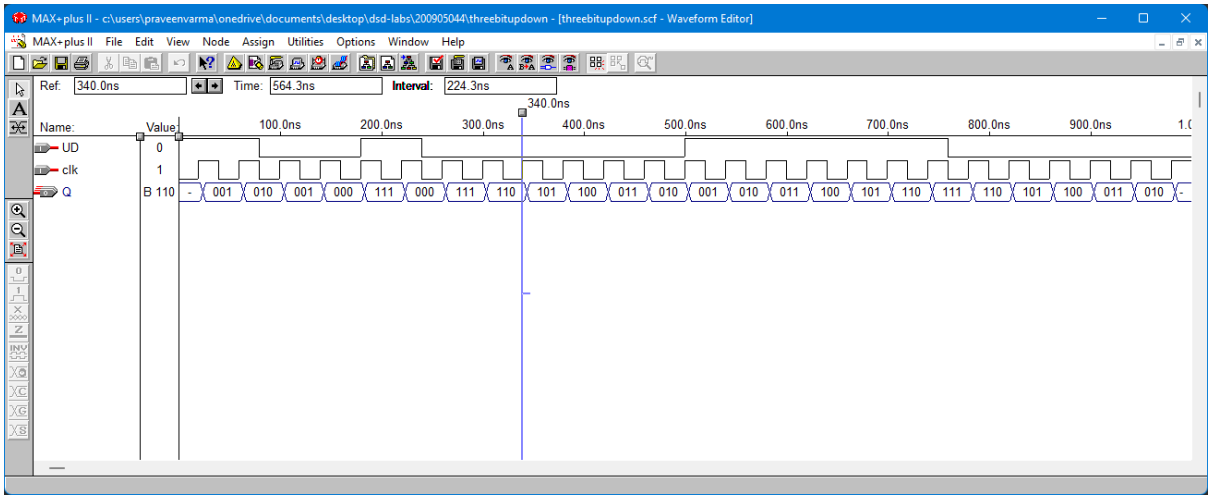
Diagram for 4-bit up counter

b) 3 bit synchronous up/down counter with a control input up/$\overline{down}$. If up/$\overline{down}$ = 1, then the circuit should behave as an up counter. If up/$\overline{down}$ = 0, then the circuit should behave as a down counter.

Verilog code:

```
module threebitupdown(clk,UD,Q);
input UD;
input clk;
output [2:0] Q;
wire control;
trial stage1(1,clk,Q[0]);
trial stage2(UD & Q[0] | (~UD & ~Q[0]),clk,Q[1]);
trial stage3(UD & Q[0] & Q[1] | (~UD & ~Q[0] & ~Q[1]),clk,Q[2]);
endmodule
module trial(T,clock,Q);
input T,clock;
output Q;
reg Q;
always@ (posedge clock)
if(T)
Q <= ~Q;
endmodule
```

Output waveform:


MAX+plus II - c:\users\praveenvarma\onedrive\documents\desktop\dsd-labs\20090504\threebitupdown - [threebitupdown.scf - Waveform Editor]
MAX+plus II File Edit View Node Assign Utilities Options Window Help
Ref: 340.0ns
Time: 564.3ns
Interval: 224.3ns
340.0ns
Name:
Value:
100.0ns
200.0ns
300.0ns
400.0ns
500.0ns
600.0ns
700.0ns
800.0ns
900.0ns
UD
0
clk
1
Q
B 110
- 001 010 001 000 111 000 111 110 101 100 011 010 001 010 011 100 101 110 111 110 101 100 011 010

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(2) Up down counter with control input

i/p	Present state			Next state			FF inputs		
UD	A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	0	1
0	1	0	0	0	1	1	1	1	1
0	1	0	1	1	0	0	0	0	1
0	1	1	0	1	0	1	0	1	1
0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	0	0	1	1	1

State table for 3 bit up down counter.

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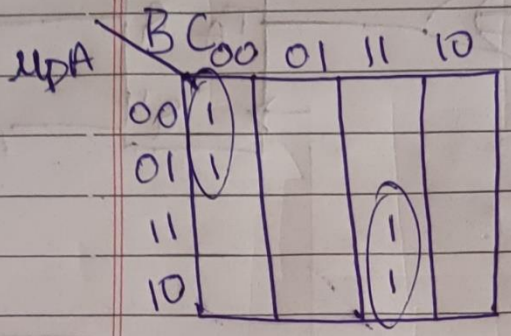
Problem:

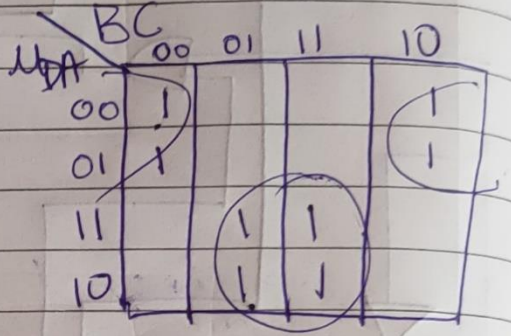
Expressions:

i) for T_A



$T_A = \bar{M_D} B\bar{C} + M_D BC$

ii) for T_B



$T_B = \bar{M_D}\bar{C} + M_D C$

$T_C = 1$ (as all inputs are 1)

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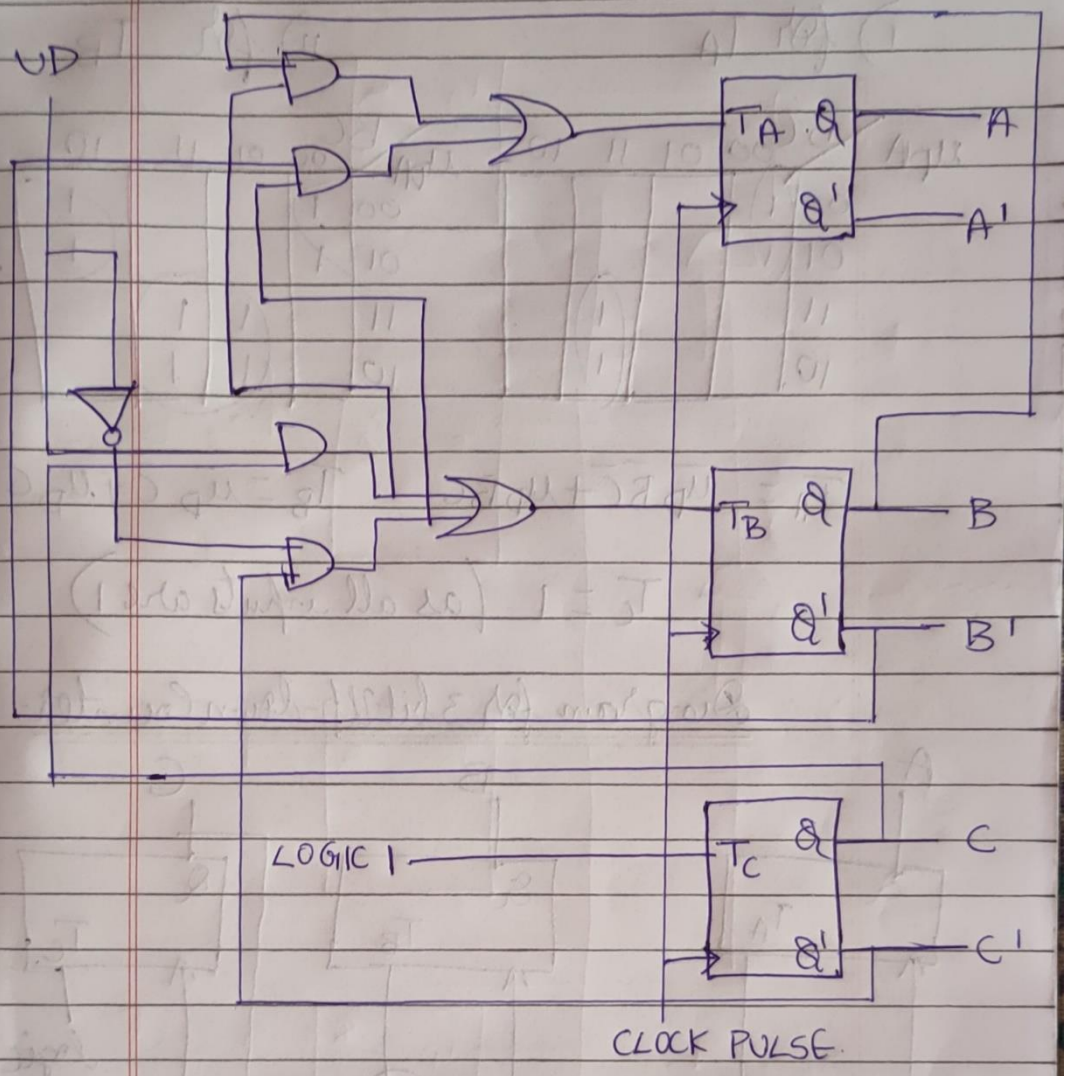
Circuit diagram :-



THANK YOU!