

# DSD LAB

## Week 6 Assignment Submission

Swamiraju Satya Praveen Varma

200905044

Batch B1

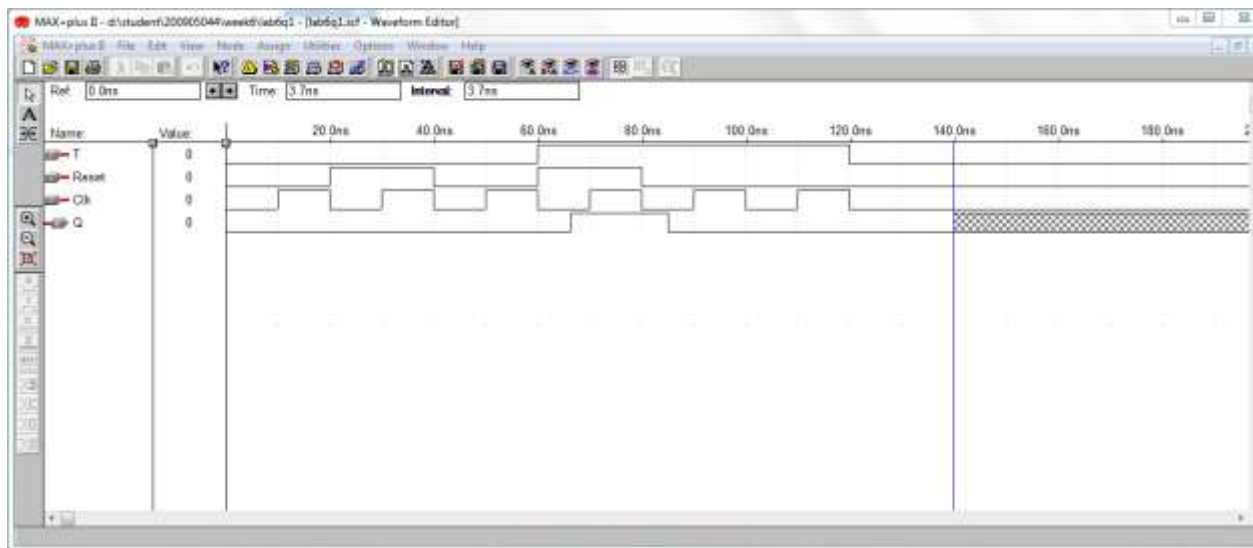
10

**1.** Write behavioral Verilog code for a negative edge triggered TFF with asynchronous active low reset.

**Verilog code:**

```
module lab6q1 (T, Clk, Q, Reset);  
input Reset, T, Clk;  
output Q;  
reg Q;  
always @ (negedge Clk or negedge Reset)  
if (!Reset)  
Q <= 0;  
else if (T == 1)  
Q <= ~Q;  
endmodule
```

**Output Waveform:**



2. Write behavioral Verilog code for a positive edge-triggered JKFF with synchronous active high reset.

**Verilog code:**

```
module lab6q2 (J, K, Clk, Reset, Q);
```

```
input J, K, Clk, Reset;
```

```
output Q;
```

```
reg Q;
```

```
always @ (posedge Clk)
```

```
if (Reset)
```

```
Q <= 0;
```

```
else
```

```
begin
```

```
case({J, K})
```

```
2'b00:Q<=Q;
```

```
2'b01:Q<=0;
```

```
2'b10:Q<=1;
```

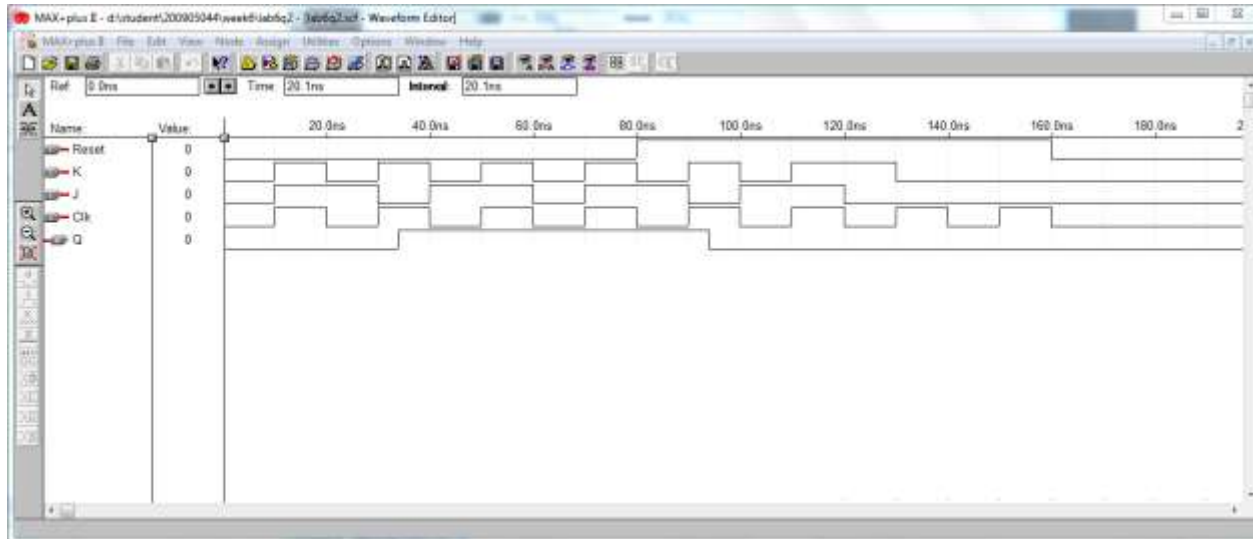
```
2'b11:Q<=~Q;
```

endcase

end

endmodule

### Output Waveform:



**3.** Design and simulate the following counters

**a)** 4-bit ring counter.

### Verilog code:

```
module lab6q3a (clk, f);
```

```
input clk;
```

```
output[3:0] f;
```

```
wire[1:0] w;
```

```
dff1 stage0 (w[0] ^ w[1], clk, w[1]);
```

```
dff1 stage1 (~w[0], clk, w[0]);
```

```
dec24 stage2 (w, clk, f);
```

```
endmodule
```

```
module dff1 (d, clk, q);  
input d;  
input clk;  
output q;  
reg q;  
always @ (posedge clk)  
begin  
q <= d;  
end  
endmodule
```

```
module dec24 (w, en, y);  
input[1:0] w;  
input en;  
output[3:0] y;  
reg[3:0] y;  
always @ (posedge en)  
begin  
case (w)  
0:y = 4'b0001;  
1:y=4'b0010;  
2:y = 4'b0100;
```

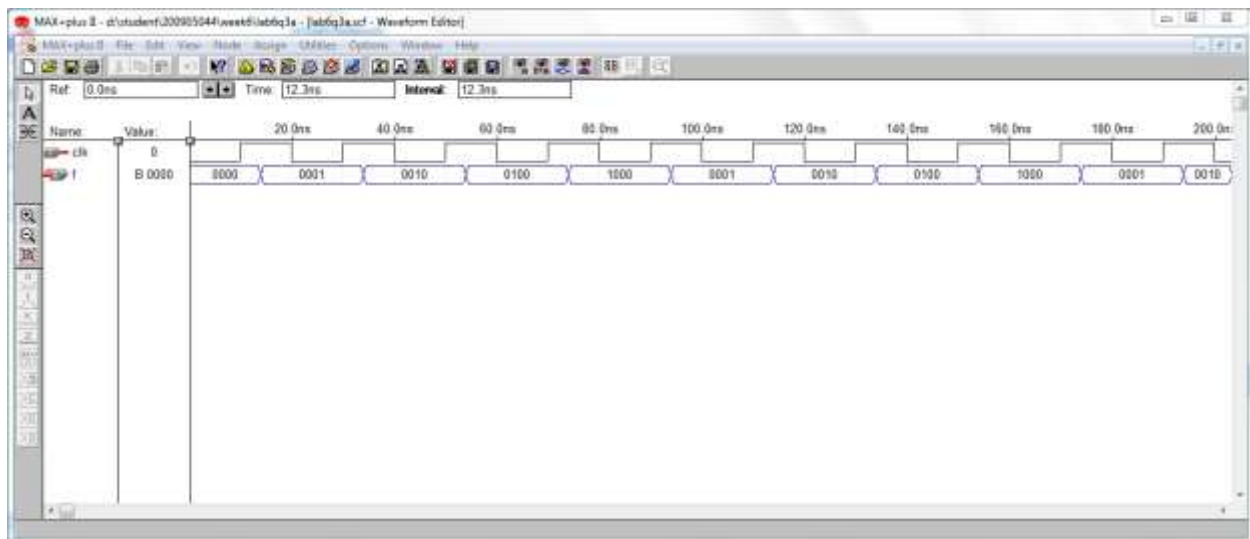
```
3:y=4'b1000;
```

```
endcase
```

```
end
```

```
endmodule
```

### Output Waveform:



**b)** 5 bit Johnson counter.

### Verilog code:

```
module lab6q3b (Clk, Q);
```

```
input Clk;
```

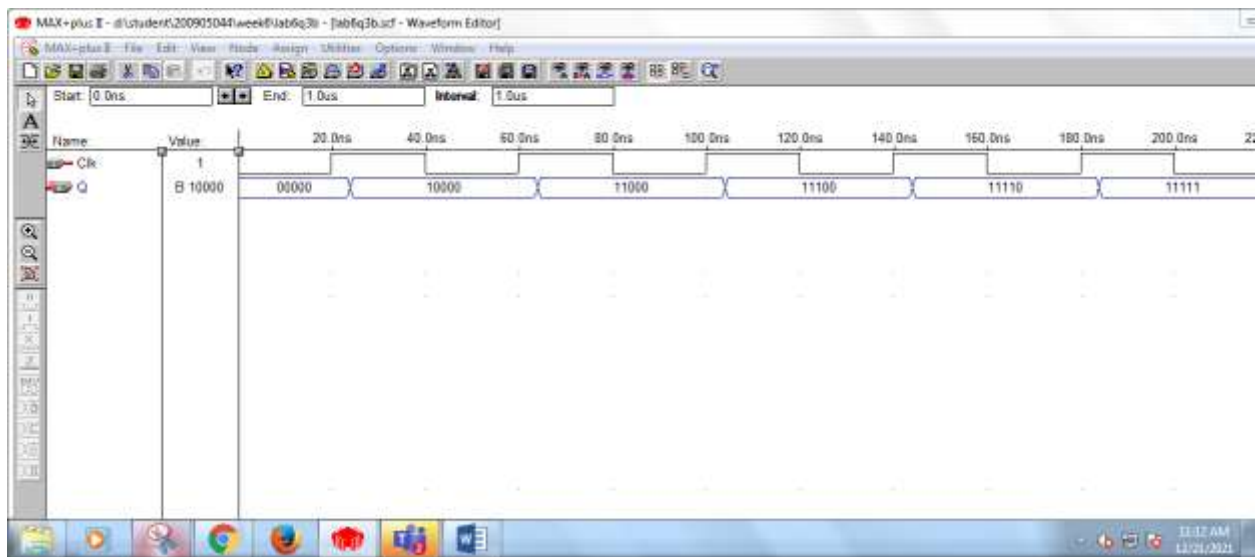
```
output[4:0] Q;
```

```
reg[4:0] Q;
```

```
always @ (posedge Clk)
```

```
begin
case (Q)
5'b00000: Q<=5'b10000;
5'b10000: Q<=5'b11000;
5'b11000: Q<=5'b11100;
5'b11100: Q<=5'b11110;
5'b11110: Q<=5'b11111;
5'b11111: Q<=5'b01111;
5'b01111: Q<=5'b00111;
5'b00111: Q<=5'b00011;
5'b00011: Q<=5'b00001;
5'b00001: Q<=5'b00000;
endcase
end
endmodule
```

**Output Waveform:**



THANK YOU!