Fully abstract categorical semantics for digital circuits
Extended abstract

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Contribution. It is essential that we have ways to verify the correctness of digital circuits and reason with them. Conventionally, this is done by translation into an executable model which can be simulated to observe its behaviour. An alternative approach, used in software, is to reason *syntactically*: programs are formulated equationally and can be reduced step by step. When provided with inputs, the goal of such a system is to apply reductions and derive an output value.

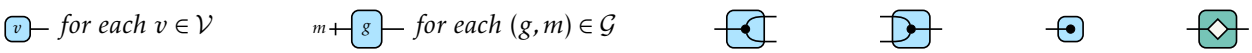
Such an equational system was first presented in [GJ16; GJL17a], in which digital circuits with delay and (instant) feedback are modelled as morphisms in a freely generated traced cartesian category, or *dataflow category* [CŞ94; Has97]. However, the presentation was informal and, crucially, not complete, and could not reduce all circuits to a stream of values. Our work brings this project to its conclusion, formalising the categorical semantics and completing the set of equations.

Syntax. Circuits are defined over a *signature*.

Definition 1 (Circuit signature)**.** *Let Σ be a tuple $(\mathcal{V}, \bullet, \circ, \mathcal{G})$ where $\mathcal{V}$ is a finite set of* values *with distinguished elements $\bullet, \circ \in \mathcal{V}$, and $\mathcal{G}$ is a finite set of tuples (g, m) where g is a* gate symbol *and $m \in \mathbb{N}$ is its* arity.

The distinct elements $\bullet$ and $\circ$ represent a *disconnected wire* (a *lack* of information) and a *short circuit* (*inconsistent* information) respectively: the latter can be thought of as 'true and false simultaneously'. Using a signature, digital circuits are constructed as morphisms in a freely generated symmetric traced monoidal category (STMC). To aid in the presentation, we shall use the graphical calculus of *string diagrams* [JS91; JSV96; Sel11].

Definition 2 (Sequential circuits)**.** *For a signature Σ, let $\mathbf{SCirc}_\Sigma$ be the symmetric traced monoidal category freely generated over:*



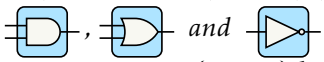
The small boxes are *values*: these represent the signals that can flow through our circuits. Next come the generators for each gate symbol in our signature, and *structural* generators for forking, joining and stubbing wires. The final generator is a *delay* generator: one can think of this as delaying its inputs for one tick. We write sequential circuits obtained by composing generators as green squares 

. If a circuit is *combinational*, i.e. it contains no delay or trace, it is drawn in a lighter blue square 

. To avoid clutter, we occasionally omit the backgrounds of generators. When restricted to the combinational circuits, this work is similar to [Laf03]. Where the approaches diverge is the inclusion of delay and feedback.

Semantics. Circuits specified syntactically have no computational content. To add *semantics* to circuits, first the signature must be interpreted in some domain.

Definition 3 (Interpretation)**.** *Let $\Sigma = (\mathcal{V}, \mathcal{G})$ be a signature. A interpretation of Σ is a tuple $\mathcal{I} = (\mathbf{V}, \mathcal{I}_\mathcal{V}, \mathcal{I}_\mathcal{G})$ where $\mathbf{V}$ is a finite lattice, $\mathcal{I}_\mathcal{V}$ is a bijective function $\mathcal{V} \setminus \{\bullet, \circ\} \to \mathbf{V} \setminus \{\top, \bot\}$, and $\mathcal{I}_\mathcal{G}$ is a map from each $(g, m) \in \mathcal{G}$ to a monotone function $\overline{g} \colon \mathbf{V}^m \to \mathbf{V}$.*

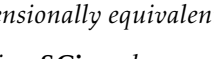
Example 4. *Let $\Sigma_\star = (\{\bullet, \mathsf{t}, \mathsf{f}, \circ\}, \bullet, \circ, \{(AND, 2), (OR, 2), (NOT, 1)\})$ be a signature. In $\mathbf{SCirc}_{\Sigma_\star}$, the values are*  *; the gates are*  *. Let $\mathbf{V}_\star$ be the lattice $(\{\bot, 0, 1, \top\}, \sqsubseteq)$, with the join defined as $0 \sqcup 1 = \top$ and the meet defined as $0 \sqcap 1 = \bot$. Let $\{\wedge, \vee, \neg\}$ be the* Belnap logic *operators [Bel77]: the truth tables are listed in Fig. 1. Let $\mathcal{I}_\star = (\mathbf{V}_\star, \{\mathsf{f} \mapsto 0, \mathsf{t} \mapsto 1\}, \{AND \mapsto \wedge, OR \mapsto \vee, NOT \mapsto \neg\})$.*

The semantics of circuits is that of *stream functions*, which take as input a stream and output a stream. In particular, we are interested in stream functions of the form $(\mathbf{V}^m)^\omega \to (\mathbf{V}^n)^\omega$.

Definition 5. *For an interpretation $\mathcal{I} = (\mathbf{V}, \mathcal{I}_\mathcal{V}, \mathcal{I}_\mathcal{G})$, let $\mathbf{Stream}_\mathcal{I}$ be the prop with morphisms $m \to n$ as stream functions $(\mathbf{V}^m)^\omega \to (\mathbf{V}^n)^\omega$ freely generated over stream functions for values $\tilde{v} \colon 0 \to 1$ for each $v \in \mathbf{V}$, defined as $\tilde{v}(0) = v$ and $\tilde{v}(i) = \bot$; for gates $\tilde{g} \colon m \to 1$ for each $(g, m) \in \mathcal{G}$ defined as $\tilde{g}(\sigma)(i) = g(\sigma(i))$; and for delay $\delta \colon 1 \to 1$ defined as $\delta(\sigma)(0) = \bot$ and $\delta(\sigma)(i+1)$.*

Theorem 6. *$\mathbf{Stream}_\mathcal{I}$ is traced.*

Definition 7. *Let $[\![-]\!]_\mathcal{I} : \mathbf{SCirc}_\Sigma \to \mathbf{Stream}_\mathcal{I}$ be a traced prop morphism, mapping circuits to appropriate stream functions. The details are omitted, see [GKS22].*

If two circuits map to the same semantics in $\mathbf{Stream}_\mathcal{I}$, we say they are *extensionally equivalent*, written 

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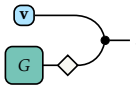
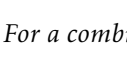
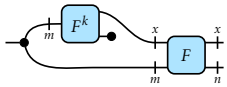
Theorem 8 ([GKS22])**.** *Let $\mathbf{SCirc}_{\Sigma,\mathcal{I}}$ be the category obtained by quotienting $\mathbf{SCirc}_\Sigma$ by $\approx_\mathcal{I}$. Then there is an isomorphism of categories $\mathbf{SCirc}_{\Sigma,\mathcal{I}} \cong \mathbf{Stream}_\mathcal{I}$.*

Equational reasoning. Circuits of non-equal syntax can have the same semantics as stream functions. However, in general it is prohibitive to check that the corresponding streams for two circuits are equal [GJL17b]: it is more efficient to reason *equationally*. Equations are identities that hold in the quotient category $\mathbf{SCirc}_{\Sigma,\mathcal{I}}$. Given a set of equations $\mathcal{E}$, we write $F =_{\mathcal{E}} G$ if F can be rewritten to G by applying equations in $\mathcal{E}$. Note that since we are using string diagrams, the axioms of STMCs are 'absorbed' into the notation and always hold by moving wires and boxes around.

Productivity. A common use of equational reasoning is to take a circuit and reduce it to its stream of output values.

Definition 9 (Productivity). *For a set of equations $\mathcal{E}$, a closed sequential circuit F is called* productive under $\mathcal{E}$ *if there exist values $\mathbf{v}$ and sequential circuit G such that $F =_{\mathcal{E}}$*  .

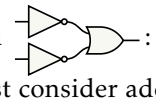
A set of equations was presented in [GJ16]. However, they were not *complete*: these axioms could not necessarily handle circuits with *non-delay-guarded feedback*, in which every feedback loop does not pass through a delay generator. While in some circuits 'instant feedback' is useful [Rie04; MSB12], in other cases it can result in an unproductive circuit. To tackle this, we use *Kleene's fixpoint theorem*: since all the gates in an interpretation are monotone, they have a least fixpoint; since our lattice is finite, we are able to compute it after a finite number of iterations.

Definition 10. *For a combinational circuit F, let its n*th iteration *F^n be defined inductively as $F^0 :=$*  *and $F^{k+1} :=$*  . *Let $\mathcal{I} = (\mathbf{V}, \mathcal{I}_{\mathcal{V}}, \mathcal{I}_{\mathcal{G}})$ be an interpretation and let c be the length of the longest chain in $\mathbf{V}$: the* fixpoint *of F in $\mathcal{I}$, denoted as $F^\dagger$, is defined as F^c.*

The complete set of equations $\mathcal{C}$ for closed circuits under *any* interpretation is shown in Fig. 2. An important consequence of these is that the *unfolding* rule for circuits with feedback can be derived, illustrated in Fig. 3.

Theorem 11. *Any closed sequential circuit F is productive under $\mathcal{C}$.*

By applying productivity, a sequence of values can be obtained for *any* sequential circuit F given some inputs $\mathbf{v}$. This sequence is precisely the corresponding stream obtained using $[\![-]\!]_{\mathcal{I}}$.

Full abstraction. In the closed case these equations suffice as the input values are propagated across the circuit, with gates evaluated one by one. However, when faced with an *open circuit* the equations in $\mathcal{C}$ are not sufficient. For example, consider the circuits  and  : when interpreted under $\mathcal{I}_\star$ their stream functions are equal by applying de Morgan's law. To tackle this we must consider additional equivalences between *combinational circuits*.

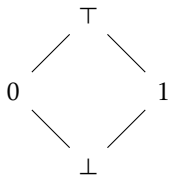
All circuits will include the generators for the fork, join, stub and disconnected wire. Under any interpretation, these four generators form a *bialgebra*, so we can add the corresponding axioms listed in to our framework, listed in Fig. 4 . All that remains is to add equations for equivalences between gates

Definition 12. *We say that a set of equations $\mathcal{E}$, where each $e \in \mathcal{E}$ contains at least one gate, is* combinationally complete *for an interpretation $\mathcal{I}$ if for all combinational circuits F and G, if $[\![F]\!]_{\mathcal{I}} = [\![G]\!]_{\mathcal{I}}$ then $F =_{\mathcal{E}} G$.*

Example 13. *A set of equations combinationally complete for $\mathcal{I}_\star$ are listed in Fig. 5.*

Theorem 14 (Full abstraction). *For an interpretation $\mathcal{I}$, let $\mathcal{E}$ be a set of equations combinationally complete for $\mathcal{I}$. Then $F =_{\mathcal{C}+\mathcal{B}+\mathcal{E}} G$ if and only if $[\![F]\!]_{\mathcal{I}} = [\![G]\!]_{\mathcal{I}}$.*

This allows us to reason *purely equationally* with digital circuits, instead of appealing to the potentially inefficient stream semantics. Even so, this does not immediately yield an *automatic* rewriting framework, as computationally it is difficult to handle the trace. A suitable strategy for tackling this problem was presented in [GJL17a] using graph rewriting on *framed point graphs*; a current thread of work is reworking this using recent work on rewriting with *hypergraphs* [Bon+16; Kay21].



∧	⊥	0	1	⊤
⊥	⊥	0	⊥	0
0	0	0	0	0
1	⊥	0	1	⊤
⊤	0	0	⊤	⊤

∨	⊥	0	1	⊤
⊥	⊥	⊥	1	1
0	⊥	0	1	⊤
1	1	1	1	1
⊤	1	⊤	1	⊤

¬	
⊥	⊥
1	0
0	1
⊤	⊤

Figure 1: The lattice structure on $\mathbf{V}_\star$, and truth tables for the gates in $\Sigma_\star$ under $\mathcal{I}_\star$.

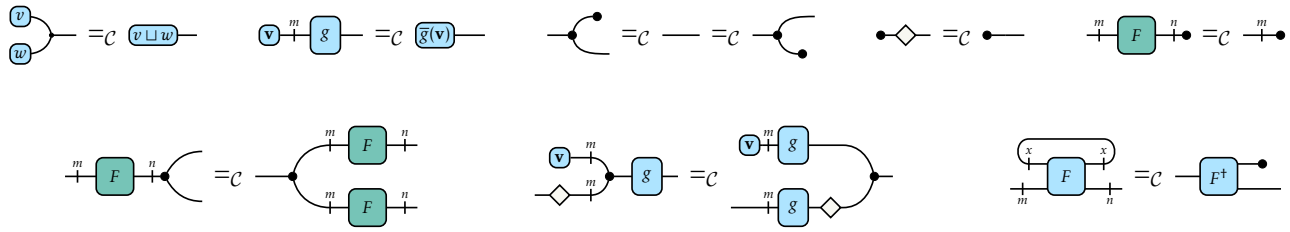


Figure 2: The set of equations $\mathcal{C}$ for reducing closed circuits.

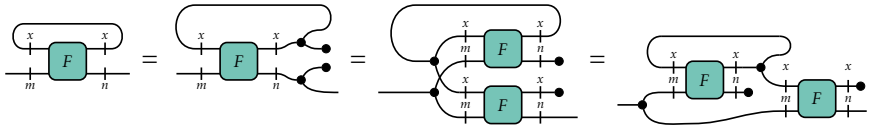


Figure 3: Deriving the *unfolding* rule using equations in $\mathcal{C}$.

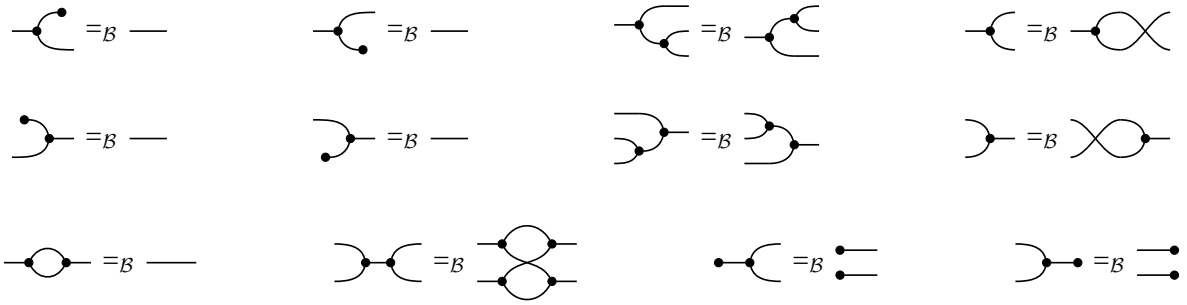


Figure 4: Set $\mathcal{B}$ of *bialgebra* equations.

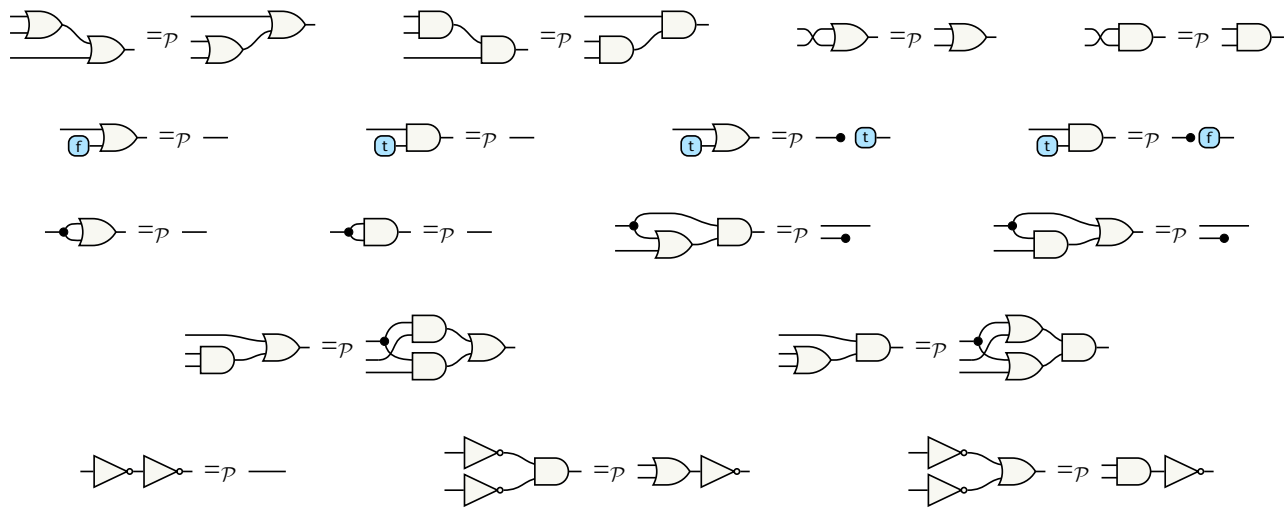


Figure 5: A (not necessarily minimal) set of equations $\mathcal{P}$ which is combinationally complete for $\mathcal{I}_\star$, adapted from [RR98].

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