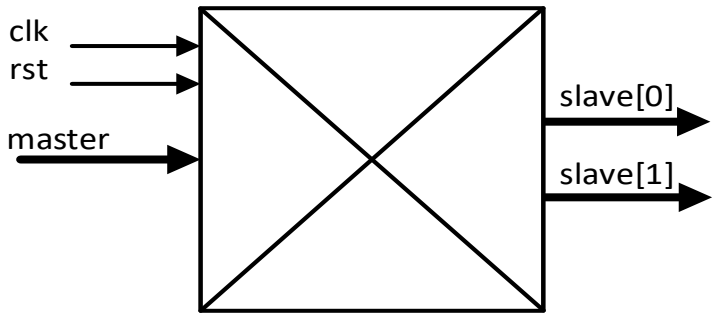
Implementation of AMBA-APB communication protocol

Advanced Microcontroller Bus Architecture (AMBA) bus protocols are a set of industry-standard communication protocols for System-on-Chip memory-mapped interconnections. The Advanced Peripheral Bus (APB) is used to access low-speed peripherals and is the simplest one. It is required to design a digital circuit for implementing a communication based on AMBA-APB standard. The interface of the circuit to be designed is as follows:

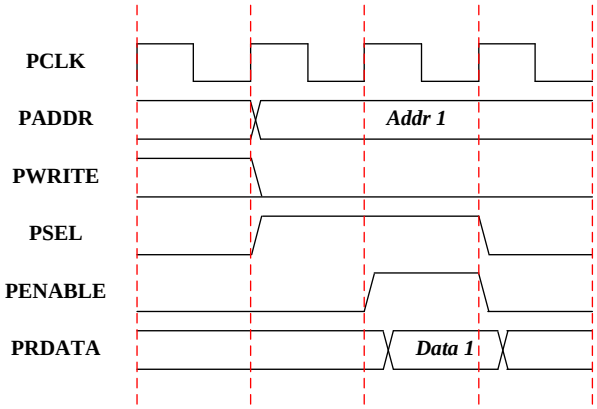


The system is composed of one *APB-Master* which can send read/write transactions to two *APB-Slaves*, a 64x16 ROM and a 128x8 RAM. The *APB-Master* coordinates the reading and writing transactions on the bus by handling the control signals of the communication interface. The *APB-Slaves* reply to the master's requests.

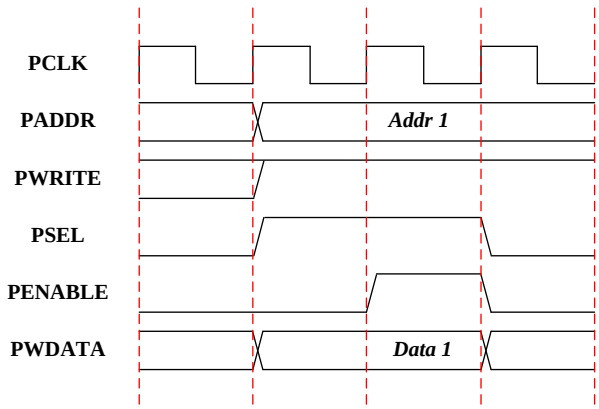
APB Interface:

- *P_clk*
- *P_sel*[0:K-1]: slave selection (K = number of slaves)
- *P_write*: 0 read transaction, 1 write transaction
- *P_enable*: enable signal
- *P_rdata*[0:N-1]: data read from peripheral
- *P_wdata*[0:N-1]: data to write to peripheral
- *P_addr*[0:M-1]: address (both for read and write transactions)

APB Read TX



APB Write TX



The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.

- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions