

Multichannel phase coherent transceiver system with GNU Radio interface

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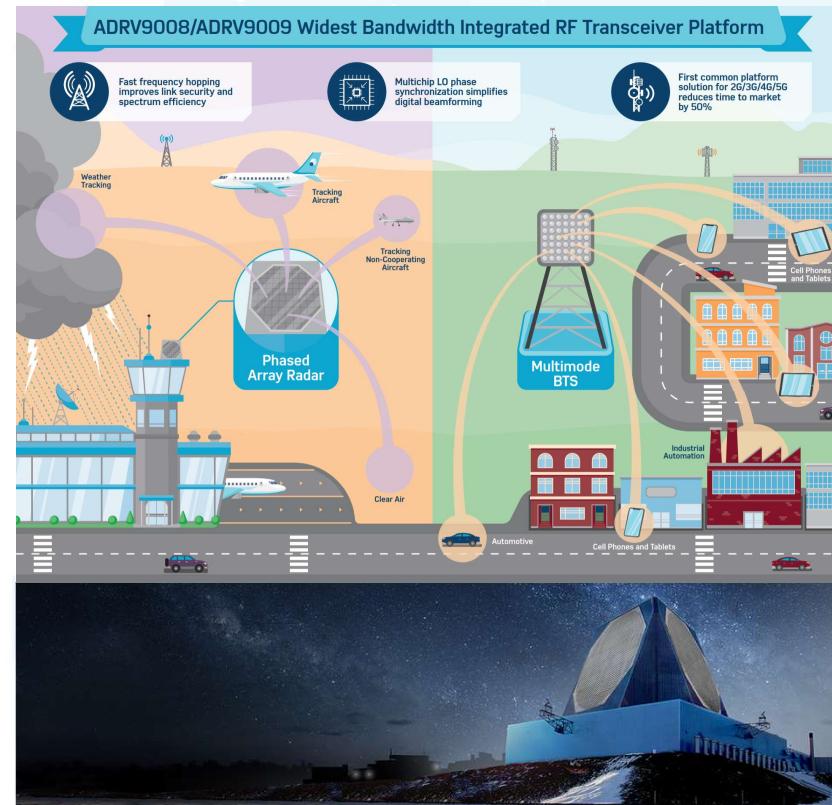
Systems Development Group



RADAR

► RADAR application examples

- Short range Tracking
 - Weather radar
 - Maritime radar
 - Level sensors
 - Mapping
 - Threat detection
 - Missile guidance
-
- **Phase array techniques are common**
 - Removal of mechanical elements for reliability and size
 - Fast steering and multiple beams
 - Improved SNR and phase noise
-
- **Important System Factors:**
 - Low Phase Noise at small offsets
 - High bandwidth – range resolution
 - Synchronization between channels
 - Dynamic Range/SNR
 - Fast response
 - Common Frequency range: 1-12GHz
-
- **MIMO or Phased-MIMO RADAR**

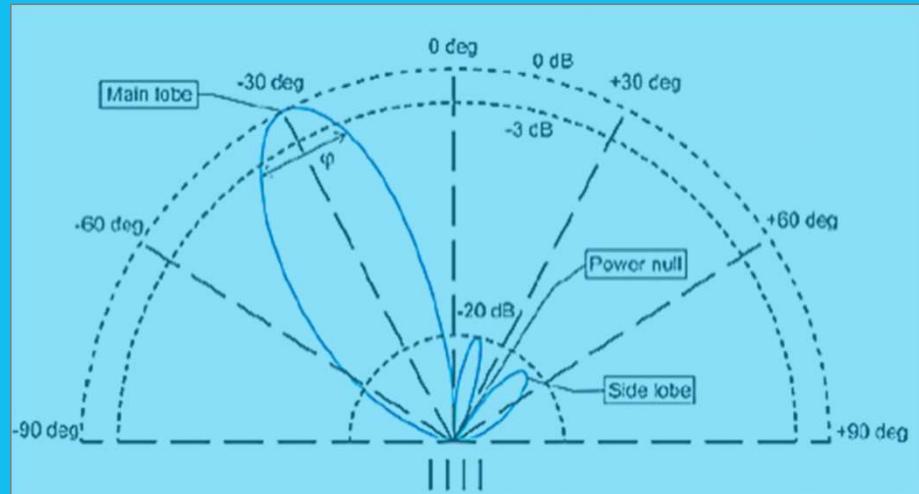


Signals Intelligence

- ▶ **Signals Intelligence (SIGINT)** – Intelligence gathering by intercepting signals

- **Communications Intelligence (COMINT)**
 - Intercept communications to determine who is transmitting and content of transmission
 - Interrogation, transceiver acts as a cell tower
- **Electronic Signals Intelligence (ELINT)**
 - Non-communications based signal identification
- **Direction Finding**
 - Time Difference of Arrival (TDOA)
 - Array of directed antennas
- **Important Signal Chain Factors**
 - **Fast sweeping to identify targets**
 - **High sensitivity**
 - **Medium to High Output Power depending on system**
 - **Sometimes RX Only**
 - **Common Frequency range: 30MHz to 6GHz**

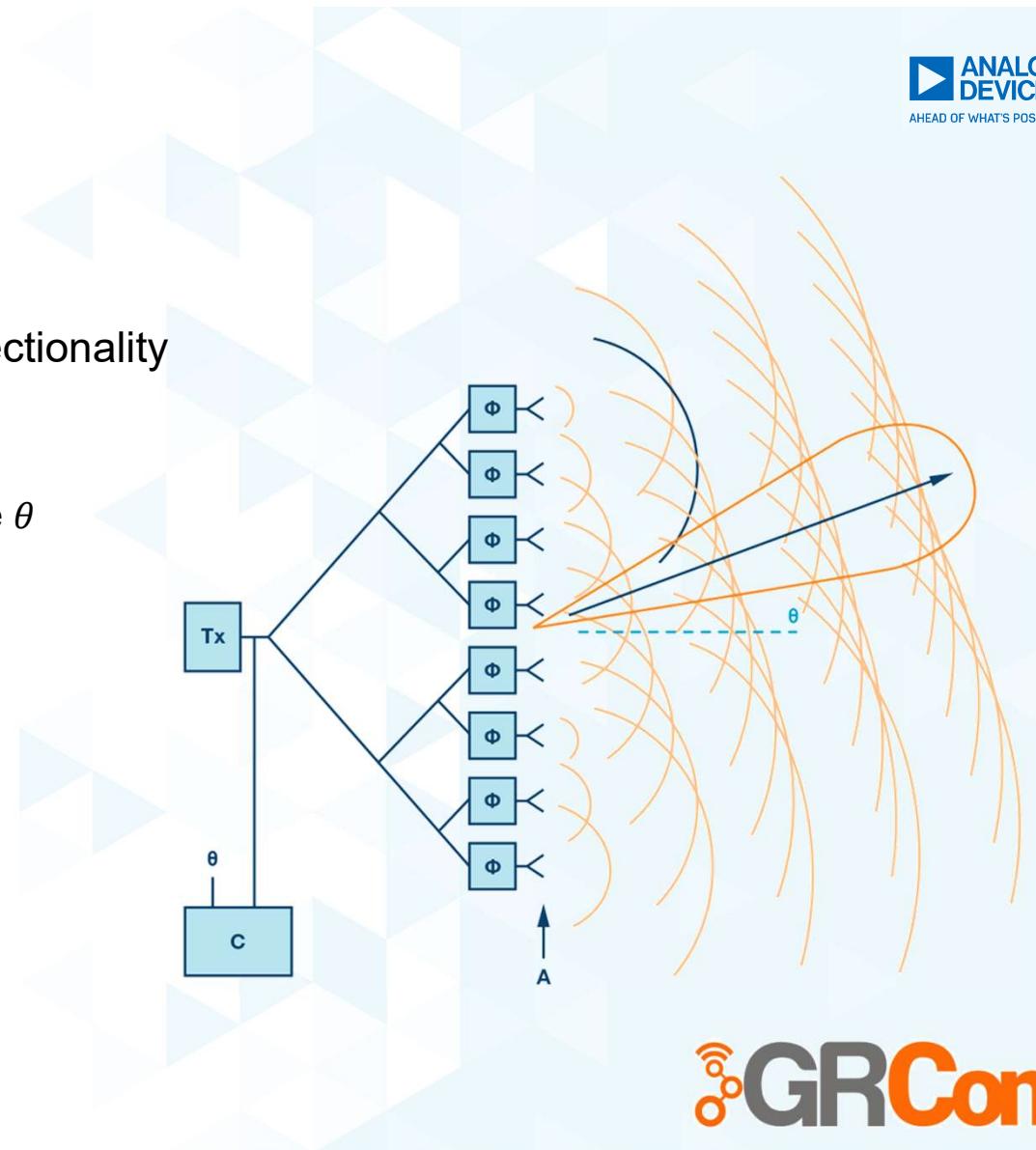




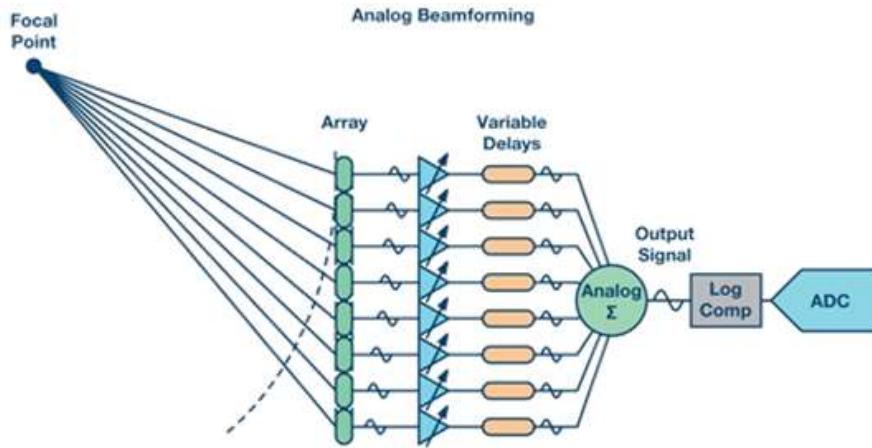
Phased Array Overview

Phased-Array RADARs

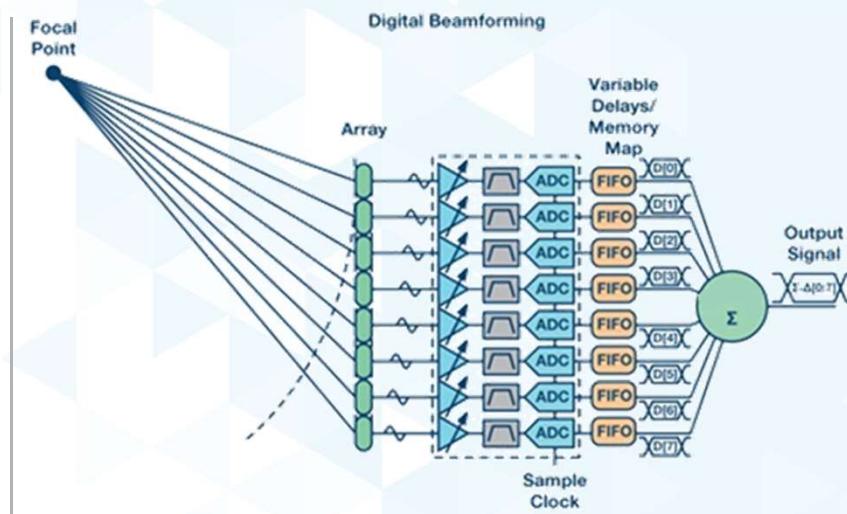
- ▶ RADAR systems utilizing array of antennas
- ▶ Analog or Digital phase shifters provide directionality
 - Eliminate mechanical rotations
 - Each channel possesses different phase
 - Steers wavefront (WF) out of antenna at angle θ
 - Looks at particular WF into antenna
- ▶ Array can be 2-dimensional
 - Allows for steering in both x- and y-directions
 - Large number of elements per channel
- ▶ Can also utilize antenna polarization
 - To transmit & decipher additional information



Beamforming techniques



- ▶ Phase shifting achieved in analog domain
- ▶ Amplitude control achieved in analog domain
- ▶ Align channels on antenna side of ADC / DAC
- ▶ **Uses discrete phase-shifters**
- ▶ Multiple channels can be combined
 - Lower number of amplifiers
 - Lower number of phase shifters
 - Requires more commands to shifters / attenuators



- ▶ Phase shifting achieved in digital domain
- ▶ With use of:
 - NCOs (continuous-wave signals)
 - Digital FIR filters (broadband signals)
- ▶ Equalize channels on FPGA side of ADC / DAC
- ▶ Each channel can be independently controlled
 - Within DSP constraints
 - Provides maximum channel configurability
 - **Multibeam capability**

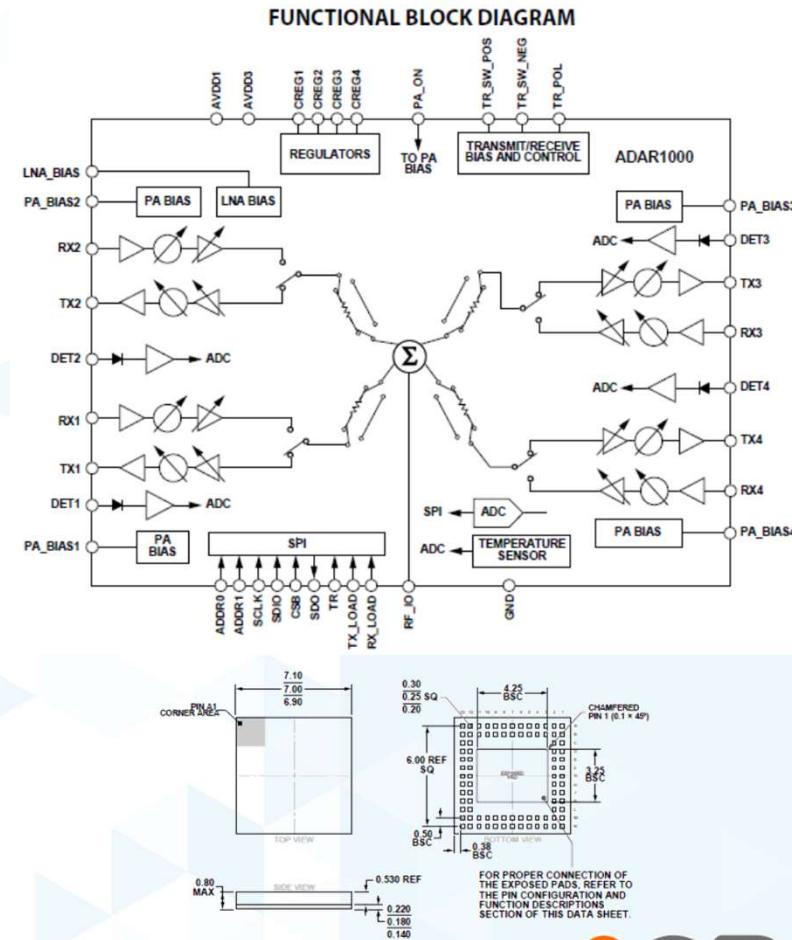
ADAR1000: 4 Channel Analog Beamformer

Key Features

- ▶ 8 GHz to 16 GHz frequency range
- ▶ Single-pin transmit and receive control
- ▶ 360° phase adjustment range
- ▶ 2.8° phase resolution
- ▶ ≥31 dB gain adjustment range
- ▶ Bias and control for external transmit and receive modules
- ▶ Memory for 121 prestored beam positions
- ▶ Four –20 dBm to +10 dBm power detectors
- ▶ 88-terminal, 7 mm × 7 mm LGA package

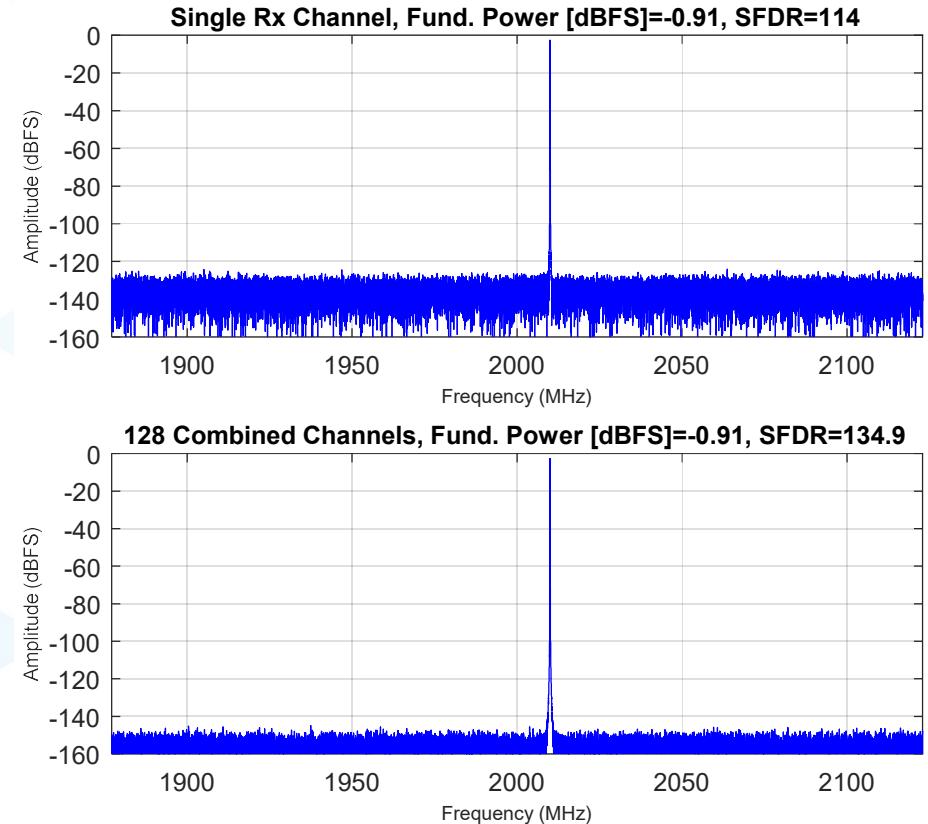
Key Benefits

- ▶ Compact form factor for electronically steered analog beamformer
- ▶ Negative bias voltage from integrated DAC intended for gate bias of GaAs or GaN amplifier
- ▶ Support low power bias mode with 50% reduction in power consumption
- ▶ Potential 5G applications



Phased-Array Dynamic Range & Spurious Improvements

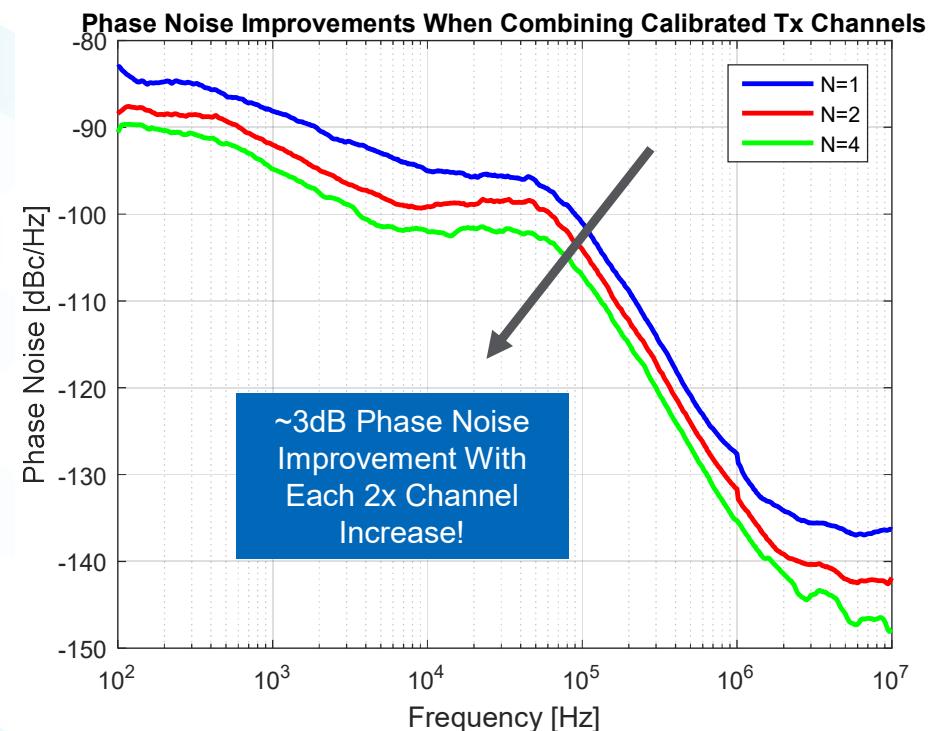
- ▶ After Rx phase and amplitude calibrations:
 - Rx system is time and amplitude aligned
 - System performance better than individual Rx
- ▶ When the number N of ADC channels is doubled:
 - The effective number of bits is incremented
 - The Rx noise spectral density (NSD) is lowered
- ▶ If channel spurious contributions uncorrelated:
 - Spurious do not add
 - Aligned, desired signal do add
 - But noise floor lowers
- ▶ Results in $10\log(N)$ improvement in dynamic range
- ▶ Improves combined Rx system sensitivity



Combined Rx Channels In Phased-Arrays Improve System Dynamic Range!

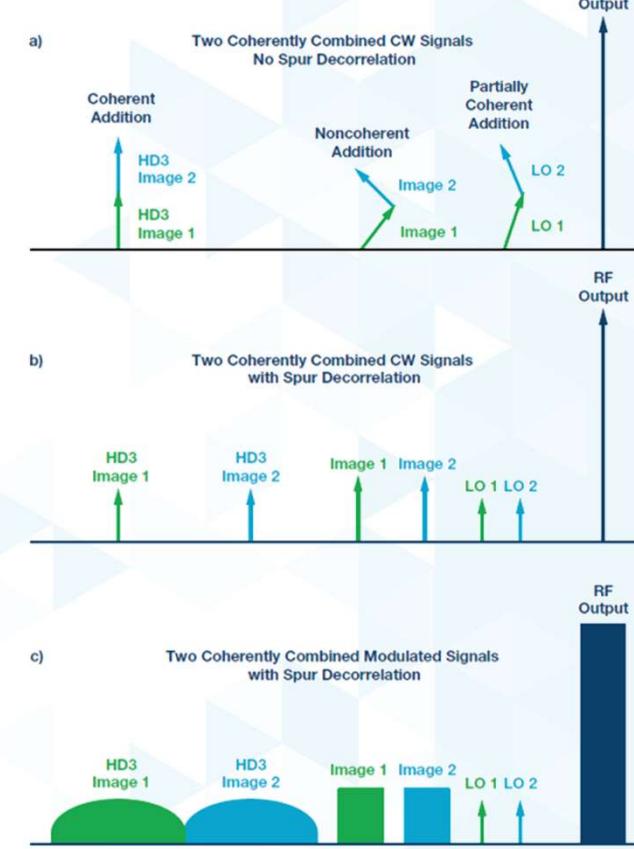
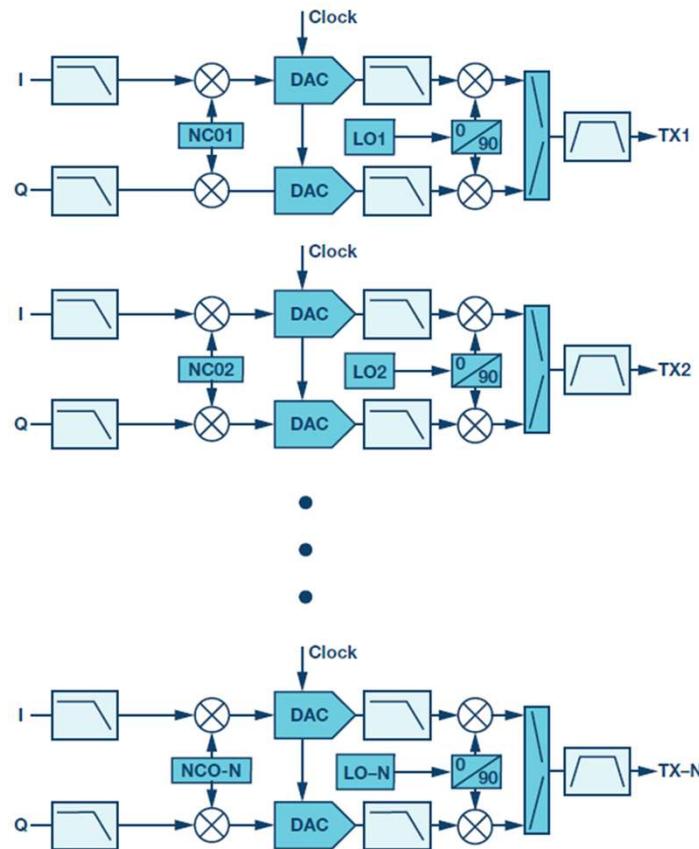
Phased-Array Tx Phase Noise Improvements

- ▶ After Tx amplitude and phase calibrations:
 - Output Tx signals can be combined constructively
 - System phase noise improvements achieved
 - System spurious performance can be improved
- ▶ Improvements rely on uncorrelated channels
 - Requires separate PLL sources to subarrays
 - Desire noise to not add constructively
- ▶ If noise sources are uncorrelated:
 - $10\log(N)$ phase noise improvements/channel achieved
 - System data throughput can be increased



Combined Tx Channels In Phased-Arrays Improve System Phase Noise!

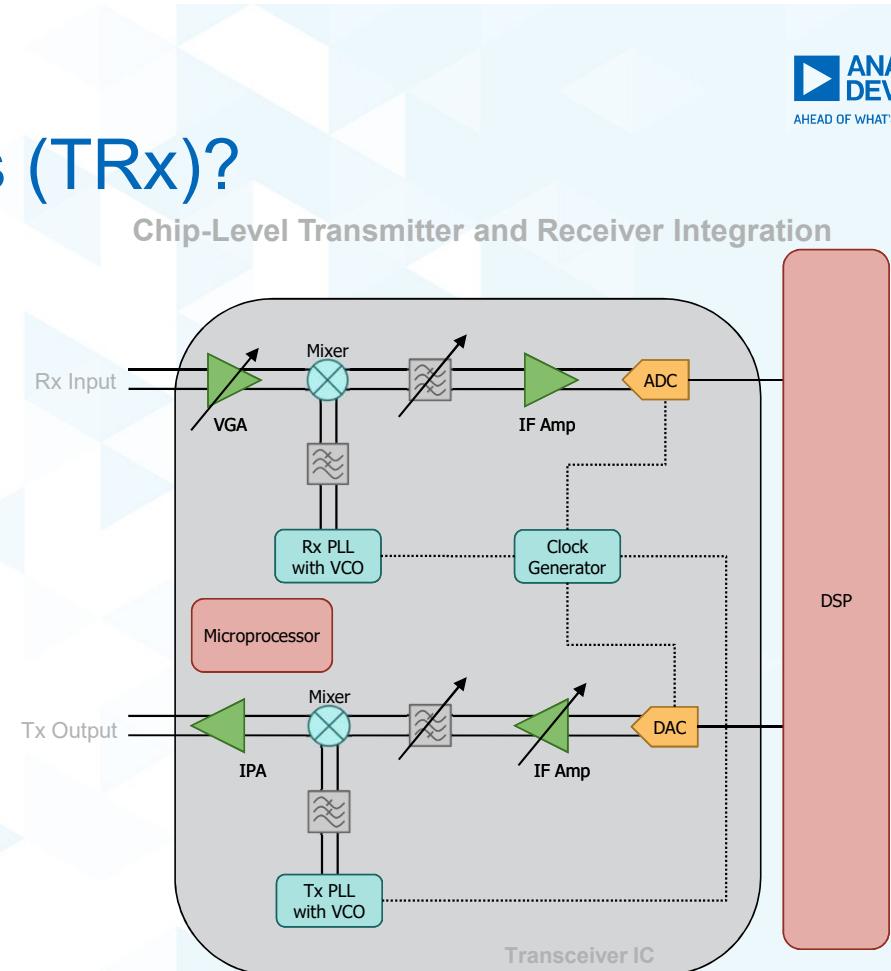
RF Transceivers Enable Forced Spurious Decorrelation in Digital Beamforming Phased Arrays [5]



Transceiver Integrated Circuits

What Are Integrated Transceivers (TRx)?

- Single-chip ICs which contain:
 - Full Rx signal chains
 - ADCs & ADC interface to baseband
 - Down-convert mixers
 - Variable digital or analog filters
 - Variable gain amplifiers or attenuators
 - Full Tx signal chains
 - DACs & DAC interface to baseband
 - Up-convert mixers
 - Variable digital and/or analog filters
 - Variable gain amplifiers and/or attenuators
 - On-chip PLLs allow for complete system solution
 - On-chip microprocessors for system calibrations
 - General-purpose input/output (GPIO) connections
 - To monitor Rx or Tx status
 - To enable automatic gain control
 - To quickly issue frequency hops or system response

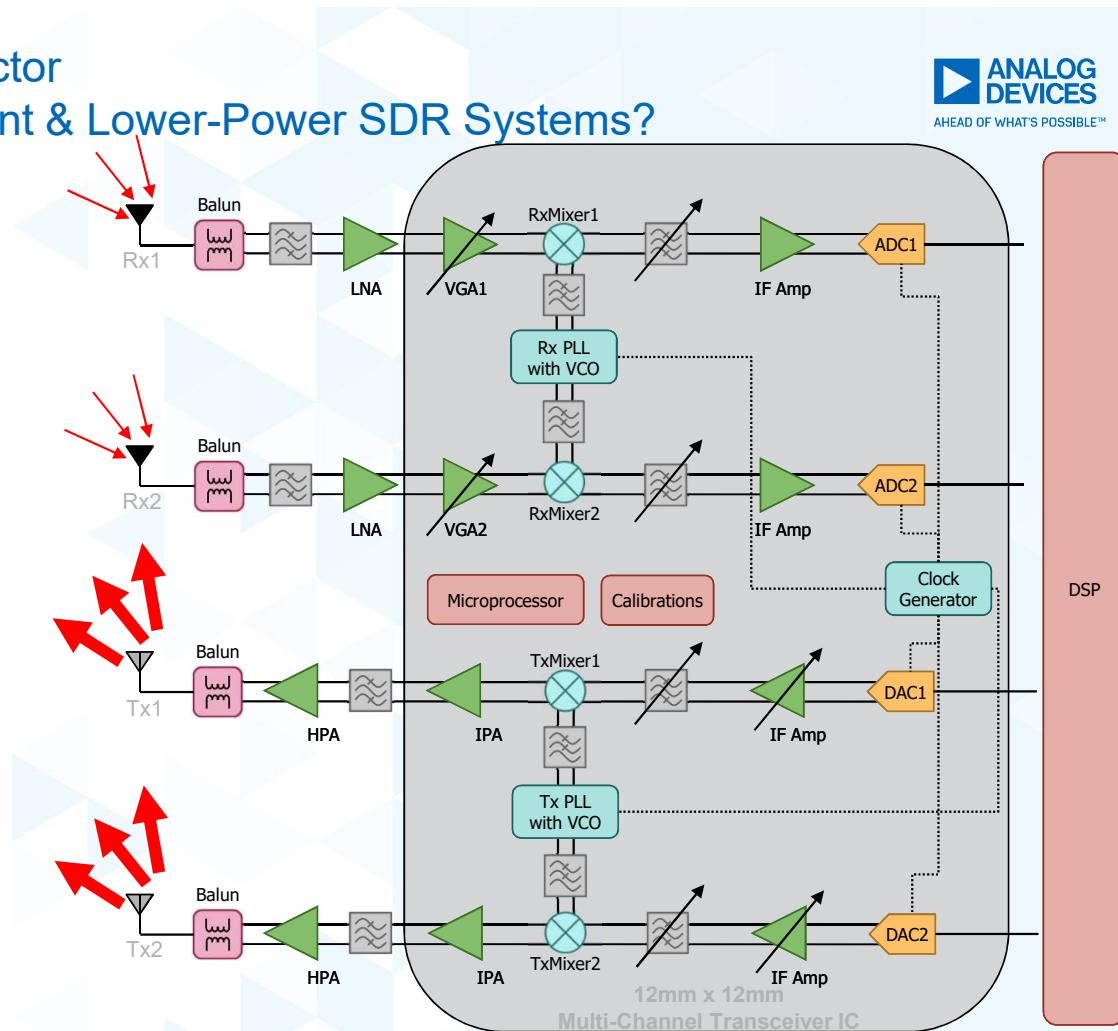


Transceivers for Low Power & Small Form Factor

How Does Integration Lead to Smaller-Footprint & Lower-Power SDR Systems?



- ▶ TRx ICs enable low-SWaP SDR systems
 - Multiple Rx & Tx channels available on-chip
 - Can serve as backbone to phased-array systems
- ▶ Built-in calibration algorithms
 - Facilitate system-level calibrations
 - Digital pre-distortion (DPD)
 - Spurious rejection algorithms
 - Improve system dynamic range & spurious
- ▶ Application programming interface (API)
 - Vetted software to control the radio
 - Capable of being incorporated into end design
- ▶ JESD204 interface
 - Developed hardware description language (HDL)
 - Easily integrate with FPGA or ASIC BBP



ADRV9009: Highly Agile Wideband Integrated RF Transceiver

Integrated Dual Rx and Dual Tx

- LO Range: 75 MHz < Fc < 6GHz
- Max Rx BW = 200MHz
- Max Tx BW = 450MHz, Primary Signal BW = 200MHz
- Max Orx BW = 450MHz

Integrated Clock Generation

- Frequency Agile
- Rx / Tx Local Oscillator
- 16 bit ADC/DAC
- Accepted Clocks up to 1GHz

Digital Features

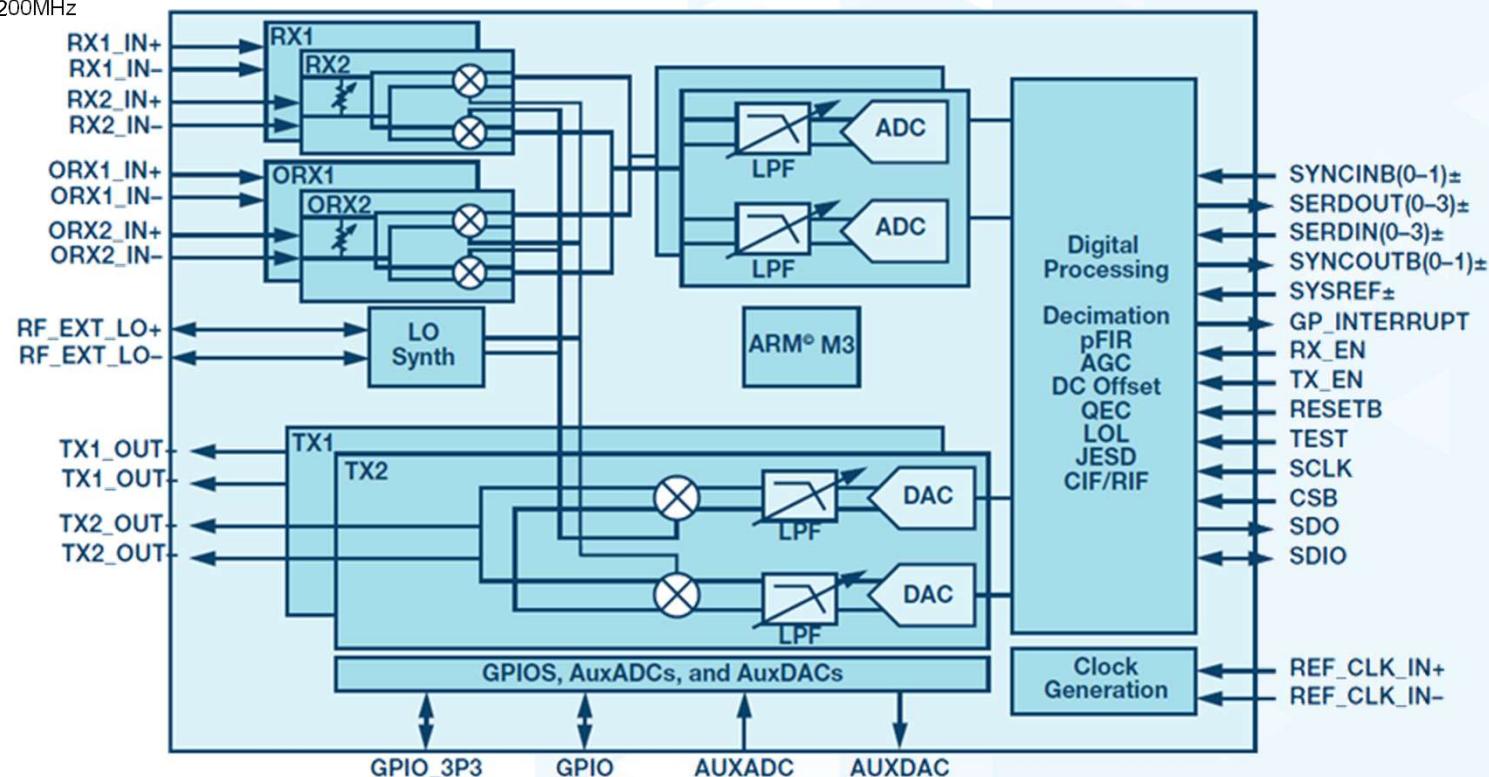
- Rx: DC Offset, QEC, AGC
- Tx: LO leakage, QEC
- Programmable FIRs
- 12.288 Gbit/s JESD204-B interface
- Embedded ARM

GPIOs

- AUX DAC, AUX ADCs
- GPIO
- Rx MGC, AGC (Hybrid)

Low power:

- 3.5W RX only
- 3.7W TX only
- 5.6W TX+Orx
- Less in TDD



Analog Devices RF SOM (System on Module)

Production Ready Module, MIL-202 qualified

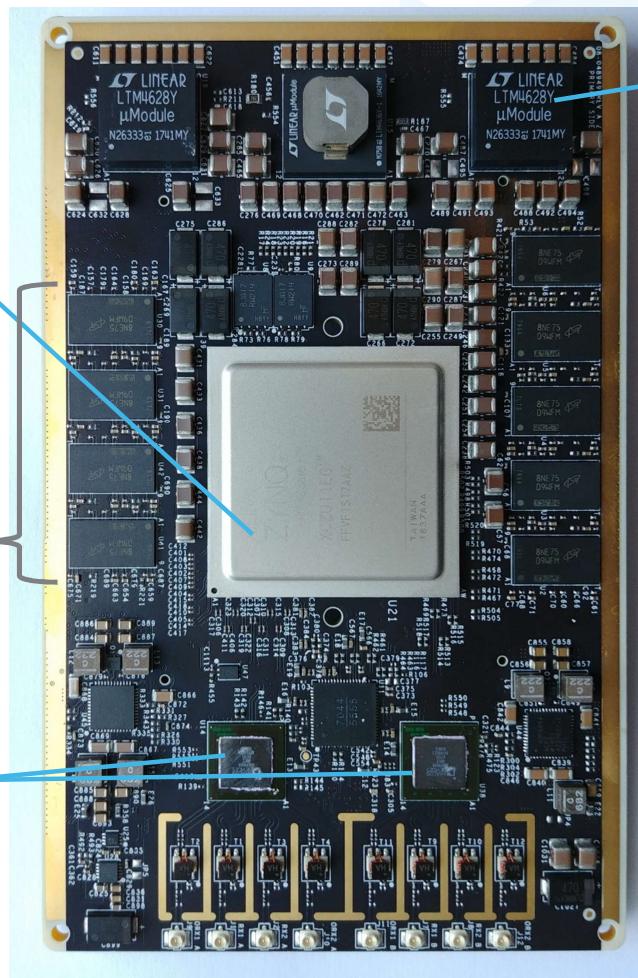


ADRV9009-ZU11EG RF SOM : \$7999

- Processor
 - Quad Core ARM Cortex A53 (1.5 GHz each)
 - L1 cache : 32 KB Instruction, 32 KB Data
 - L2 cache : 512 KB
- Processor
 - Dual ARM R5 (600 MHz each)
 - L1 cache : 32 KB Instruction, 32 KB Data
 - 128KB Memory per core
- GPU : Mali-400 MP2 up to 667MHz
 - L2 Cache 64KB
- FPGA
 - Kintex Ultrascale+ Fabric
 - 653k Logic Cells
 - 52.7 Mb Block RAM
 - 2,928 DSP Slices
 - Vivado license required
- 2 Banks of 2 Gbyte (x32) DDR4 for PL (Radio)
- 128 Mbyte SPI Flash
- MicroSD Card (lockable)

Xilinx ZU11EG

ADI ADRV9009



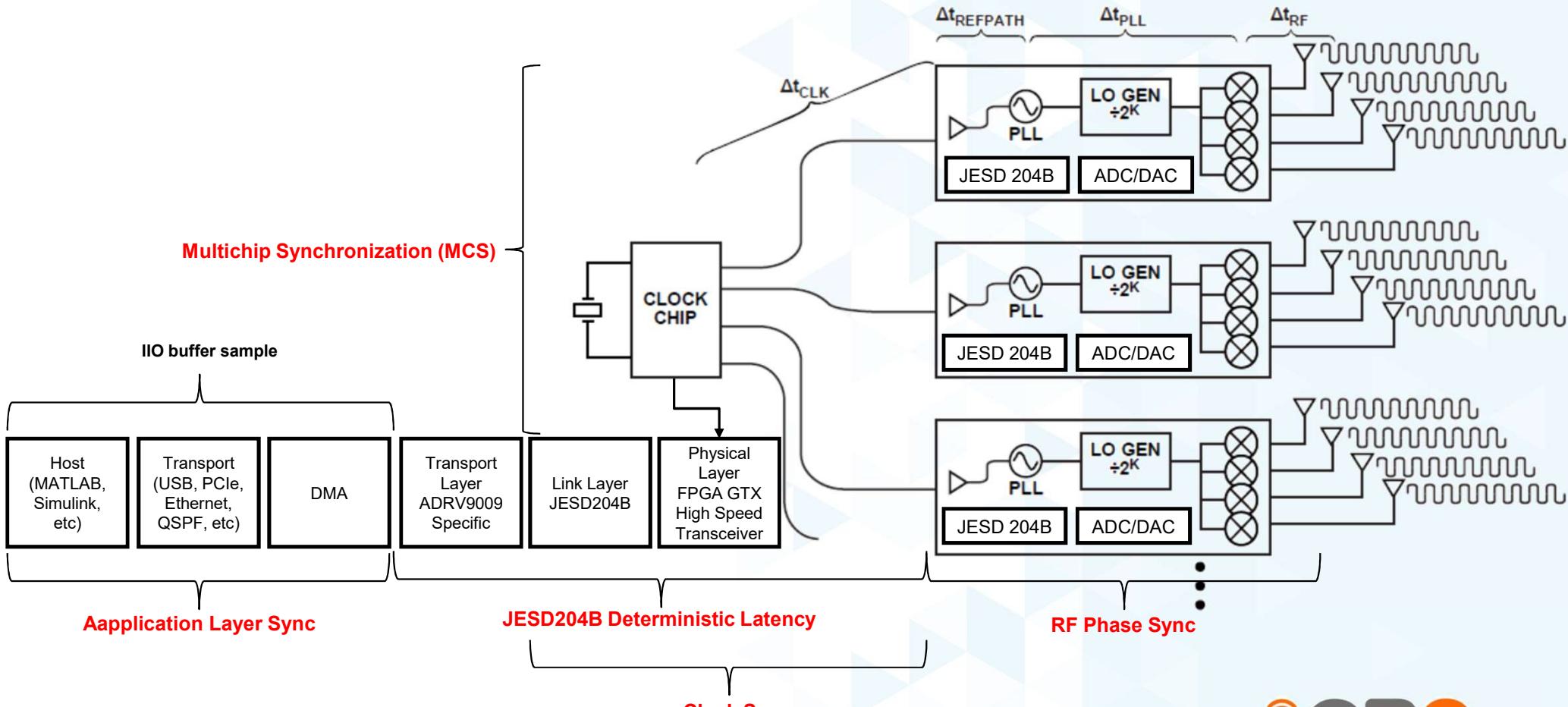
Power Modules

- 12V input
- 4 Gbyte DDR4 + ECC for Processors
- 128 Mbyte SPI Flash
- USB 2.0 (OTG Controller + Phy)
- 4 x GTR share among:
 - PCIe® Gen2 x4,
 - 2x USB3.0,
 - SATA 3.1,
 - DisplayPort,
- 4x Tri-mode Gigabit Ethernet
 - 1 x 10/100/1000 Ethernet Phy
- 2xUSB 2.0
 - 1 USB 2.0 Phy
- 2x SD/SDIO
 - 1x MicroSD Card (lockable)
- 2x UART,
- 2x CAN 2.0B,
- 2x I2C,
- 2x SPI,
- 4x 32b GPIO
- 24 x GTH (12.5 Gb/s)
 - 2x 100G Ethernet MAC/PCS w/RS-FEC
 - PCI Express® Gen 3 (x16)
 - External JESD204B ADRV9009 Devices

- Full Linux based reference design
- Fully integrated and tested system
- Common connector
- Digital I/O pins :
- U.FL connectors : 20

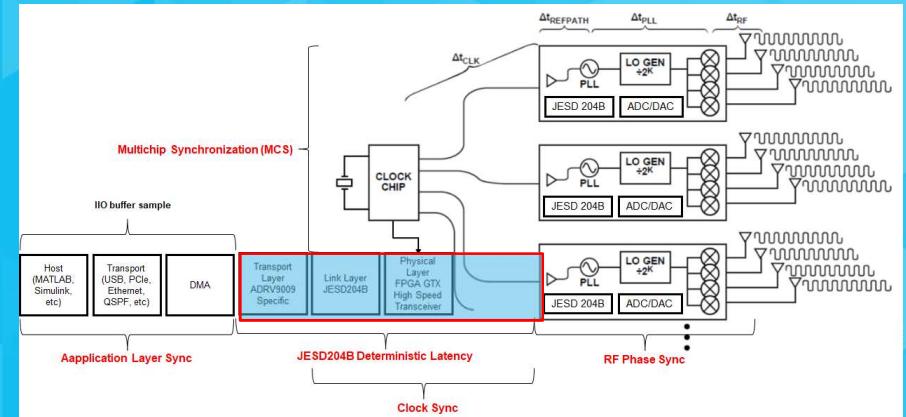


Synchronization For Many Channel System



JESD204B

Digital Interface synchronization



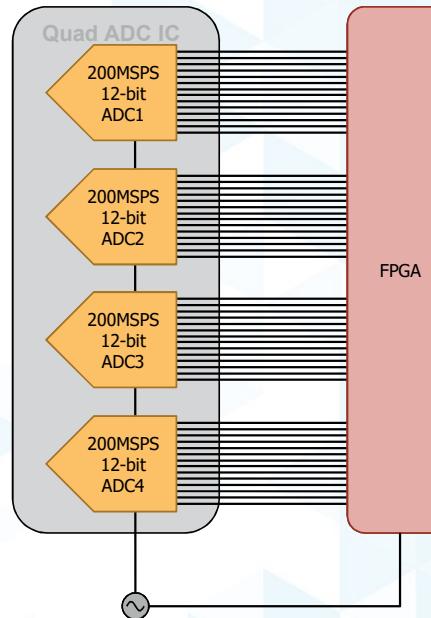
High-Speed Converter / FPGA / ASIC Interfaces

How Do Converters Communicate With the Baseband Interfaces?

- ▶ Faster rates increase converter data volume
- ▶ Data sent to baseband processor (BBP)
 - Field programmable gate array (FPGA)
 - Application-specific integrated circuit (ASIC)
- ▶ Historically done with parallel interfaces:
 - Low-voltage differential signal (LVDS) > 200MSPS
 - Complementary metal-oxide semiconductor (CMOS)
- ▶ Newer JESD204 serialized standard simplifies:
 - Board layout (fewer number of traces for interface)
 - Provides deterministic latency
 - Scalable to increasing sample rates & channel counts

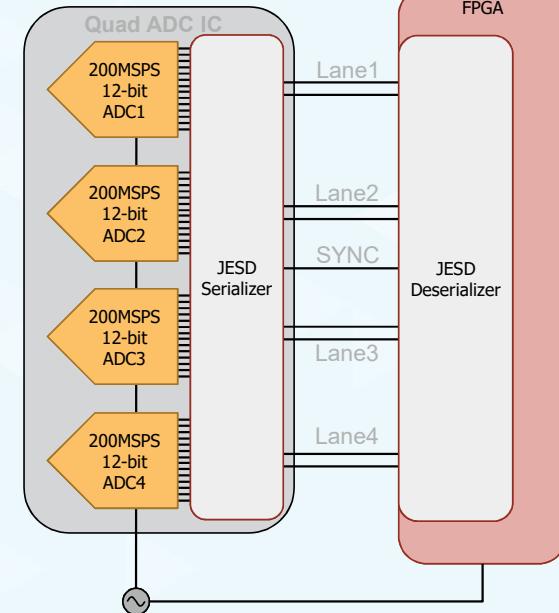
Historical LVDS With Quad-ADC

- Requires Equal Trace Lengths
- Changing Converter Resolution/Count Necessitates Complete Hardware Redesign



Newer Serialized JESD204B/C

- Fewer Traces Required
- Scalable For Additional Channels
- Scalable For Changing Converter Resolution



JESD204 Standard

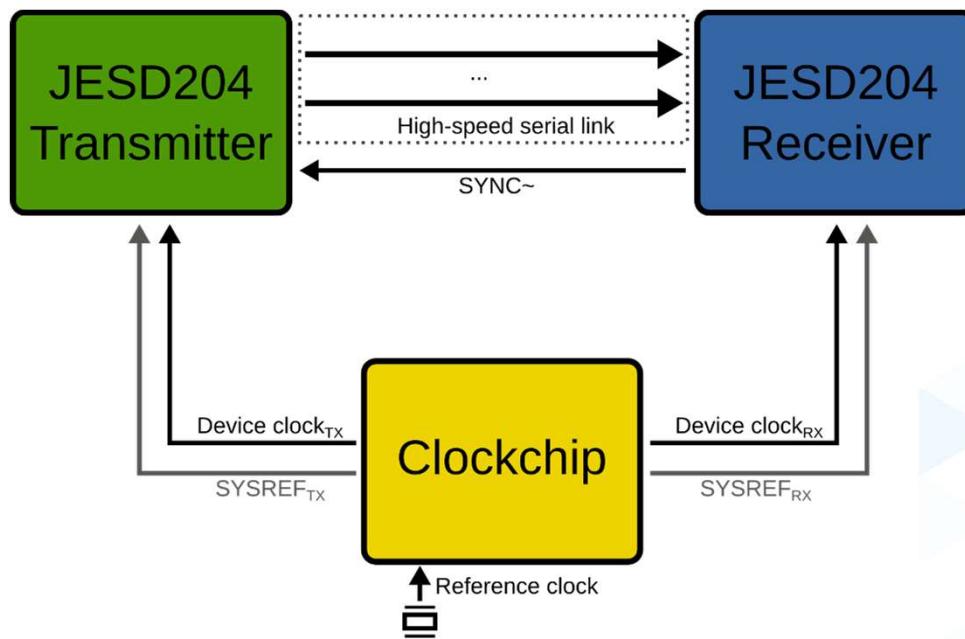


- ▶ **Designed as high-speed serial data link between converter (ADC, DAC) and logic device**
 - Up to 32 lanes per link
 - Up to 32 Gbps (raw) per lane
- ▶ Describes data mapping and framing
- ▶ Multi-chip synchronization
- ▶ Deterministic latency

- ▶ 2006: JESD204
 - 1 lane, 3.125Gbps
- ▶ 2008: JESD204A
 - Multi-lane, 3.125 Gbps
- ▶ 2012: JESD204B
 - Multi-lane, 12.5 Gbps
 - Deterministic latency
 - Subclass 0, 1, 2
 - More flexible clocking scheme
- ▶ 2017: JESD204C
 - Multi-lane, 32 Gbps
 - 64b/66b and 64b/80b encoding
 - Forward Error Correction

JESD204 Architecture

Overview



Layers



Application specific processing

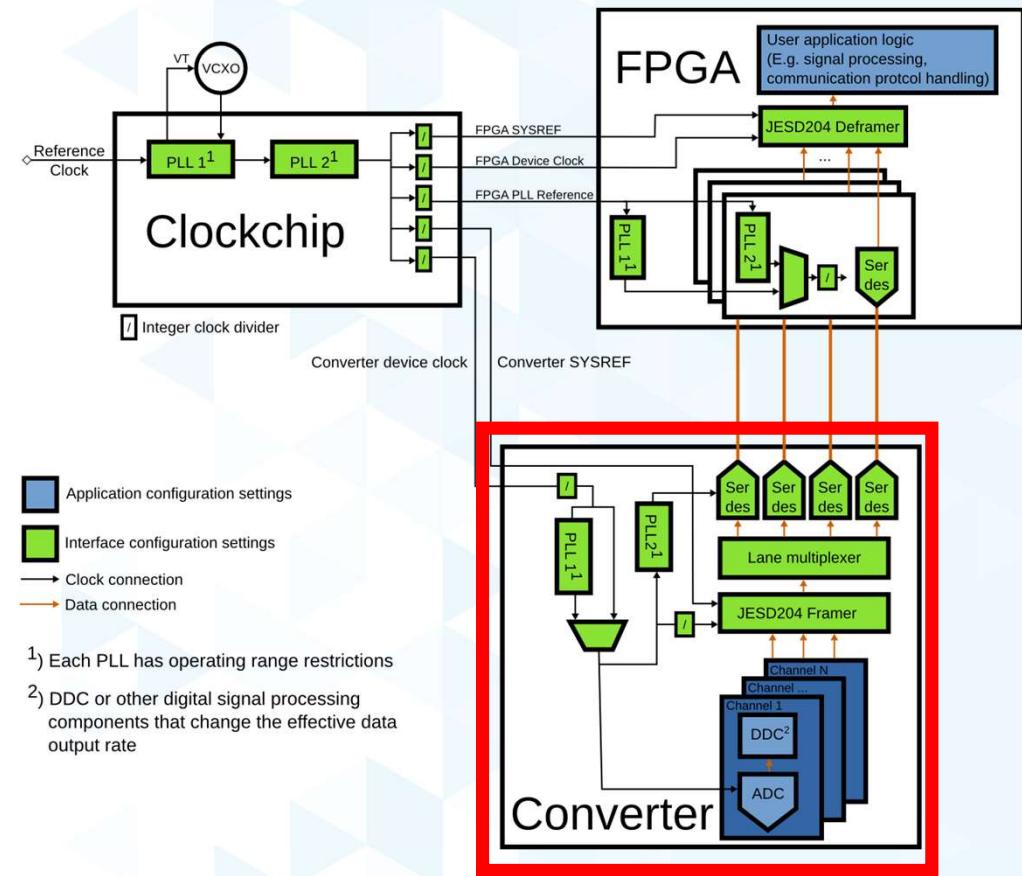
Sample framing
Lane mapping

Scrambling
Character replacement
8b/10b encoding

High-speed SerDes
Clock recovery
Signal shaping

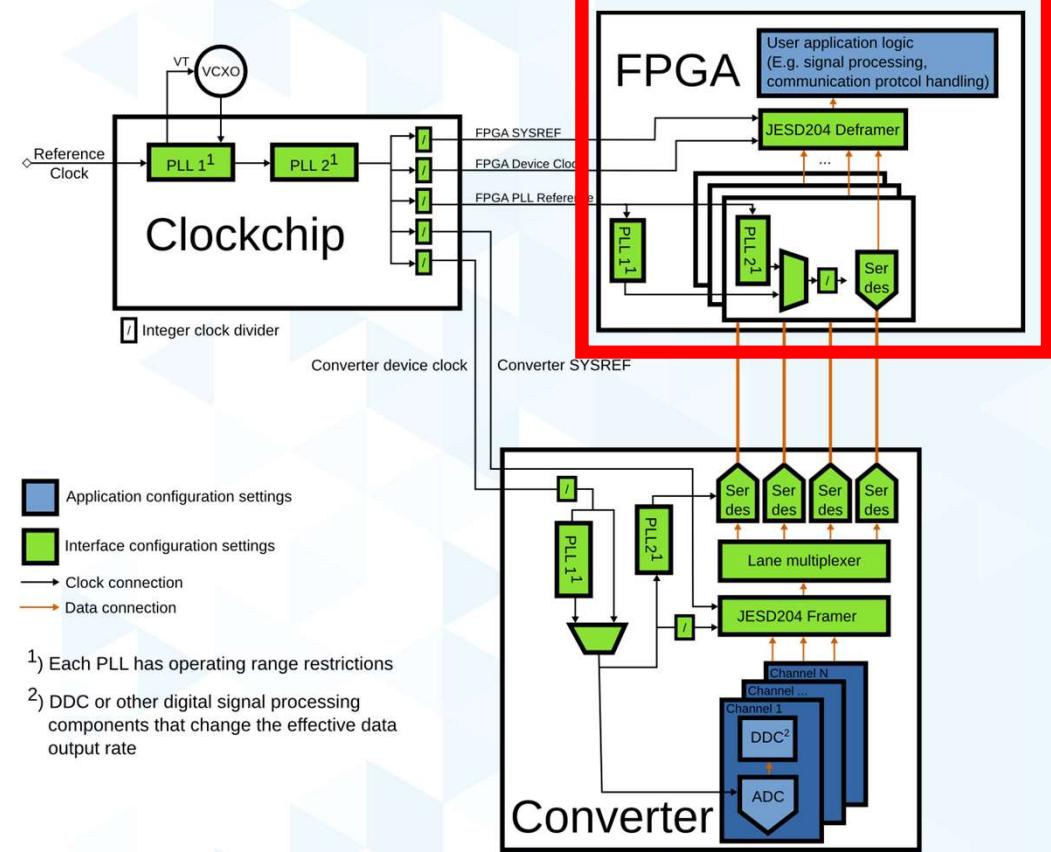
Converter Device

- ▶ Does either A2D or D2A conversion
- ▶ Contains one or more converters
 - All synchronous
- ▶ Modern converter devices often include digital processing



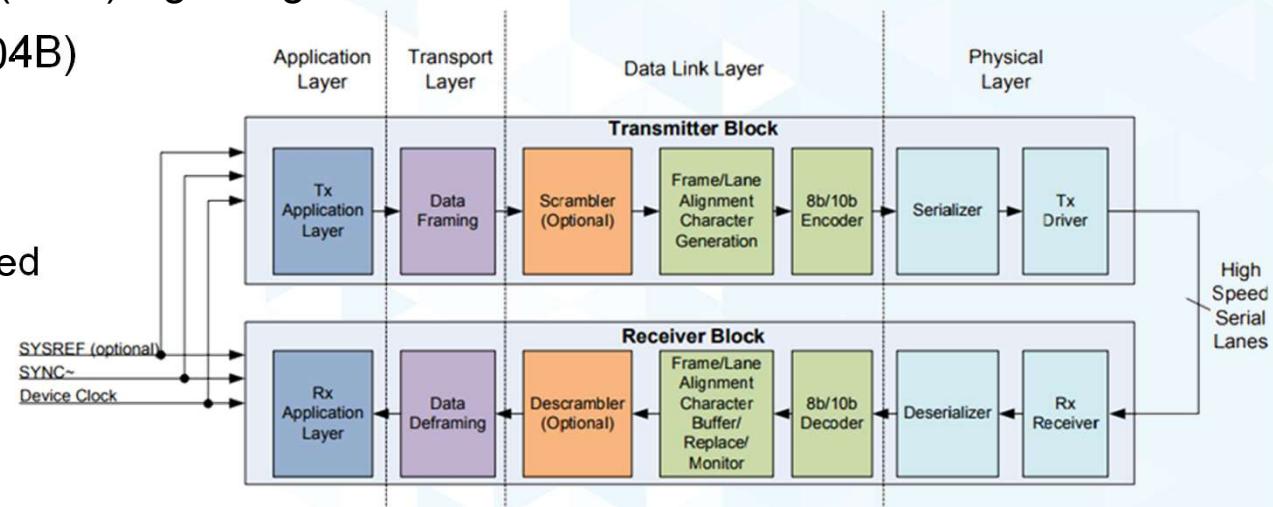
Logic Device

- ▶ Implements digital signal processing
- ▶ Often implemented in a FPGA
- ▶ One logic device can interface multiple synchronous converter devices
 - Multi-point link



Link

- ▶ Link consist of multiple independent lanes
- ▶ Differential current-mode-logic (CML) signaling
- ▶ 8b/10b data encoding (JESD204B)
- ▶ Embedded clock
- ▶ Data scrambling
 - Optional, but highly recommended



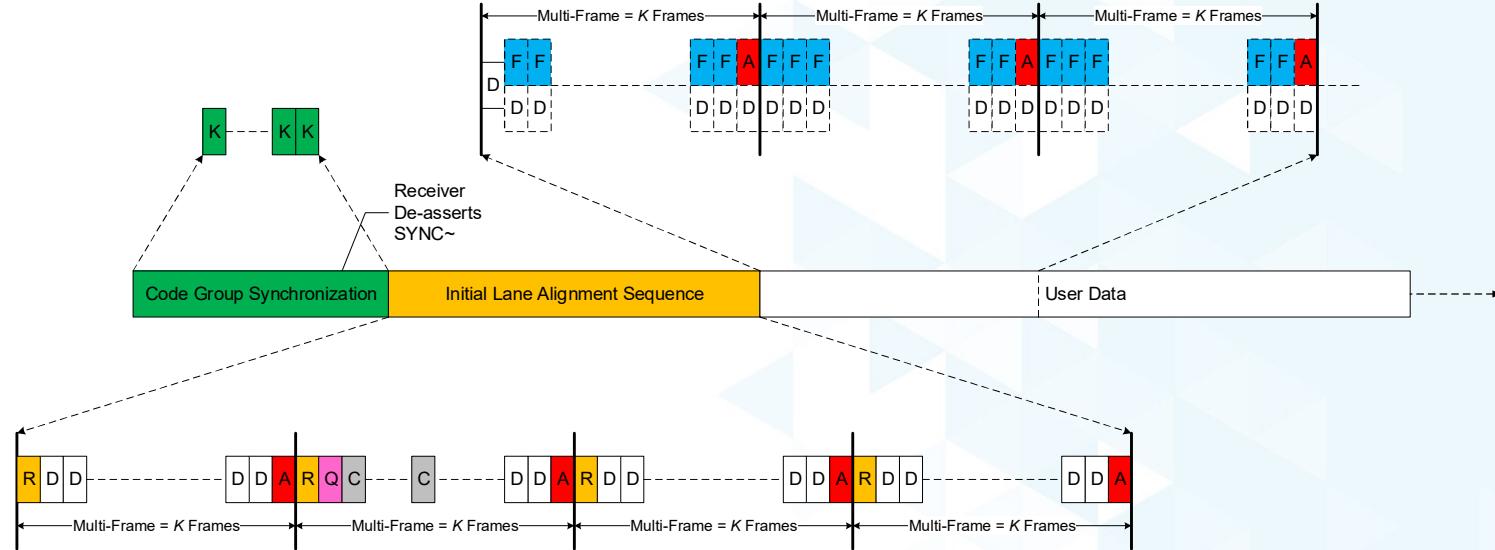
Link/Lane Parameters

Parameter*	Description
DID	Device identification
LID	Lane identification
F	Octets per frame
K	Frames per multi-frame
L	Number of lanes per converter device
N	Converter resolution
N'	Number of bits per sample (recommended to be multiple of 4)
SCR	Scrambling enabled/disabled
HD	High-density (Single sample split over multiple lanes)
JESDV	JESD204 Version (JESD204A, JESD204B)
SUBCLASSV	JESD204B Subclass (0, 1, 2)

* Table is a excerpt of the most important parameters

- Parameters are used to describe the link and lane configuration

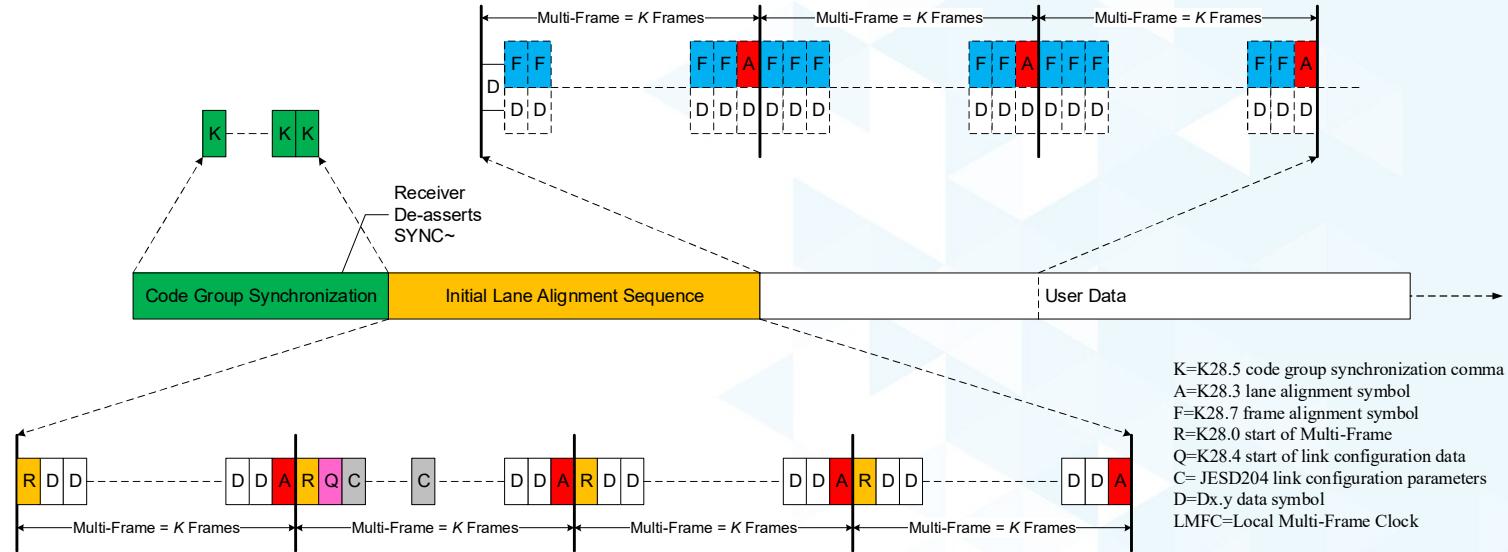
Link Synchronization



- ▶ Receiver asserts SYNC
 - ▶ Transmitter repeatedly sends /K/ character
 - ▶ Receiver performs CGS and character alignment
 - ▶ Receiver de-asserts SYNC
 - ▶ Transmitter starts sending ILAS and data

K=K28.5 code group synchronization comma character
A=K28.3 lane alignment symbol
F=K28.7 frame alignment symbol
R=K28.0 start of Multi-Frame
Q=K28.4 start of link configuration data
C= JESD204 link configuration parameters
D=Dx.y data symbol
LMFC=Local Multi-Frame Clock

Initial Lane Alignment Sequence



- After link synchronization the transmitter sends the (Initial Lane Alignment Sequence) ILAS
- Allows verification of link alignment
 - Special control character at the start and end of ILAS multi-frame
- Second ILAS multi-frame contains link configuration parameters
 - Allows to verify configuration and lane mapping

Latency



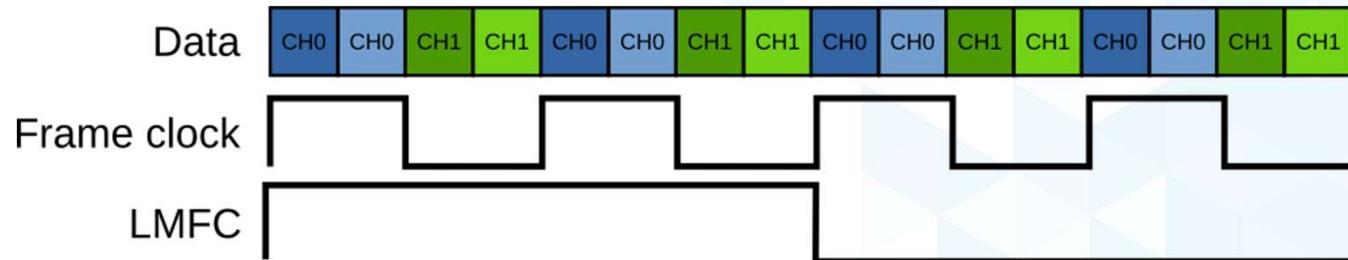
- ▶ Propagating data over the link takes time
- ▶ JESD204 defines latency as the time difference between when the sample is inserted in the TX framer and outputted on the RX defamer
 - Part of the latency is fixed
 - Digital pipeline delays
 - Trace lengths
 - Part of the latency depends on manufacturing and environmental conditions (PVT)
 - PCB propagation delays
 - Process, Voltage, Temperature (PVT)
- ▶ Some systems/algorithms are latency sensitive
 - Closed-loop-control systems
 - RADAR

Deterministic Latency



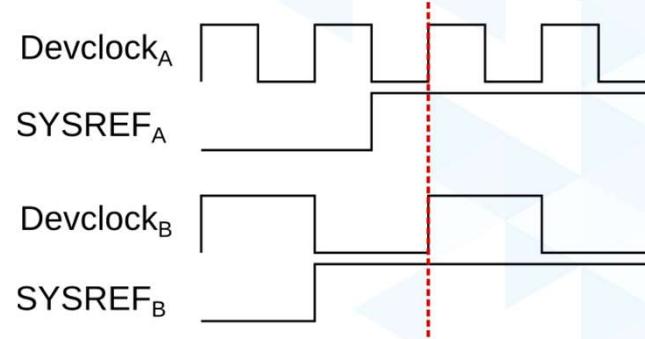
- ▶ **Latency can be defined as deterministic when the time from the input of the JESD204x transmitter to the output of the JESD204x receiver is consistently the same number of clock cycles**
 - In parallel implementations, deterministic latency is rather simple – clocks are carried with the data
 - In serial implementations, multiple clock domains exist, which can cause nondeterminism
- ▶ End-to-End (JESD link) Latency is consistent (and deterministic) across PVT variations and from power-on to power-on
- ▶ Non-deterministic latency components are not removed, but compensated
 - Data is buffered before released to the application layer (elastic buffer)
 - Release happens at deterministic release opportunities
- ▶ Supported by JESD204C and JESD204B subclass 1 and 2

Local Multi-Frame Clock



- ▶ Each JESD204B device generates an internal local multi-frame clock (LMFC)
 - 1-32 frames long
- ▶ Beginning of the LMFC is synchronized externally
 - Subclass 0: N/A (no deterministic latency)
 - Subclass 1: SYSREF
 - Subclass 2: SYNC
- ▶ Internal events are synchronized to the LMFC

SYSREF



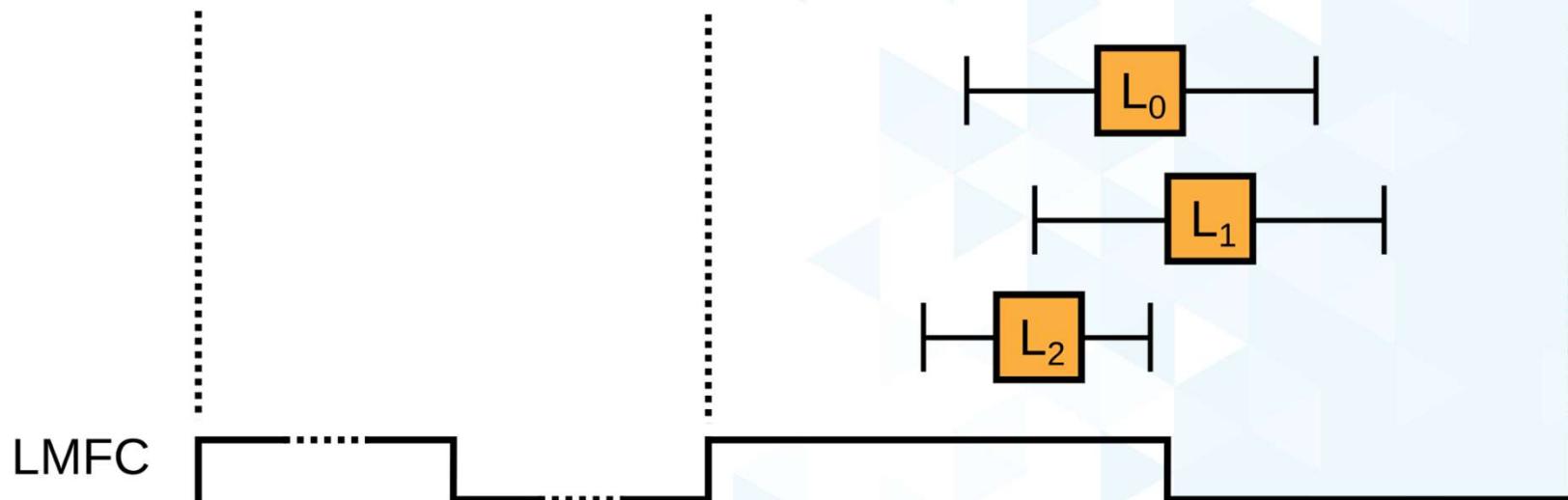
- ▶ SYSREF is used as a synchronization signal
 - In Subclass 1
- ▶ Source synchronous to the device clock
- ▶ Three modes
 - Periodic, gapped periodic, one-shot
- ▶ LMFC is aligned to SYSREF

Deterministic Latency

RX de-asserts SYNC

TX starts sending data

Release opportunity

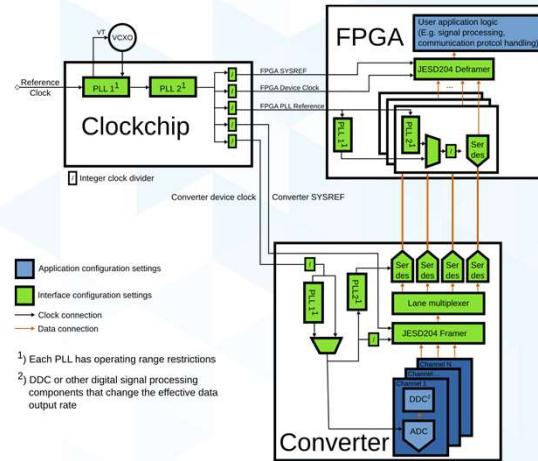


- ▶ Deterministic link latency is achieved by using a elastic buffer with an appropriate data release point.
- ▶ Alignment of all local multi-frame clocks (LMFCs) at the TX and RX devices by SYSREF
- ▶ Release point for the data must be after the last arriving lane (L1)

JESD204 Interface Framework

- ▶ System-level integrated HDL and software framework covering the whole stack
 - Hardware: Reference and rapid prototyping systems
 - HDL: Components for JESD204 protocol handling
 - Software: Drivers to manage clock-chips, converters and HDL
- ▶ Components have been co-designed for improved interoperability
- ▶ Key features
 - Automatic interface configuration based on application settings
 - High-level API
 - Dynamic re-configuration
 - Improved diagnostics
- ▶ ADI provides full stack reference designs
 - Works out of the box
 - Starting point for development of custom designs

JESD204
Interface Framework



Application	Application specific processing
Transport	Sample framing Lane mapping
Link	Scrambling Character replacement 8b/10b encoding High-speed SerDes Clock recovery Signal shaping
Physical	DDC ADC

Third Party Tool Integration	Matlab/Simulink	Python
GNU Radio		
Software Reference Designs	Configures drivers for HDL and hardware reference design	
Software System Libraries	Provides unified interface (API) Implements common system tasks	
Software Drivers	Manages Hardware Components Manages HDL Components	
HDL Reference Designs	Instanciates HDL IP for hardware reference design	
HDL IP Components	Phy Layer Link Layer	Transport Layer DMA
Hardware Reference Desgins	Rapid prototyping boards Evaluation boards	
Hardware Components	Converter Clockchip	Power Analog Frontend

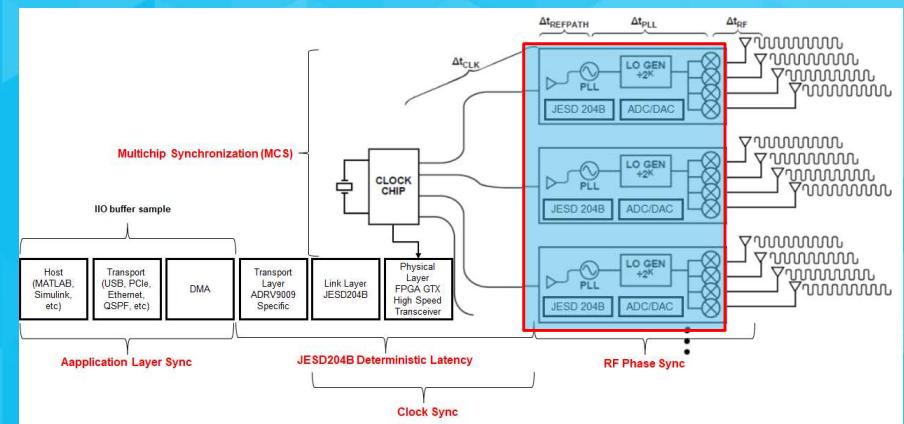
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JESD204 Diagnostics

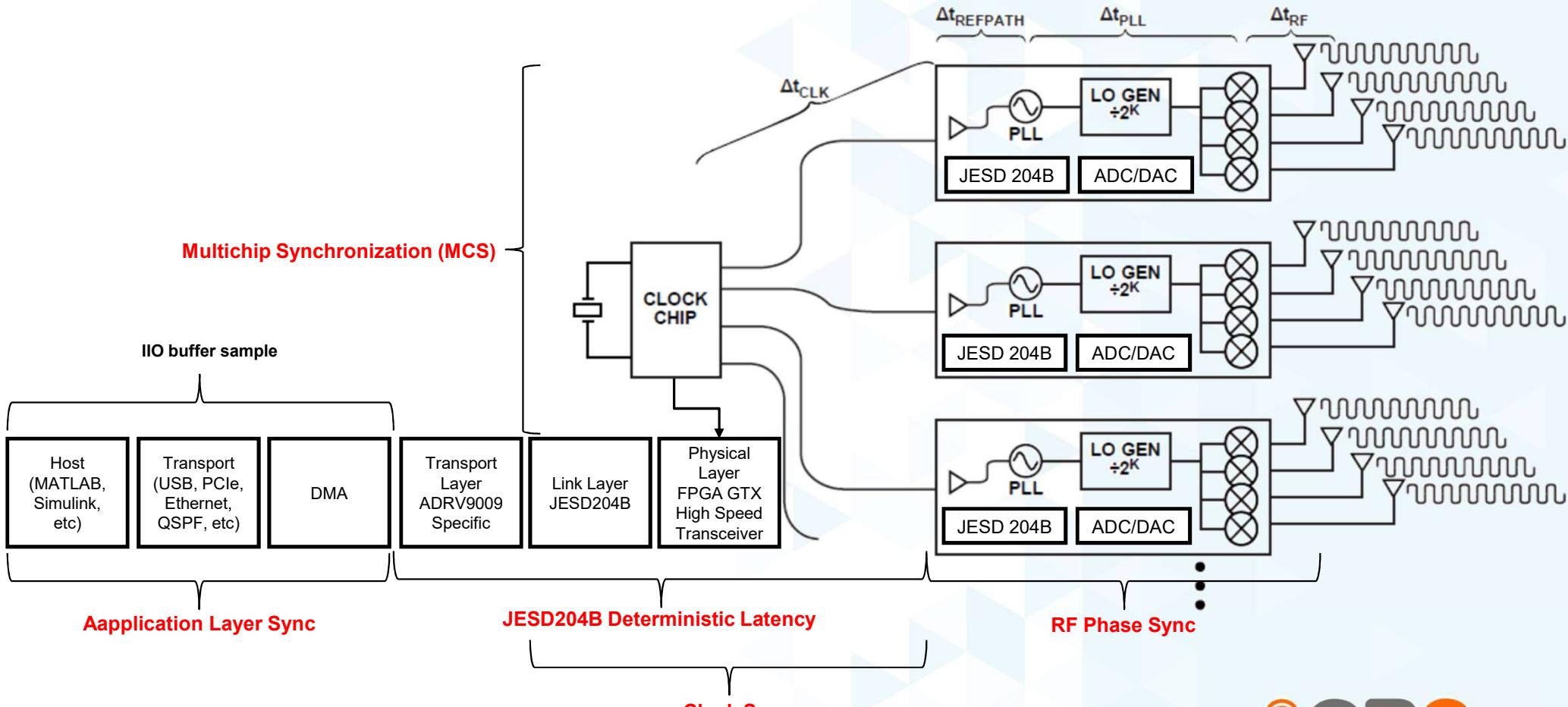
- ▶ Statistical Eyescan, Bit-error-rate monitoring
 - Detect electrical signal integrity issues
- ▶ Clock rate monitoring for all system clocks
 - Detect bad clock wiring
 - Detect clock failures
- ▶ Initial lane sequence monitoring and verification
 - Detect lane swaps
- ▶ Lane arrival monitoring (relative to SYSREF)
 - Detect potential sources of non-deterministic latency
- ▶ SYSREF alignment monitoring
 - Detect SYSREF timing and configuration issues
- ▶ Continuous monitoring
 - Application is notified as soon as failure occurs



Multichip Synchronization

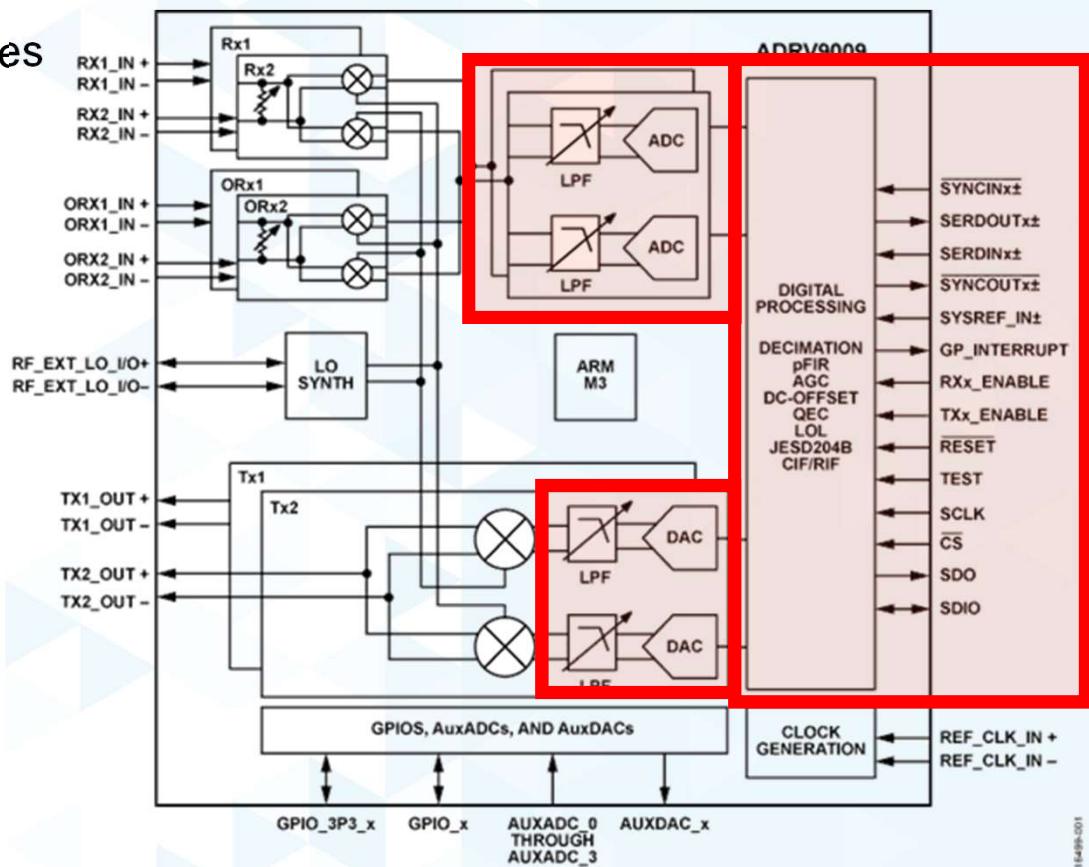


Synchronization For Many Channel System

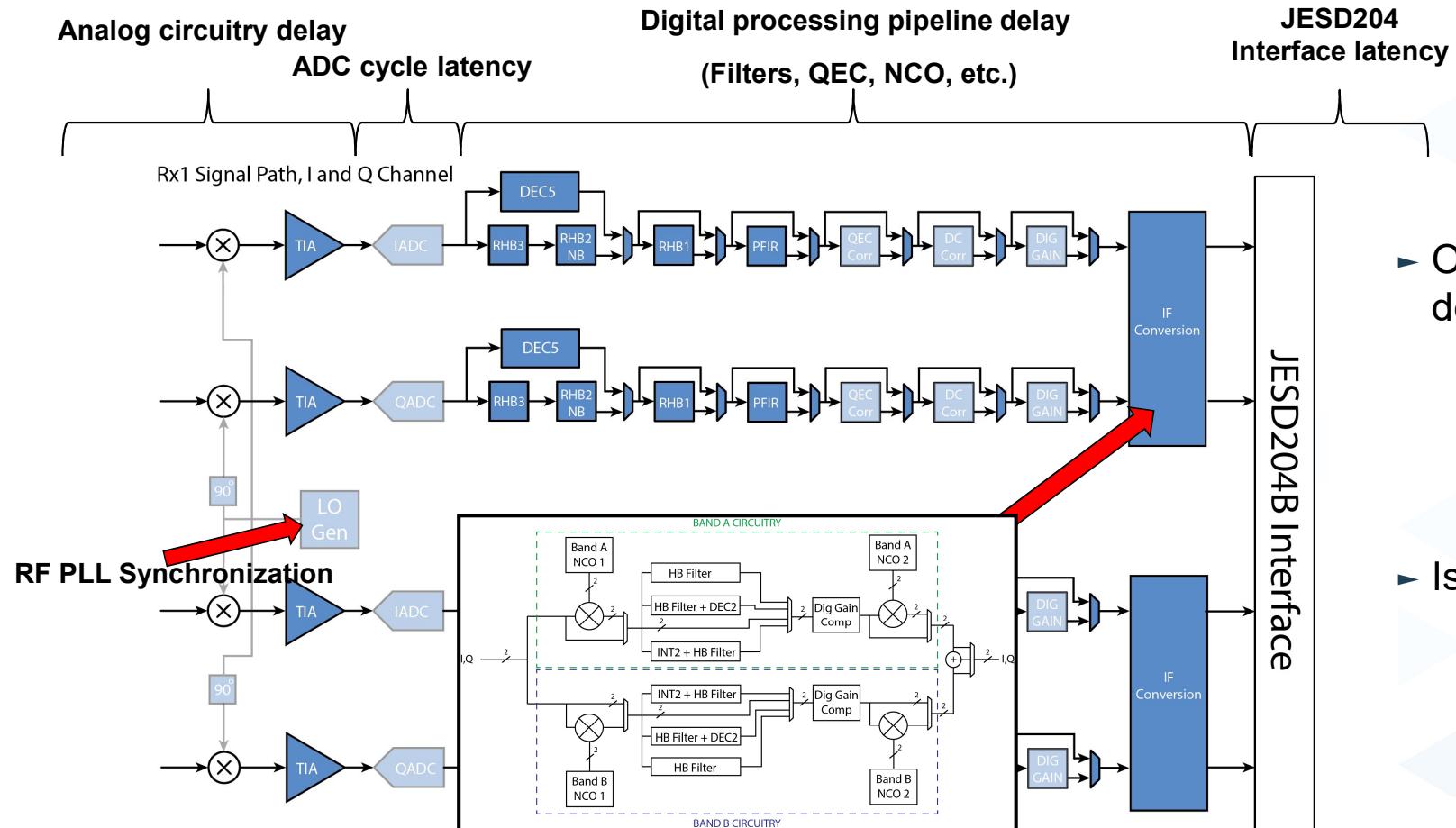


Multichip Synchronization

- ▶ Multichip Synchronization (MCS) synchronizes baseband data paths of multiple devices
- ▶ Accomplished through SYSREF, REF_CLK and JESD deterministic latency
- ▶ Controlled through API functions
- ▶ Provides synchronization for:
 - Device clock dividers
 - High speed digital clock divider
 - BB PLLs (ADCs/DACs)
 - NCOs
 - JESD LMFC
 - RF PLLs phases
 - Gain control AGC
 - State machines

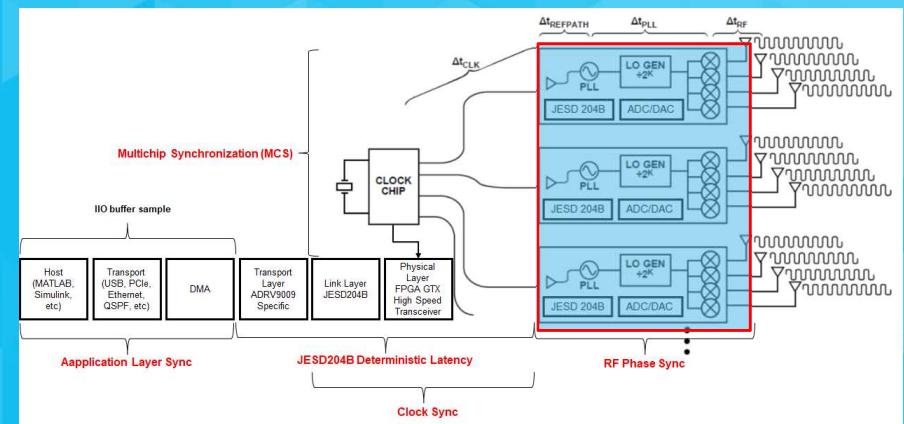


Integrated RF Transceiver latencies



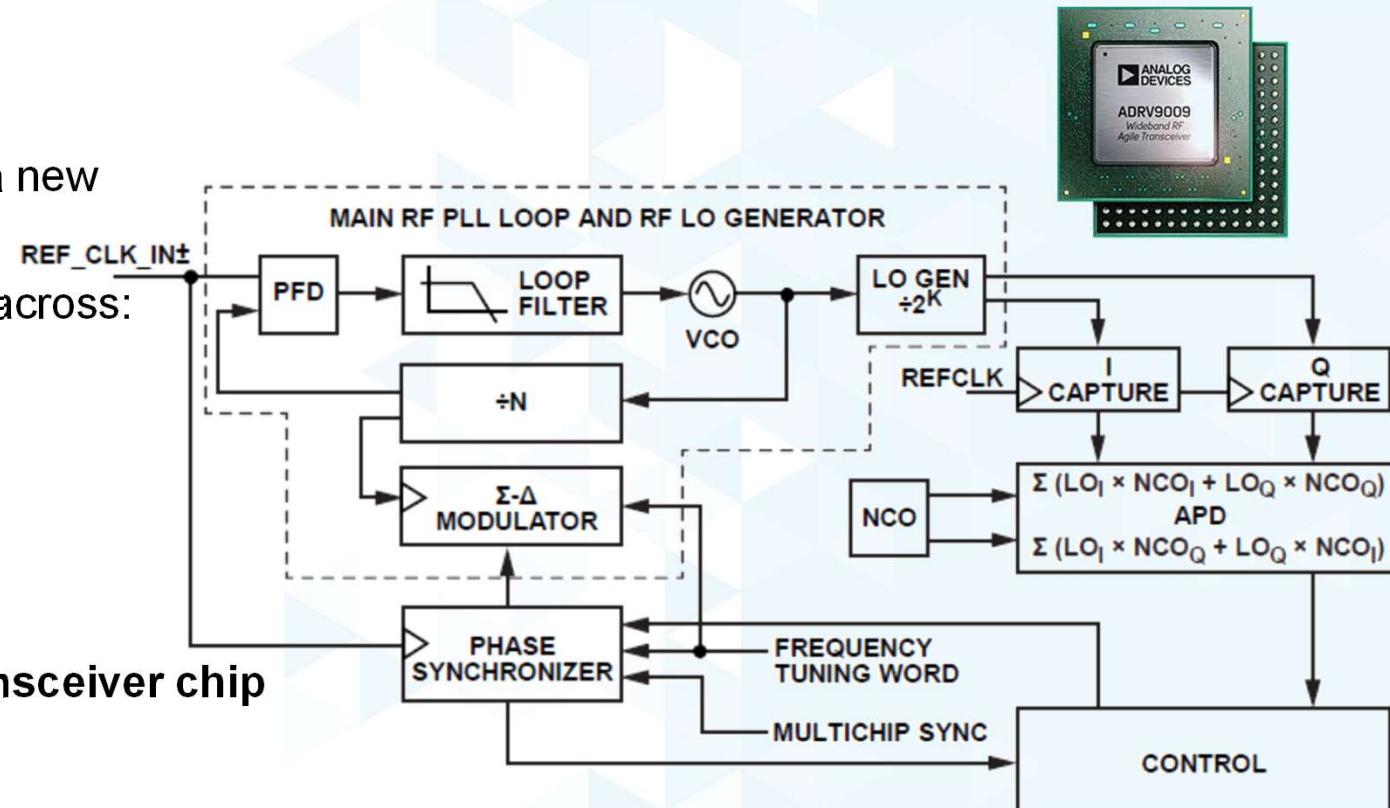
- Overall Latency depends on
 - BB Rate
 - ADC clock
 - Filter settings
- Is deterministic

RF Phase Synchronization

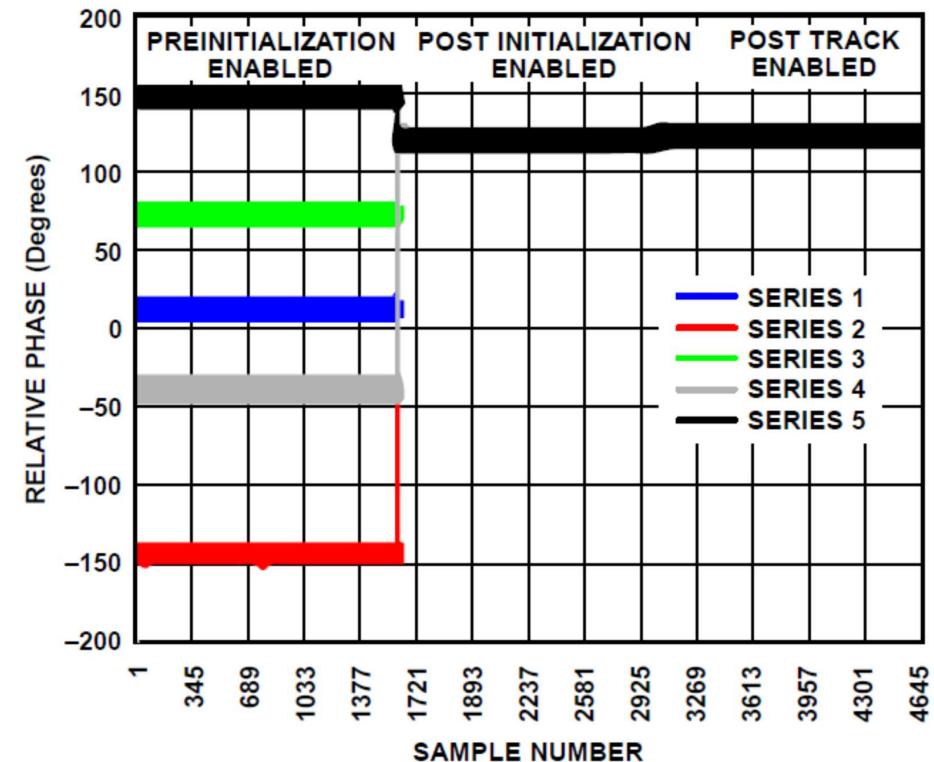
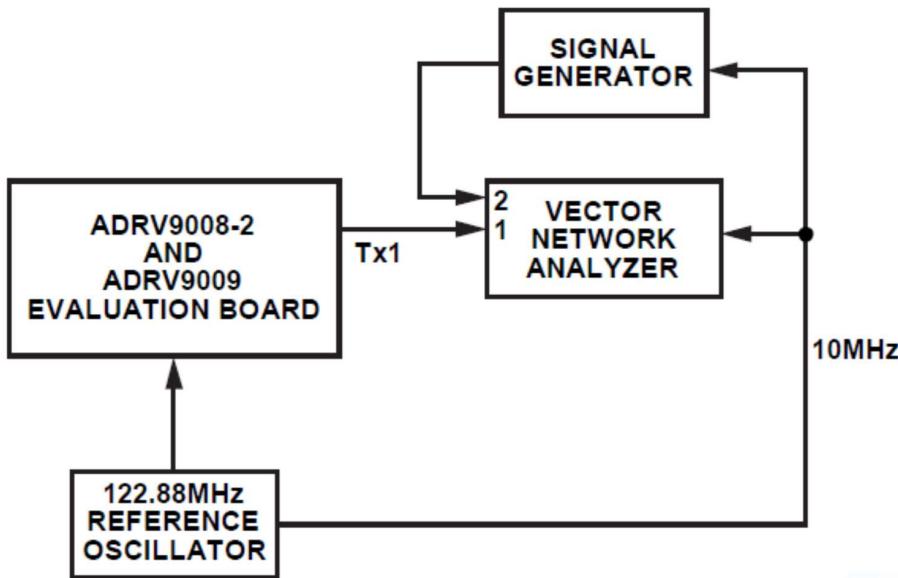


RF PLL Synchronization

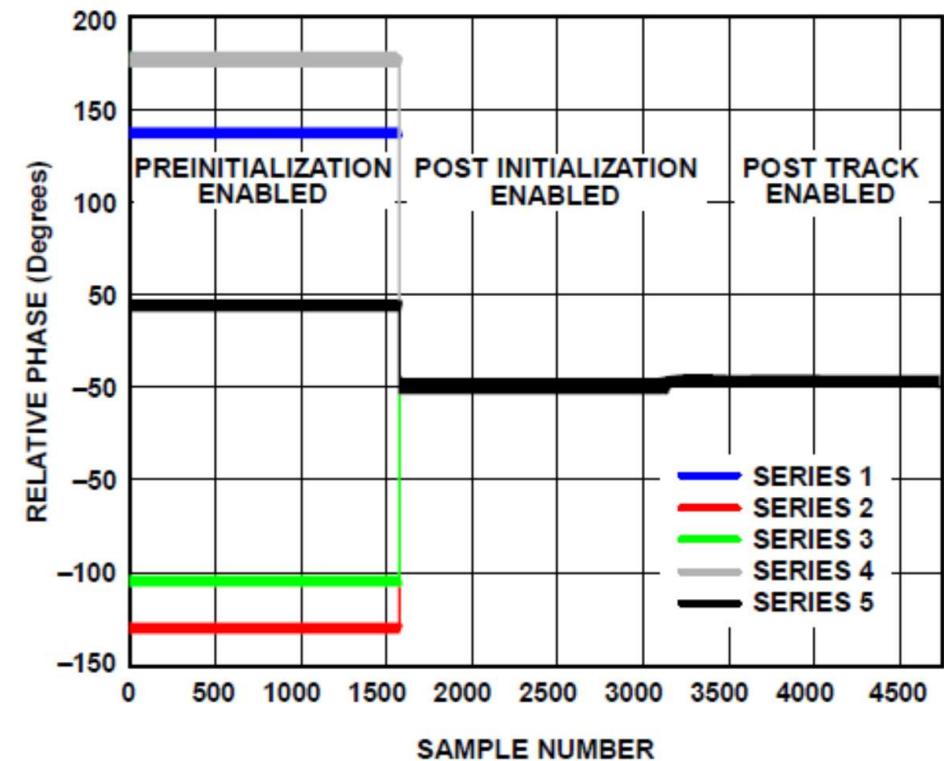
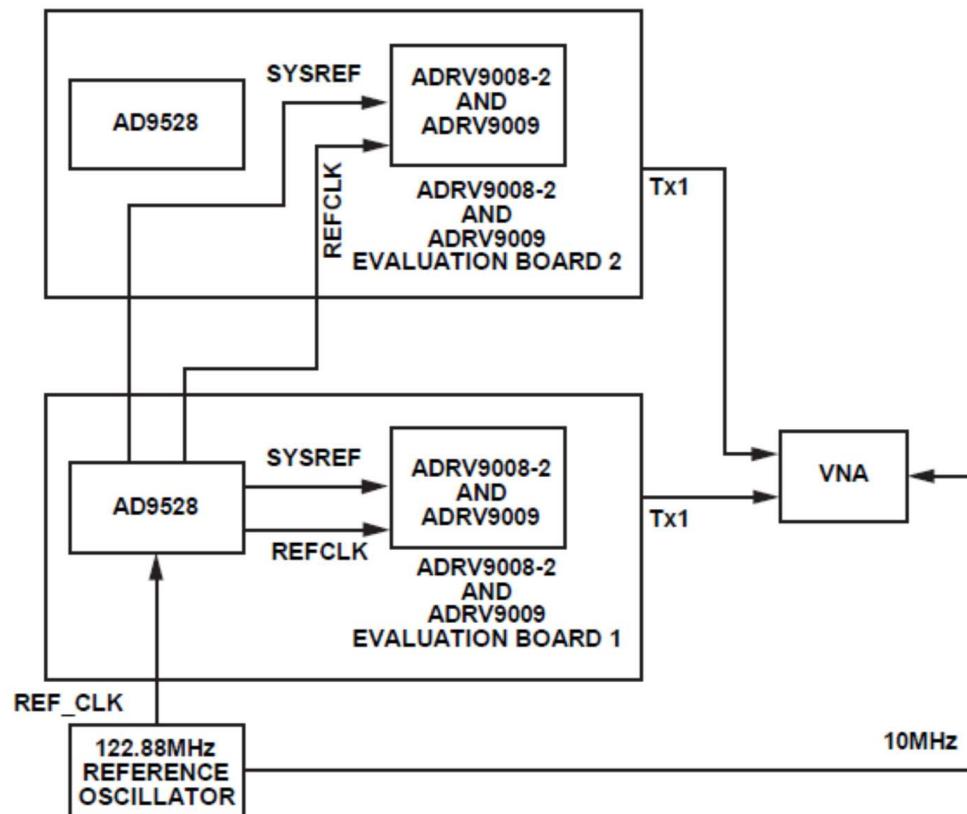
- ▶ RF phase synchronization is a new transceiver feature
- ▶ Provides deterministic phase across:
 - Power cycles
 - LO frequency changes
 - Initializations
 - Temperature
- ▶ Works across multiple TRX.
- ▶ **Phase is unique to each transceiver chip**



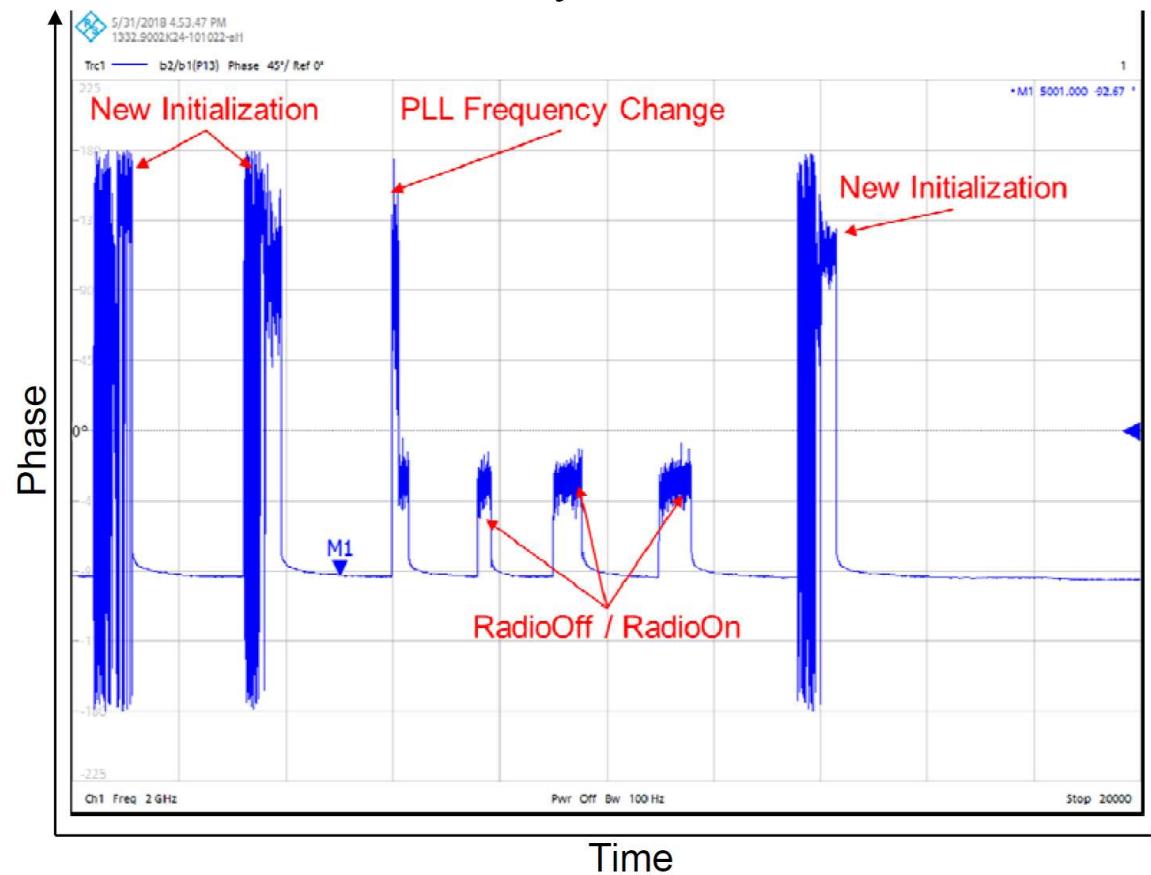
Phase Synchronization of Single ADRV9009 Over Power Cycles



Phase Synchronization Between ADRV9009s

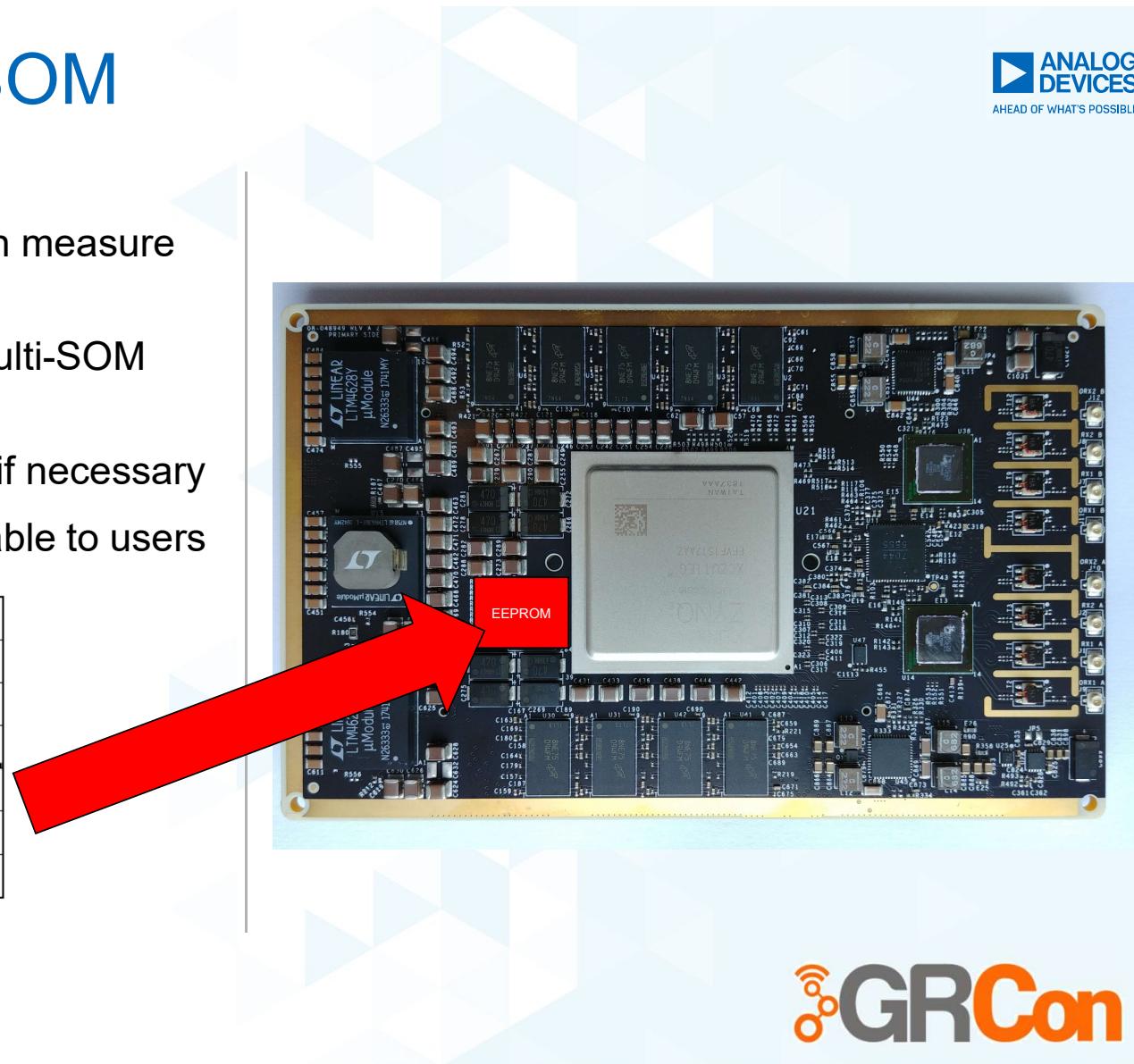
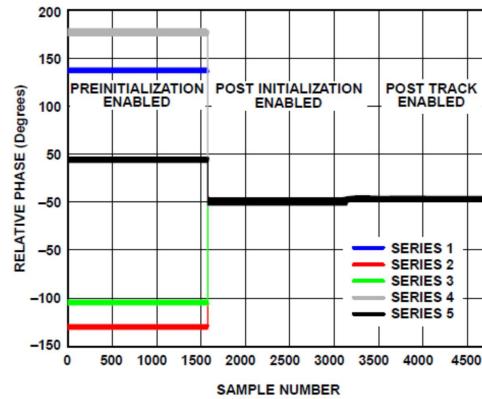


ADRV9009 RF PLL phase synchronization



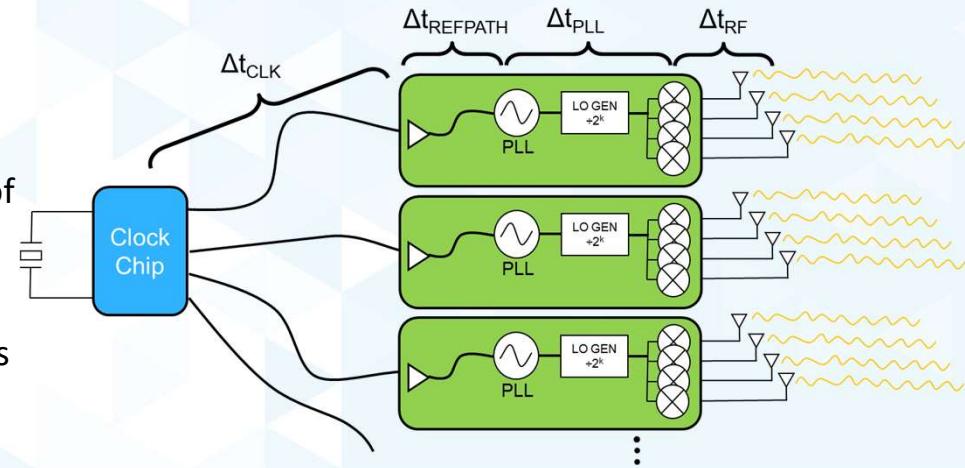
Phase Offsets and SOM

- SOM can be factory calibration with measure offset provided in EEPROM
- Calibrated phases allow aligned multi-SOM synchronization
- EEPROM can be updated by user if necessary
- Calibration procedure will be available to users

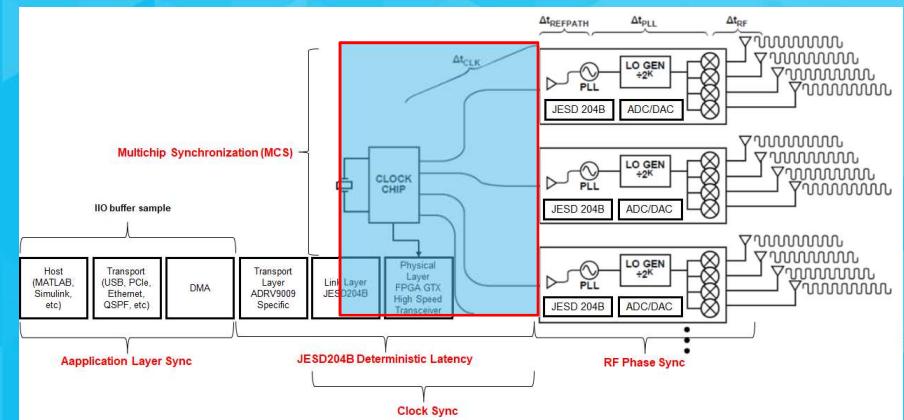


System considerations

- Overall phase synchronization is determined by a number of factors
 - Board level clock routing (t_{CLK})
 - On-chip reference path routing ($t_{REFPATH}$)
 - PLL and LO divider path (t_{PLL})
 - RF & antenna paths (t_{RF})
- The LO phase synchronization method addresses **the initial PLL phase and LO divider state** and reduces their **temperature dependence** to a negligible amount compared to other sources of phase drift in the system
- In a beamforming/MIMO system, there is a system level antenna calibration which is performed to equalize the sum of these paths between all channels. The goals of this transceiver mechanism are:
 - Reduce the complexity of the antenna calibration by initializing to a more **consistent startup condition** with deterministic PLL phase and LO divider state.
 - Reduce the temperature dependence of the system phase synchronization to allow the **antenna calibration to run less frequently** during operation.
 - Allow transceivers to be **stopped and started in an operational system** and “hot synchronize” with the other transceiver elements.



Distributed Multichip Clock Synchronization



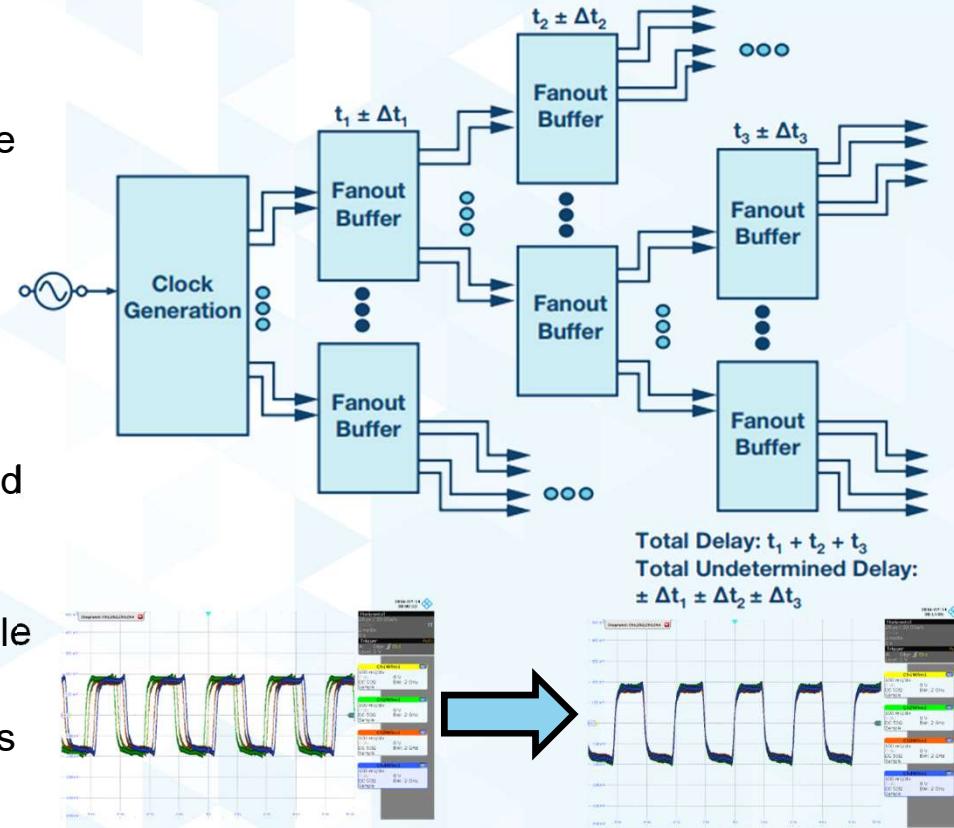
Distributed Multichip Clock Synchronization

► Requirements

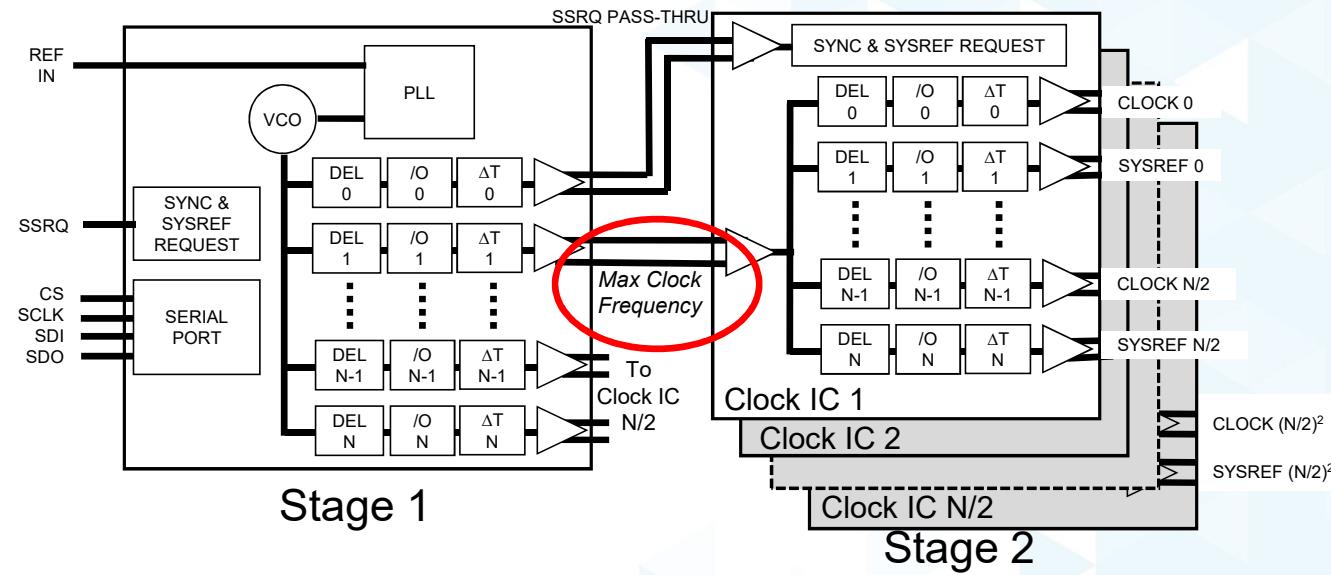
- Deterministically align clocks and minimize channel skews across all outputs and layers in a clocking tree
- Meet setup and hold times for SYSREF signals relative to the device clock at each data converter (TRX)

► Problems

- Large number of clocks required
- In multiple-device clock tree structures that are based on simple clock buffers, controlling setup and hold times is challenging
- Maintain deterministic phase accuracy across multiple levels of clock expansion
- Maintain clock jitter, phase noise performance across all tree layers and avoid extra clock spurs



Multichip Clock Distribution



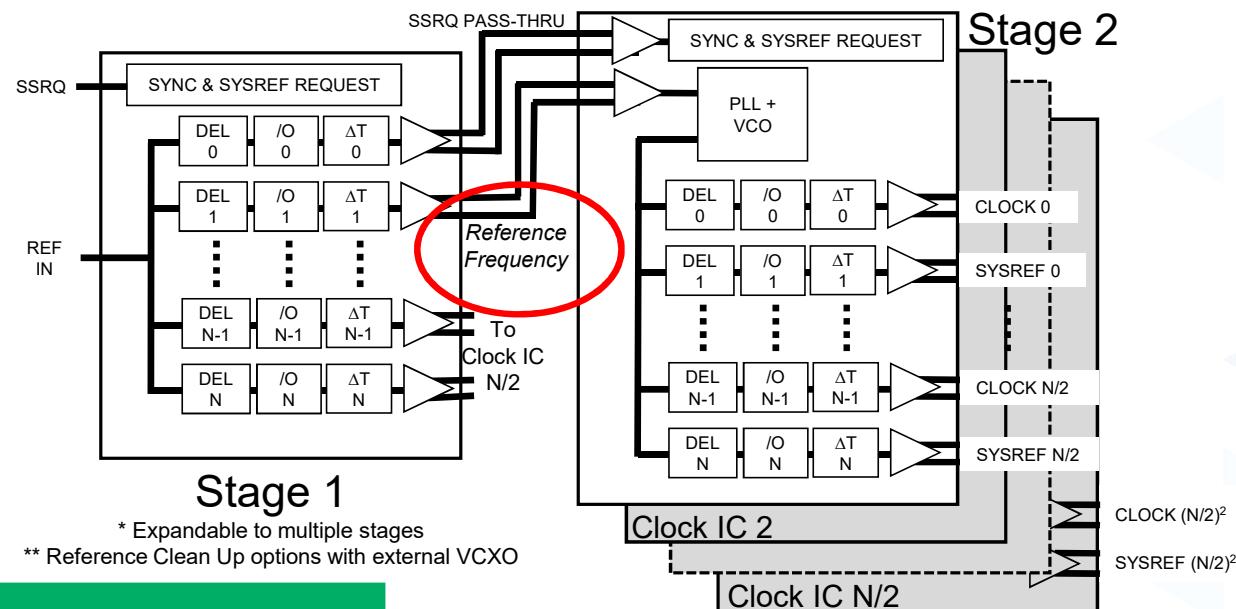
Advantages

Large Clock Trees

Simplifies Clock/SYSREF Sync & Alignment

Single VCO generates all clocks (cost)

Multichip Reference Distribution



Advantages

- Large Clock Trees w/ Ultralow Jitter Clocks
- Simplifies Clock/SYSREF Sync & Alignment
- Minimizes Traces Length of x GHz Clocks
- Multiple boards via backplane reference

Large Clock Trees: Clock vs Reference Distribution Comparison



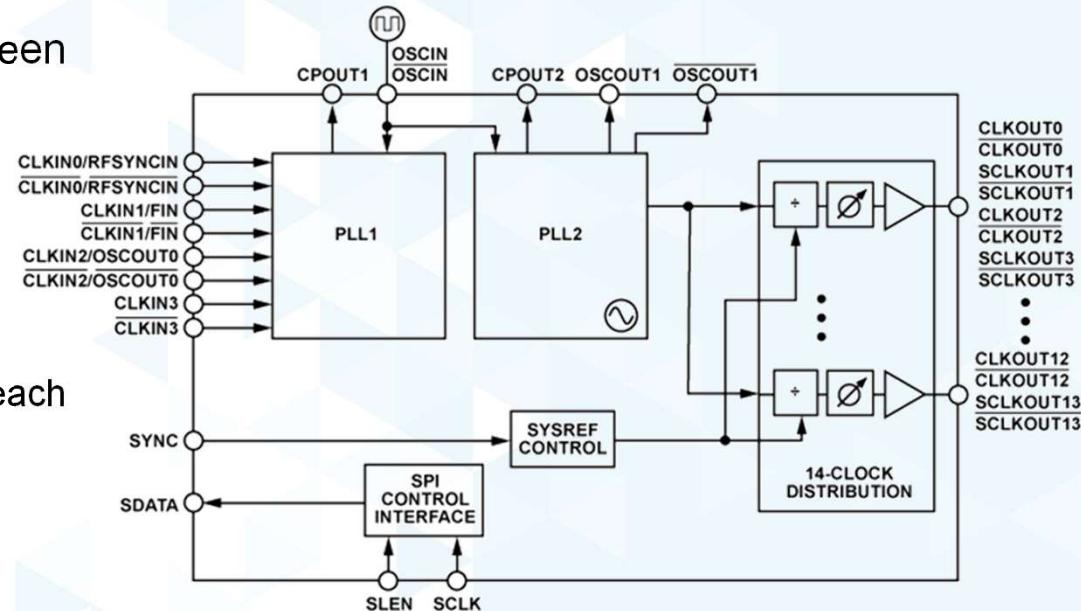
	Clock Distribution	Reference Distribution
Jitter	Low	Ultralow
Number of VCOs	1 (cost advantage)	1 per Clock Device
Correlated Close in Phase Noise (due to single PLL/VCO)	Yes ⁽¹⁾	No ⁽¹⁾
Timing Requirement: Multichip Output Synchronization	Easy	Easy to Moderate ⁽²⁾
Timing Requirement: SYSREF Generation	Easy to Moderate ⁽²⁾	Easy to Moderate ⁽²⁾
Inter-stage Frequency	Max Clock Speed (GHz) <small>RF routing concerns, may increase PCB cost sooner than Reference Distribution method</small>	Reference Frequency (MHz)
Risk of unwanted Signal Coupling onto Clock Signal (ADC SFDR)	Yes	Lower Risk <small>PLL/VCO loop filter at final stage will remove coupling affects on reference distribution</small>

(1) Application-dependent advantage

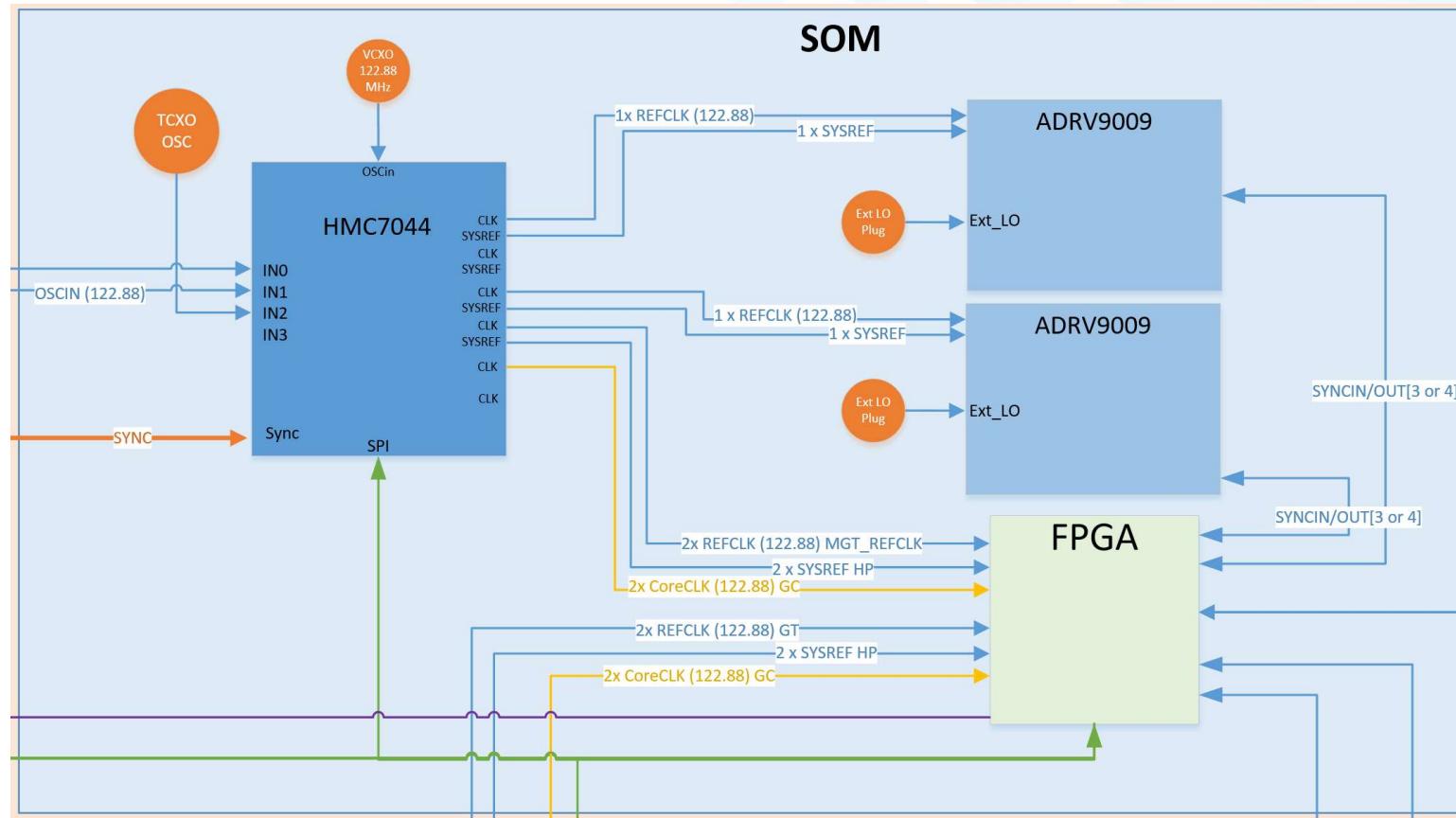
(2) Dependent on clock device family chosen. Newer clock device families have developed methods to ease these requirements

HMC7044

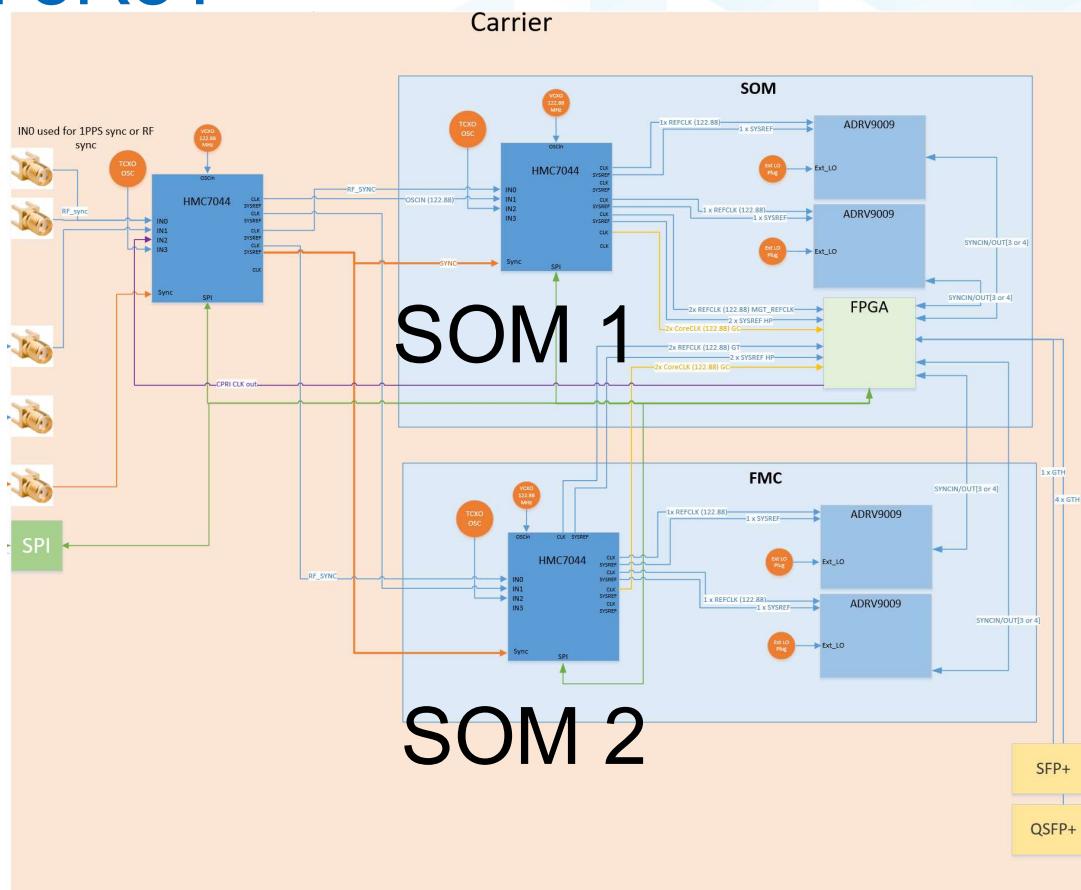
- ▶ SOM uses HMC7044 for clock/reference distribution for onboard ADRV9009s and between multiple SOMs
- ▶ JESD204B/JESD204C-compatible system reference (SYSREF) pulses
- ▶ 14 ultralow noise and configurable outputs
- ▶ Programmable phase delay:
 - 25 ps analog, and $\frac{1}{2}$ VCO cycle digital delay on each output
- ▶ Multiple HMC7044 can be synced
- ▶ Supports both Reference and Clock Distribution techniques
 - Multi-SOM can choose either or



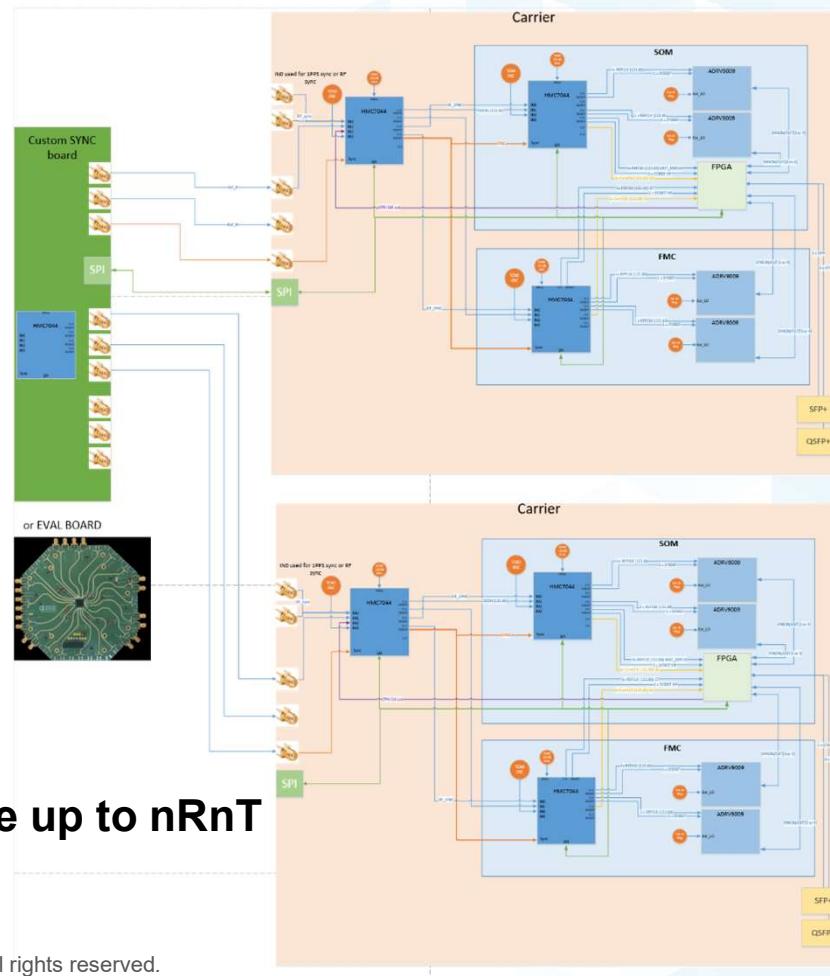
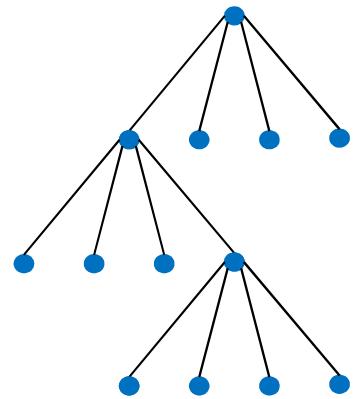
Multi-ADRV9009 Synchronization 4R4T



Multi-ADRV9009 Synchronization with Daughtercard 8R8T



Multi-SOM Sync 16R16T



SOM 1

SOM 2

SOM 3

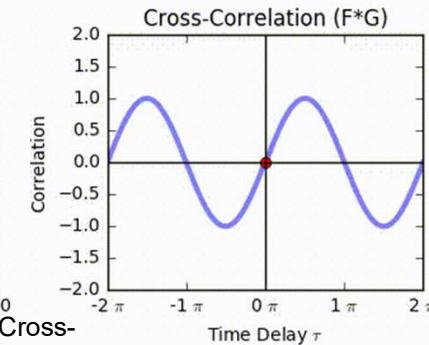
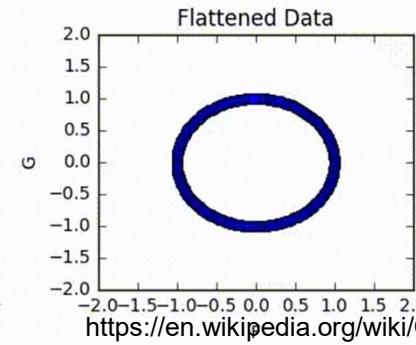
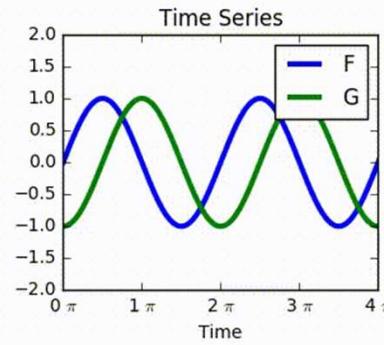
SOM 4

- Extending the clock tree
 - This concept can scale up to nRnT

Multichannel Phase Offset Validation

Measuring Phase

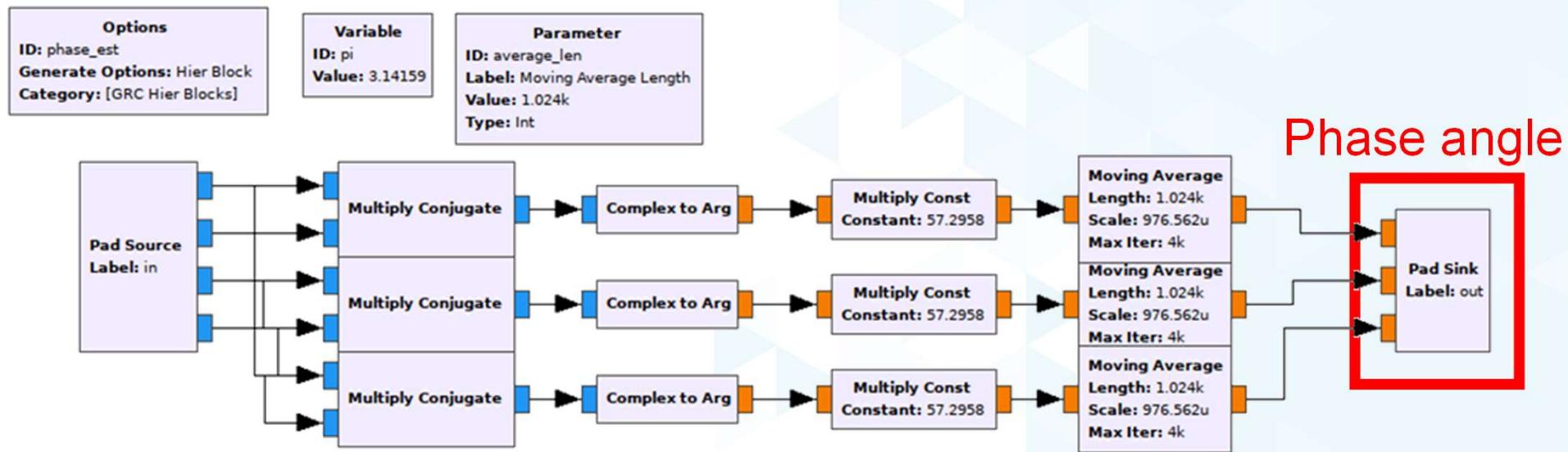
- ▶ Many ways to measure phase but two used here
- ▶ Average instantaneous phase
 - $f(\vec{x}, \vec{y}) = \tan^{-1}(\sum_{n=0}^{N-1} \bar{x}[n]y[n])$
- ▶ Cross-Correlation
 - $f(\vec{x}, \vec{y}) = \tan^{-1}(\max|\Im^{-1}[\overline{\Im(\vec{x})}\Im(\vec{y})]|)$
 - \Im is an FFT
 - Sample delay $\text{argmax}|\Im^{-1}[\overline{\Im(\vec{x})}\Im(\vec{y})]|$
 - Peak is reasonable confidence measurement



https://en.wikipedia.org/wiki/Cross-correlation#/media/File:Cross_correlation_animation.gif

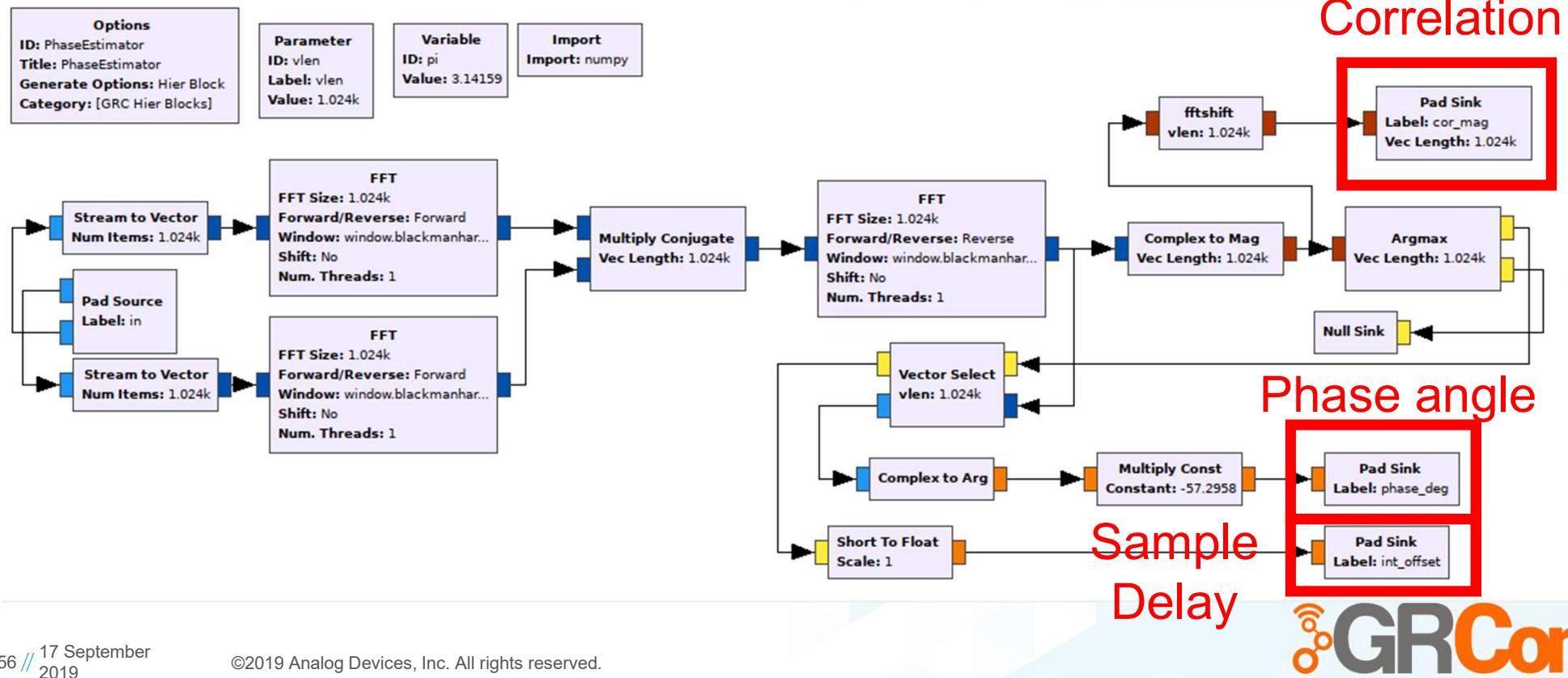
Averaged Instantaneous Phase Hier Block

- ▶ Fast, easy to implement, works great with sinusoids
- ▶ Sensitive to sample offset

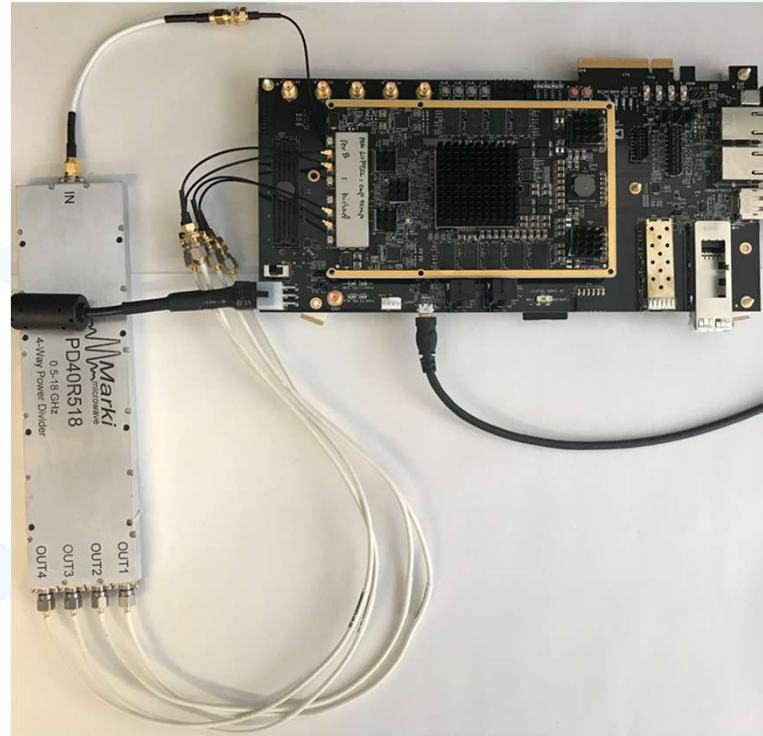
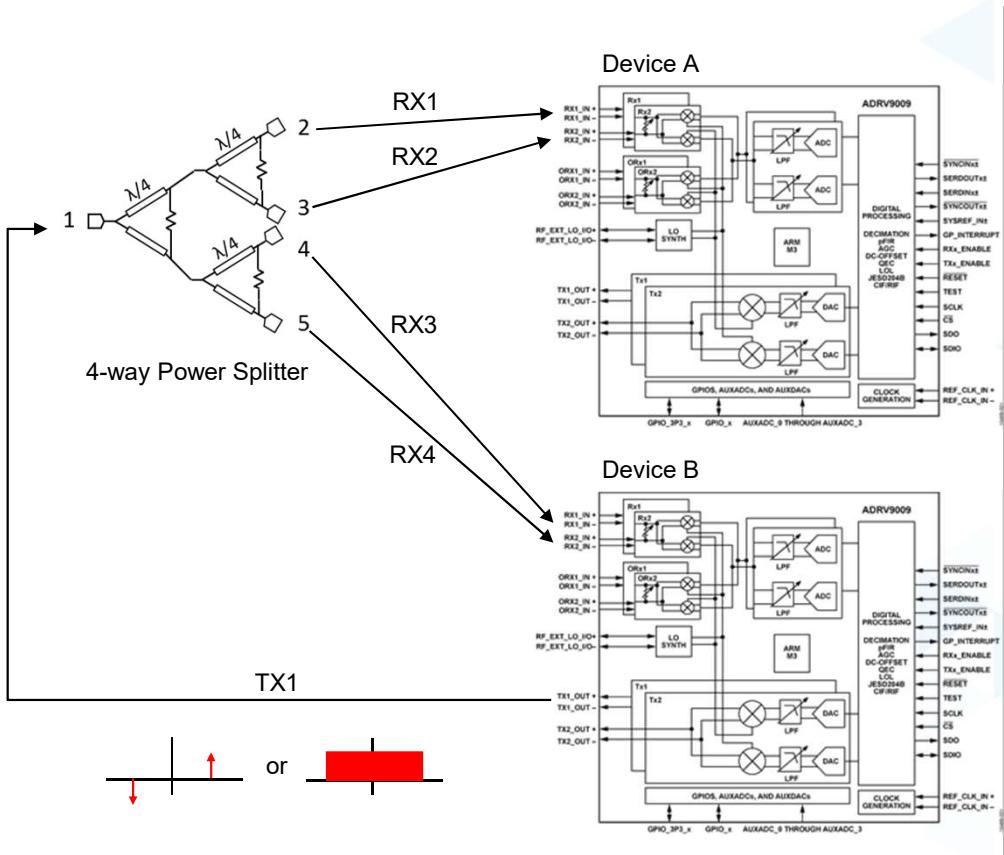


Cross-Correlation Method Hier Block

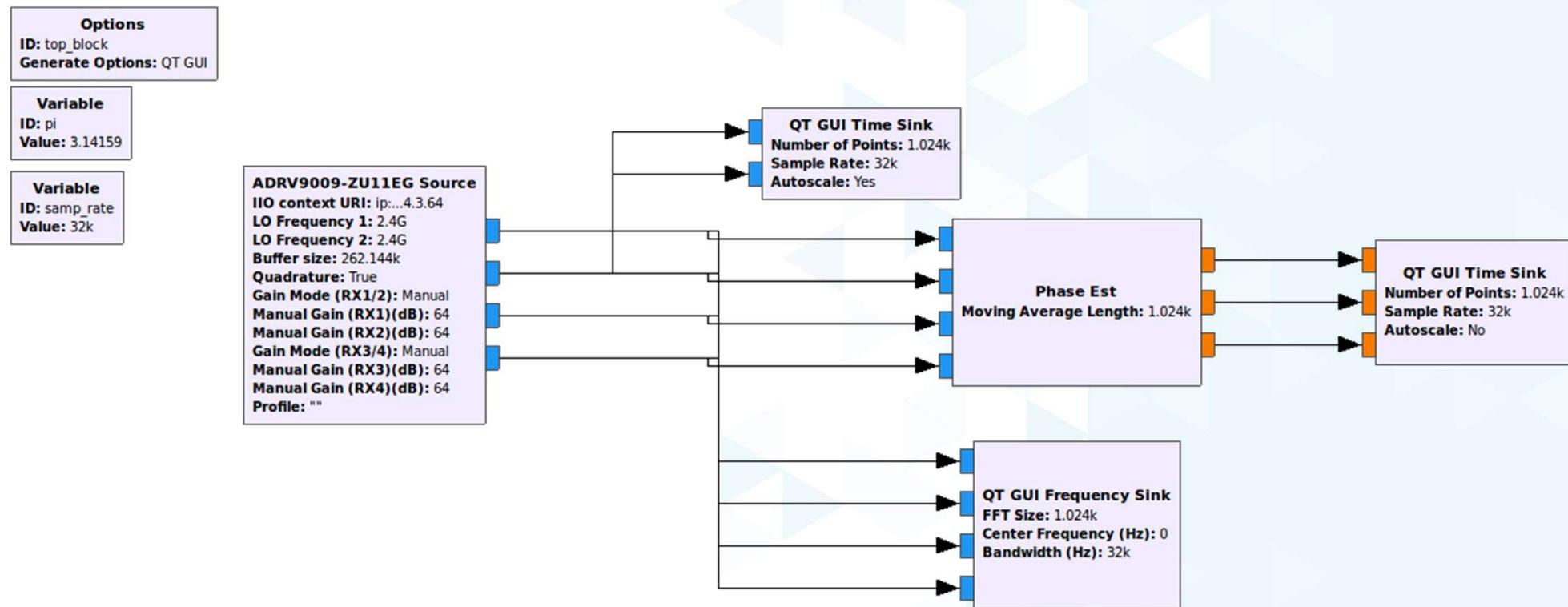
- ▶ Slow relative to direct method
- ▶ Sample offset measured separately and captured



Measurement Setup

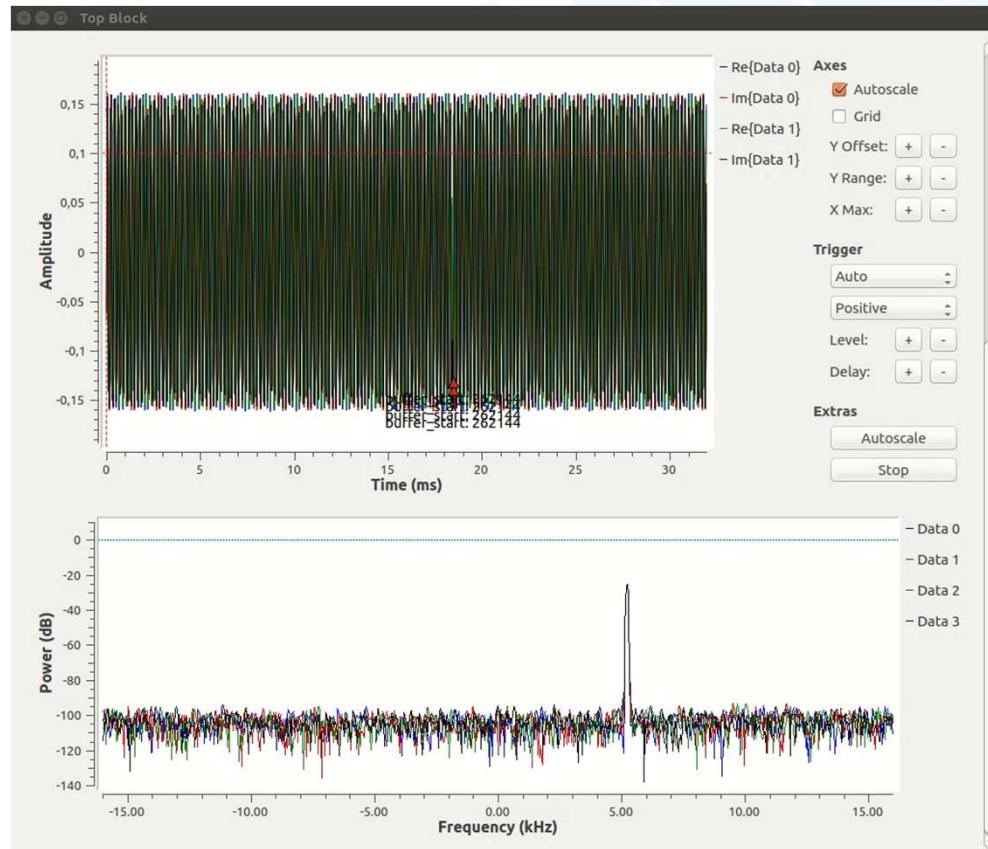


Flow Graph: Averaged Instantaneous Phase (sinewave_phase_est.grc)



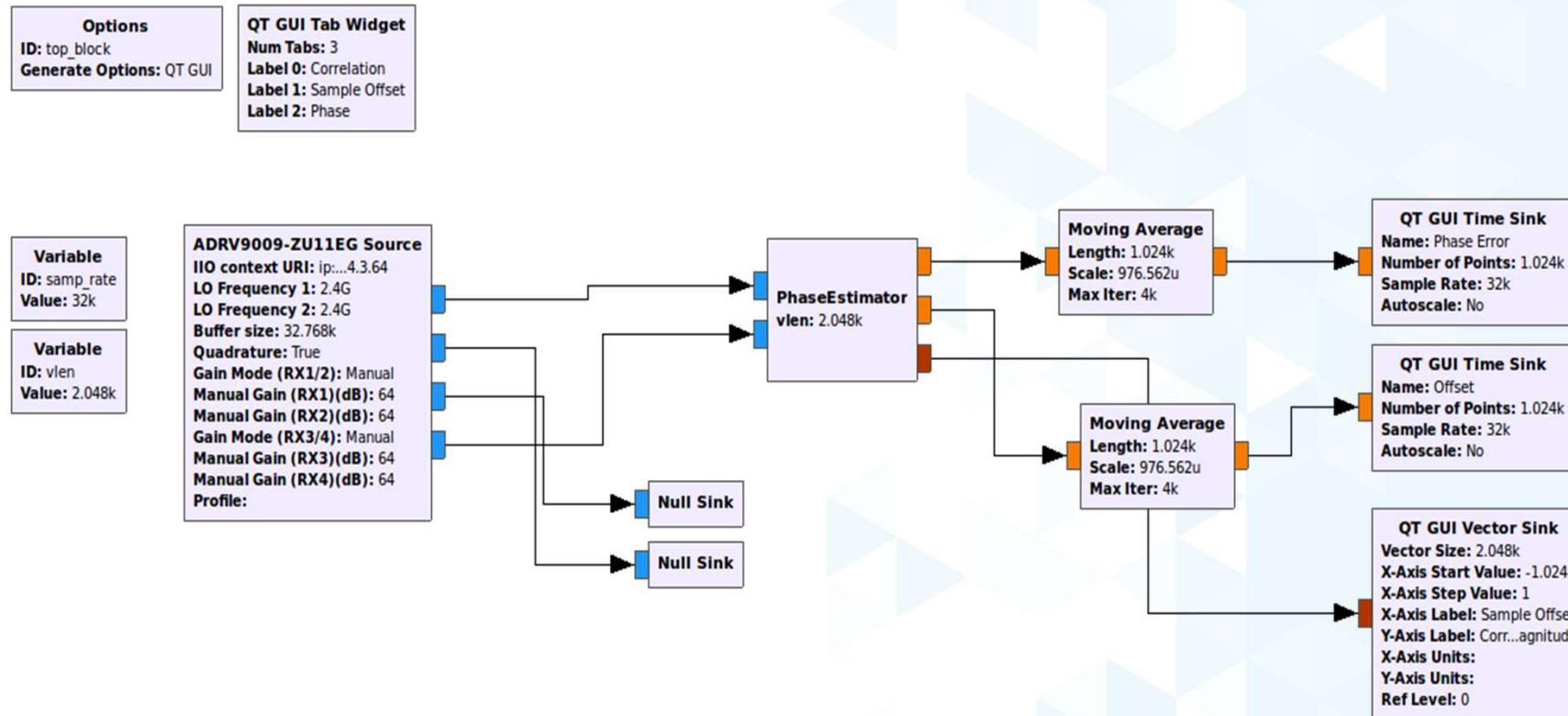
https://github.com/analogdevicesinc/gr-iio/blob/grcon2019/demos/adrv9009zu11eg/sinewave_phase_est.grc

Flow Graph: Averaged Instantaneous Phase



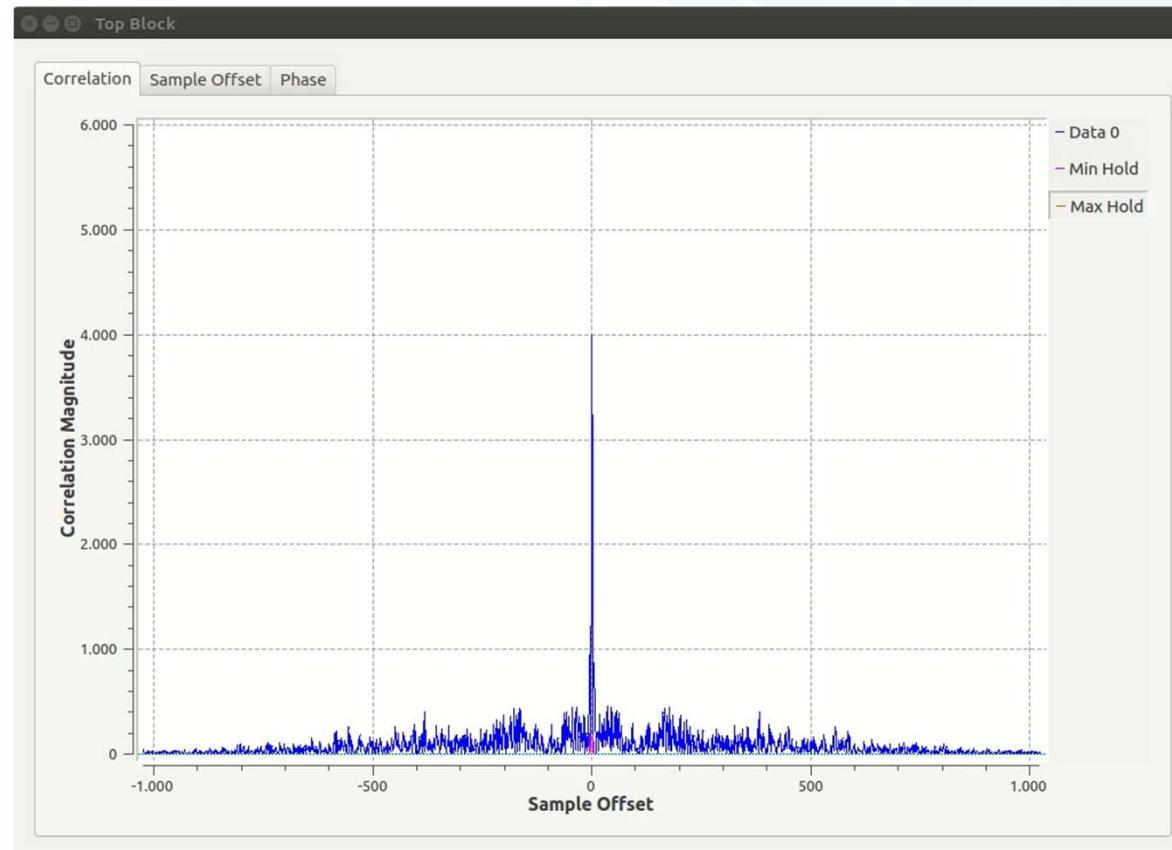
Flow Graph: Cross-Correlation Method

(noise_phase_est.grc)



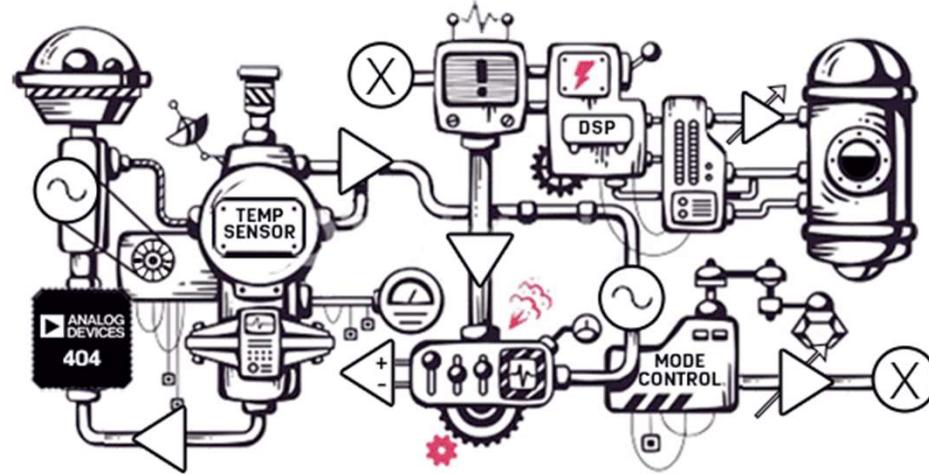
https://github.com/analogdevicesinc/gr-iio/blob/grcon2019/demos/adrv9009zu11eg/noise_phase_est.grc

Flow Graph: Cross-Correlation Method



Conclusions

- ▶ End-to-end deterministic latency and RF frequency and phase coherent synchronization in scalable Multichannel Systems can be realized
 - Using the latest generation of Integrated RF transceivers
 - Multichip LO Phase Synchronization simply phased array beamforming
 - RF Transceivers simplify Forced Spurious Decorrelation
 - Combined Rx Channels improve System Dynamic Range
 - Combined Tx Channels improve System Phase Noise
 - Flexible clocking and synchronization topology
 - Impedance controlled trace length matching
- ▶ Phase offsets can be **measured, avoided or compensated**
- ▶ GNU Radio is a very effective tool to build, model, analyze and visualize complex multichannel SDR systems



Ahhh, technology. We can't find that page.

Thanks Q & A

References



- [1] <https://wiki.analog.com/resources/eval/user-guides/adrv9009-zu11eg>
- [2] <https://www.analog.com/en/technical-articles/understanding-layers-in-jesd204b-specification.html>
- [3] <https://www.analog.com/en/analog-dialogue/articles/jesd204c-primer-part1.html>
- [4] <https://www.analog.com/en/technical-articles/synchronizing-sample-clocks-of-a-data-converter-array.html>
- [5] <https://www.analog.com/en/technical-articles/rf-transceivers-enable-forced-spurious-decorrelation-in-digital-beamforming-phased-arrays.html>
- [6] <https://www.analog.com/en/technical-articles/system-level-lo-phase-noise-model-for-phased-arrays-with-distributed-phase-locked-loops.html>