LAB 02
Combinational Circuit Design
19/02/2020
EEE-102
Section2
Haider Raheem

Design Methodology

Preliminary report formed the foundation of the design methodology. The Boolean equations helped to identify the gates to be used in creation of the Master Switch model. This Combinational Circuit implements the Master Switch model, it shows how in a home, a main switch controls other switches in main electric panel that controls electricity to the whole house. The design methodology consist of following steps:

1. Identified the logic gates to be used by Boolean equations. In this case two AND were used as the Boolean equations in preliminary report were, Msw.sw1 & Msw.sw2.
2. Identified 3 inputs (Msw, sw1, sw2) and 2 outputs (LED1, LED2)
3. Using the Vivado Design Suite wrote a VHDL code to describe the design of the Master switch.
4. Created a test bench file and with the help of Vivado tutorial document from Moodle wrote the VHDL code in order to run a simulation.
5. Checked the simulation and it worked well according to expectation.
6. Created a constraints file in order to assign the inputs to switches and outputs to LEDs. Msw assigned to sw3 of basys 3, sw1 to sw1 of the basys and sw2 to sw2 of Basys3. The output LED1 and LED2 were assigned to LD0 and LD1 of Basys 3 respectively.
7. Synthesized and Implemented VHDL design code in order to create a RTL schematic.
8. Generated Bitstream
9. Using hardware manager programmed the Basys 3 and it worked on Basys 3 too.
10. Design Complete!

Note : The VHDL Code is attached at end of the report

Truth Table:

Inputs			**Outputs**	
msw	Sw1	Sw2	**LED1**	**LED2**
0	0	0	**0**	**0**
0	0	1	**0**	**0**
0	1	0	**0**	**0**
0	1	1	**0**	**0**
1	0	0	**0**	**0**
1	0	1	**0**	**1**
1	1	0	**1**	**0**
1	1	1	**1**	**1**

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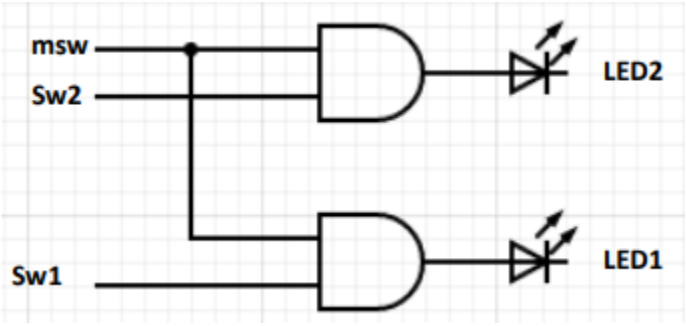
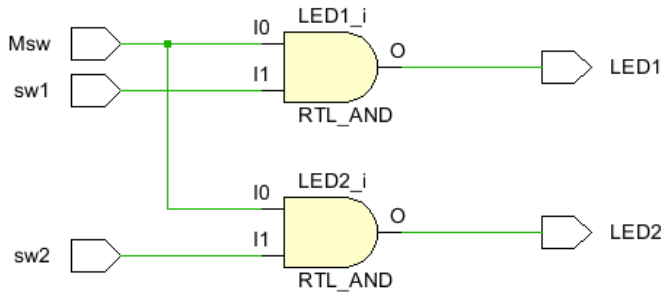


Schematics in preliminary report

Results:

The results satisfied the results of the truth table in preliminary report as planned. The results of the test bench and the RTL schematics are as following:



RTL Schematics

The RTL Schematics show the use of two AND gates and two LEDs. The Inputs to AND gate labelled LED1_i are Msw and sw1. The Inputs to AND gate labelled LED2_i are Msw and sw2. The Outputs are labelled as LED1 and LED2 just according to the design methodology.

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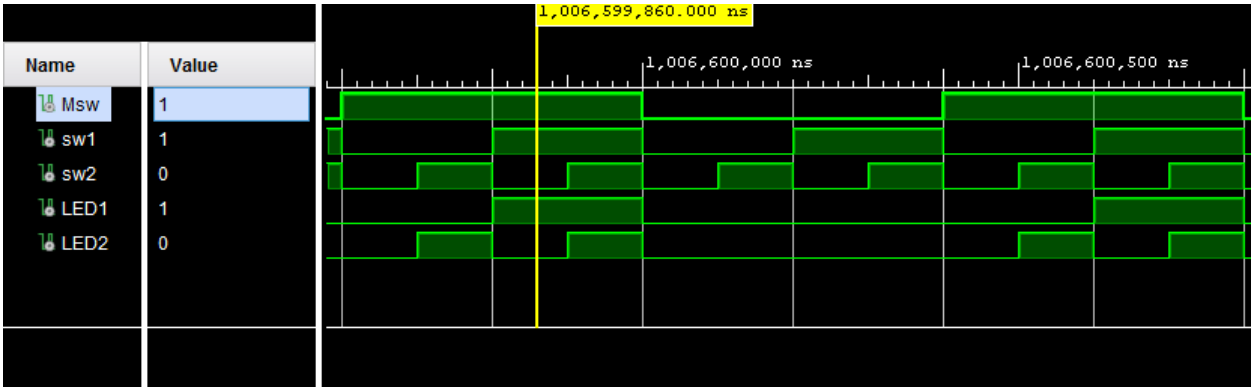
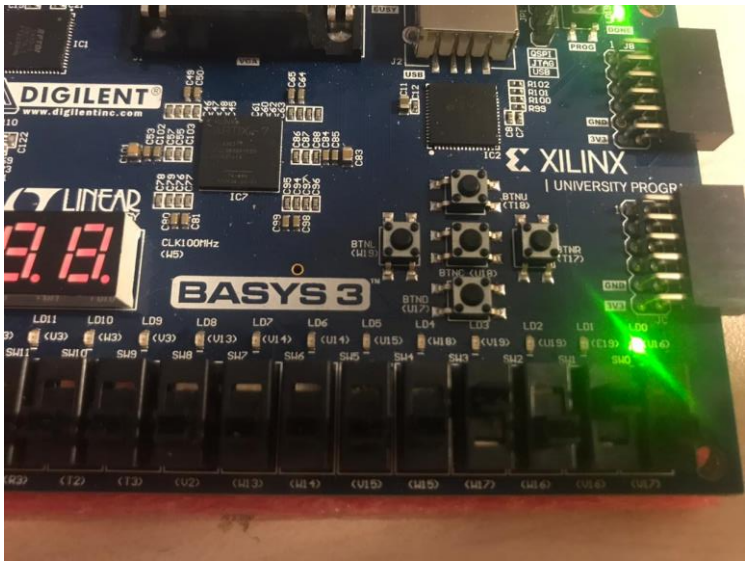


Test Bench Simulation results

The test bench results also justify the design methodology when the MSw is '0' the output is zero at LED1 and LED2. When MSw is '0', sw1 and sw2 are don't care there bits does not matter. When MSw and Sw1 have logic value 1, LED1 has logic value 1 and similar goes with sw2. When all inputs have logic value 1 then all outputs have logic value 1.

Basys 3 Board Implementation:



Msw = 1, sw1 = 1, sw=0

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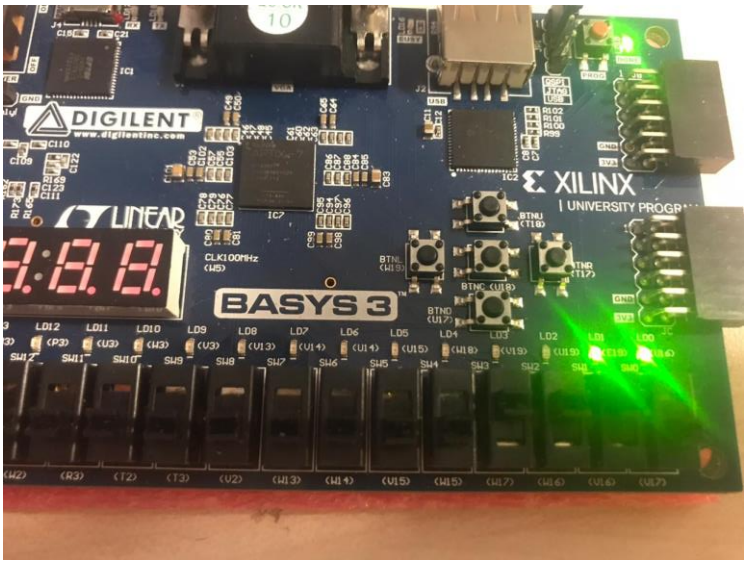
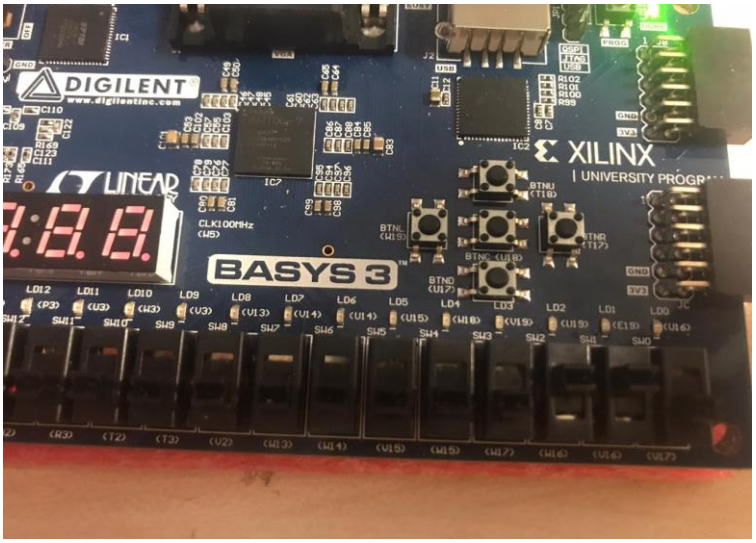


Msw = 1, sw1 = 1, sw=1



Msw = 0, sw1 = 1, sw=1

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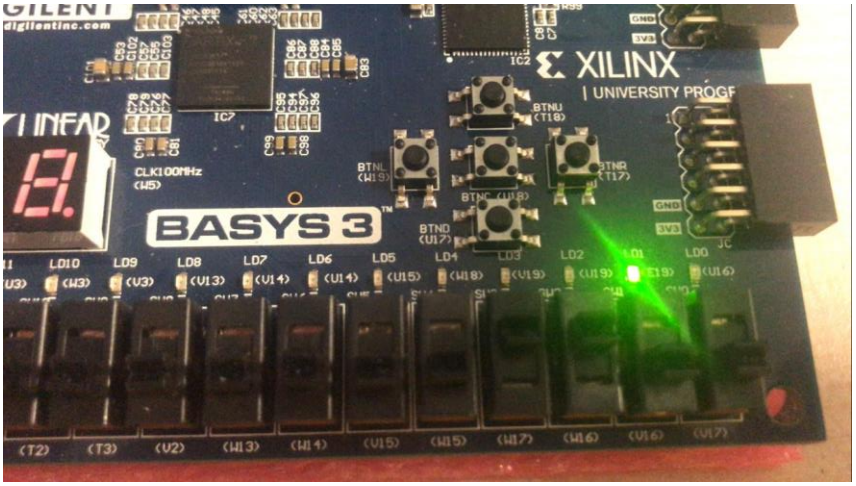

Msw = 1, sw1 = 0, sw=1

Conclusion:

This lab was a learning experience as it taught how to write a basic level VHDL code. The most interesting and difficult part was Test bench as its method was confusing. However, at the end this lab helped to learn the basics of VHDL, creating test bench simulations for digital design circuits and taught the basics of implementation of digital logic design on the Basys 3 board. At the end the combinational circuit in the preliminary report was implemented easily during the Lab.

The VHDL Code:

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use IEEE.std_logic_unsigned.all;
entity masterswitch is
Port (Msw: in std_logic;
sw1: in std_logic;
sw2: in std_logic;
LED1: out std_logic;
LED2: out std_logic );
end masterswitch;
architecture Behavioral of masterswitch is
begin
LED1 <= Msw And sw1;
LED2 <= Msw And sw2;
end Behavioral;
```

Test Bench Code:

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;
use IEEE.std_logic_unsigned.all;
entity tb_msw is
end tb_msw;
architecture Behavioral of tb_msw is
-- Component Declaration for the Unit Under Test (UUT)
 COMPONENT masterswitch
 Port (Msw: in std_logic;
sw1: in std_logic;
sw2: in std_logic;
LED1: out std_logic;
LED2: out std_logic );
 END COMPONENT;
--Inputs
signal Msw : std_logic := '0';
signal sw1 : std_logic := '0';
signal sw2 : std_logic := '0';
--Outputs
signal LED1 : std_logic;
signal LED2 : std_logic;
begin
-- Instantiate the Unit Under Test (UUT)
uut: masterswitch PORT MAP (
Msw => Msw,
sw1 => sw1,
sw2 => sw2,
LED1 => LED1,
LED2 => LED2
);
-- Stimulus process
stim_proc: process
begin
Msw<='0';sw1<='0';sw2<='0';
wait for 100ns;
Msw<='0';sw1<='0';sw2<='1';
wait for 100ns;
Msw<='0';sw1<='1';sw2<='0';
wait for 100ns;
Msw<='0';sw1<='1';sw2<='1';
wait for 100ns;
```

```
Msw<='1';sw1<='0';sw2<='0';
wait for 100ns;
Msw<='1';sw1<='0';sw2<='1';
wait for 100ns;
Msw<='1';sw1<='1';sw2<='0';
wait for 100ns;
Msw<='1';sw1<='1';sw2<='1';
wait for 100ns;
end process;
END;
```

Constraints:

For Inputs:

```
set_property PACKAGE_PIN V16 [get_ports {sw1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw1}]
set_property PACKAGE_PIN W16 [get_ports {sw2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw2}]
set_property PACKAGE_PIN W17 [get_ports {Msw}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Msw}]
```

For Outputs:

```
set_property PACKAGE_PIN U16 [get_ports {LED1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {LED1}]
set_property PACKAGE_PIN E19 [get_ports {LED2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {LED2}]
```