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**Absolute maximum ratings**

Operation beyond the specified absolute maximum ranges can result in permanent damage or degradation of the voltage detector.

Symbol	Description	Min	Max	Unit
$V_{IN}$	Input voltage	-0.5	20	V
$V_{DD}$	Load voltage supply-rail	0	5.5	V
$V_{PGOUT}$	Power-gated output voltage	0	5.5	V
$V_{OD}$	Open-drain output voltage of UB20M	0	5.5	V
$V_{\overline{OD}}$	Active-high open-drain output voltage	0	25	V
$I_{PGO}$	PGO load current	-	120	mA
$I_{OD}$	OD output current	-	5.6	mA
$I_{\overline{OD}}$	$\overline{OD}$ output current	-	220	mA
$T_{amb}$	Ambient temperature	-40	85	°C

For more information, please refer to the UB20M datasheet and the corresponding datasheets of Q1 and Q2.

**Output configuration**

One of three different output configurations can be selected. This is achieved through the zero-ohm links R2, R3, and R4. In all configurations the output of the voltage detector is pulled up to  $V_{DD}$  by R1. Using larger pull-up resistor minimises the leakage current during ON state. However, it will also increase the time to trigger the circuit connected to OD.

*Open-drain output*

Supply terminal	<b>VDD</b>
Output terminal	<b>OD</b>
Closed links	-
Open links	<b>R2, R3, R4</b>

The open-drain output of UB20M is directly connected to the OD terminal. If this option is preferred links R2, R3, and R4 should be removed to disconnect Q1 and Q2 and minimise the total leakage of the circuit. When  $V_{IN}$  is lower and the threshold of UB20M the OD output is pulled-up by R1 to  $V_{DD}$ . When  $V_{IN}$  becomes higher than the threshold the OD output is pulled down.

The voltage at the OD output must always be lower than the specified maximum of 5.5 V. If your application requires higher  $V_{DD}$  a pull-down resistor can be connected between the OD terminal and GND. Along with R1 this resistor will form a potential divider and limit the OD voltage. Considering the recommended maximum of 5V for  $V_{OD}$ , the value of the pull-down resistor can be calculated as:

$$R_{PD} = \frac{V_{ODmax}}{V_{DD} - V_{ODmax}} R_1 = \frac{5}{V_{DD} - 5} R_1.$$

*Active-high open-drain output*

Supply terminal	<b>VDD</b>
Output terminal	<b><math>\overline{\text{OD}}</math></b>
Closed links	<b>R4</b>
Open links	<b>R2, R3</b>

Some applications require an active-high signal when the voltage detector is triggered. In this case link R4 is closed, while R2 and R3 are open. When VIN is lower than the threshold the gate of Q1 is pulled up by R1 and the  $\overline{\text{OD}}$  open-drain output is low. When VIN becomes higher than the threshold, Q1 is turned-off. This configuration requires an external pull-up.

*Power-gated output*

Supply terminal	<b>VDD</b>
Output terminal	<b>PGO</b>
Closed links	<b>R2, R3</b>
Open links	<b>R4</b>

The power-gated output PGO allows the VD to switch the power supply rail of loads operating at voltages up to 5V. In this case the external power supply is connected to VDD and the load is connected to PGO. The high-side switch Q2 is controlled by UB20M. The turn-off time is determined by R1 and the input capacitance of Q2.

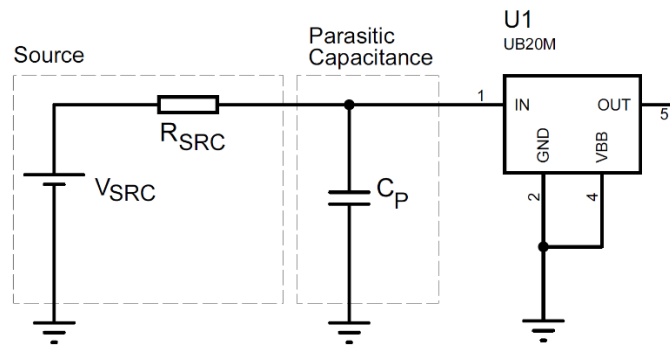
**IMPORTANT:****Voltage Measurements**

When voltage measurements are performed, the probe impedance should be considered. For example, a voltage probe connected to the OD terminal will form a potential divider with R1, and the OD line will not be pulled-up to V<sub>DD</sub> when the voltage detector is off. This could result in Q1 being always on.

**High-impedance sources and parasitic capacitance**

Source capacitance, PCB terminals and tracks, and device pins all contribute to the total parasitic capacitance that is present at the input of the voltage detector. This parasitic capacitance needs to be charged as the source voltage rises. For high source impedances, the parasitic capacitance will therefore influence turn-on time.

As the equivalent open-circuit source voltage of the source V<sub>SRC</sub> (Figure 3) drops, the parasitic capacitance C<sub>P</sub> needs to be discharged through the source resistance R<sub>SRC</sub> with an insignificant contribution flowing into the input of the voltage detector. The source resistance and parasitic capacitance therefore determine discharge time and consequently turn-off delay. This delay can be reduced by adding a leakage path to ground, e.g. with a reverse biased diode in parallel to C<sub>P</sub>.



**Figure 3 High impedance source and parasitic capacitance**

### Power-line interference

In environments with AC power lines nearby, care must be taken when using long input wires between the VIN terminal and the source or when touching the UB20M input pin. Capacitive or inductive coupling with the AC power lines or cross-talk from communication lines could cause an AC voltage to be induced at the input terminal and activate the detector.

### Reducing power-line interference

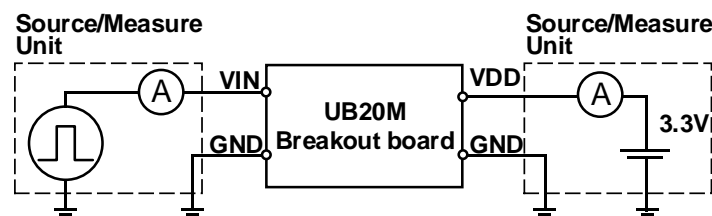
- Input lines should be kept short; place the voltage detector within mm of the sensor.
- Use a ground plane when using the discrete UB20M. If using the evaluation board, use a ground plane under the whole set-up, including under any breadboards used.
- Where longer leads from the sensor are required, twist the wires, and use a conductive sheath that is grounded at the voltage detector end. It is better to place the UB20M and any power-gating switches at the sensor, and bring the switched output via leads to a main electronics board.

### PCB leakage

Moisture and contamination on the surface of the breakout board cause leakage between tracks, which, in turn, increases the required input current. This leakage is typically 10s of pA, but can increase to 100s of pA, depending on air humidity, and the state of the surface of the board.

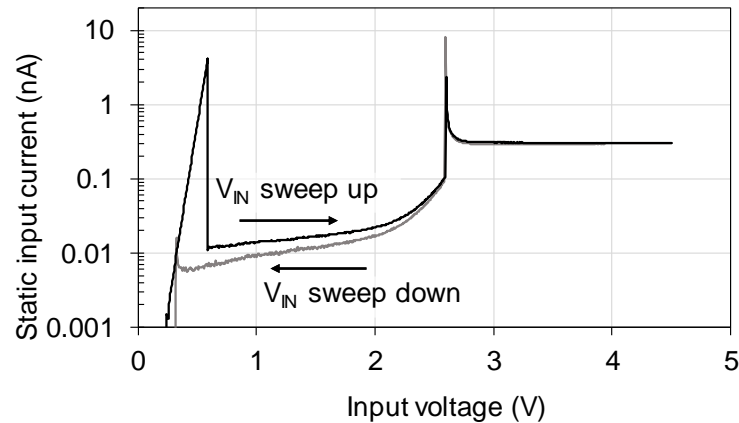
This variability is a result of the board having exposed pads and additional components, to provide flexibility during prototyping. In addition, there is a leakage current associated with the FR4 substrate.

To determine the board leakage currents, the measurement set-up of Figure 4 can be used.

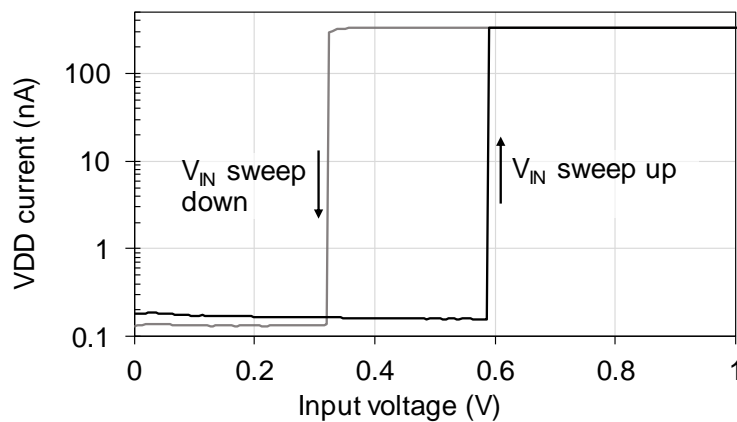


**Figure 4 UB20M breakout board input and output current measurement set up**

Figure 5 shows input current and board-leakage versus input voltage, although it must be noted that this is a relatively clean board in dry conditions. This graph is derived using the set-up of Figure 4, with a Keysight B2902A Source/Measure Unit carrying out both the input and output current measurements. The output voltage is kept constant at 3.3V and the input voltage is swept from 0V to 5V in 5 mV steps, and the steady state current input and output current are measured.



**Figure 5a UB20M breakout board input currents**



**Figure 5b UB20M breakout board leakage current**

These graphs show that the breakout board increases the effective input quiescent current at 1V to 17pA on a rising input voltage. When the voltage is decreasing, this current is below 10pA. The peak input current of the board at the detection threshold is 4nA, whereas the UB20M's steady-state input current peaks at about 1.6nA.

The output leakage current, when the UB20M is not active, is below 200pA.

These measurements were performed at 23 °C ambient temperature.

### Reducing board leakage current

In order to minimise the input and output leakage currents, the following measures can be taken:

- Remove unnecessary components from the PCB.
- Clean the PCB (e.g. with Ambresil PCB Cleaner) and apply protective coating (e.g. Electrolube HPA Conformal Coating).
- Use the UB20M voltage detector discrete device on a specially designed low-leakage PCB.

## Supporting material

Voltage detector and breakout board datasheets, technical support and sample requests:

[www.sensor-driven.com](http://www.sensor-driven.com)

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*The UB20M device is currently a pre-production prototype.*

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