M_(TT)CAN

Controller Area Network

Functional Changes

R3.0.1 to R3.1.0

05.06.2014

Robert Bosch GmbH
Automotive Electronics

LEGAL NOTICE

INCLUDING, BUT NOT LIMITED TO, CLAIMS, SUITS OR CAUSES OF ACTION INVOLVING ALLEGED INFRINGEMENT OF COPYRIGHTS, PATENTS, TRADEMARKS, TRADE SECRETS, OR UNFAIR COMPETITION.

INDEMNIFICATION: TO THE MAXIMUM EXTEND PERMITTED BY LAW YOU AGREE TO INDEMNIFY AND HOLD HARMLESS THE INTELLECTUAL PROPERTY OWNERS, COPYRIGHT HOLDERS AND CONTRIBUTORS, AND EMPLOYEES, AND ANY PERSON FROM AND AGAINST ALL CLAIMS, LIABILITIES, LOSSES, CAUSES OF ACTION, DAMAGES, JUDGMENTS, AND EXPENSES, INCLUDING THE REASONABLE COST OF ATTORNEYS' FEES AND COURT COSTS, FOR INJURIES OR DAMAGES TO THE PERSON OR PROPERTY OF THIRD PARTIES, INCLUDING, WITHOUT LIMITATIONS, CONSEQUENTIAL, DIRECT AND INDIRECT DAMAGES AND ANY ECONOMIC LOSSES, THAT ARISE OUT OF OR IN CONNECTION WITH YOUR USE, MODIFICATION, OR DISTRIBUTION OF THIS SPECIFICATION, SOFTWARE RELATED THERETO, CODE AND/ OR PROGRAM RELATED THERETO, ITS OUTPUT, OR ANY ACCOMPANYING DOCUMENTATION.

GOVERNING LAW: THE RELATIONSHIP BETWEEN YOU AND ROBERT BOSCH GMBH SHALL BE GOVERNED SOLELY BY THE LAWS OF THE FEDERAL REPUBLIC OF GERMANY. THE STIPULATIONS OF INTERNATIONAL CONVENTIONS REGARDING THE INTERNATIONAL SALE OF GOODS SHALL NOT BE APPLICABLE. THE EXCLUSIVE LEGAL VENUE SHALL BE DUESSELDORF, GERMANY.

MANDATORY LAW SHALL BE UNAFFECTED BY THE FOREGOING PARAGRAPHS.

INTELLECTUAL PROPERTY OWNERS/COPYRIGHT OWNERS/CONTRIBUTORS: ROBERT BOSCH GMBH, ROBERT BOSCH PLATZ 1, 70839 GERLINGEN, GERMANY AND ITS LICENSORS.

REFERENCES

This document refers to the following documents:

Ref	Author(s)	Title
[1]	AE/EIN	M_CAN User's Manual
[2]	AE/EIN	M_TTCAN User's Manual

Table of Contents

Purpose

This document describes the changes between M_CAN / M_TTCAN R3.0.1 and R3.1.0 from a software developer's point of view.

The functional changes listed below were introduced to keep the M_CAN / M_TTCAN aligned with the ongoing standardization activities for ISO11898-1 (marked as **iso**). In addition some functions of the M_CAN / M_TTCAN were optimized (marked as **opt**). A detailed description can be found in the M_CAN / M_TTCAN User's Manual. These changes have to be considered when migrating software from M_CAN / M_TTCAN R3.0.1 to R3.1.0 implementations.

1. Register FBTP renamed to DBTP and restructured

R3.0.1 software which configures **TDCO** has to be updated. The bit fields for configuration of **DTSEG1**, **DTSEG2**, and **DSJW** start at the same bit position as with R3.0.1. The expanded ranges should have no impact on R3.0.1 software.

1.1 Transmitter delay compensation offset moved to new register (opt)

TDCO moved to new Transmitter Delay Compensation Register **TDCR.TDCO** (see section 6).

1.2 Increased configuration range for data bit timing (iso)

FTSEG1 renamed to **DTSEG1** and range expanded from 1...15 (4 bit) to 0...31 (5 bit).

FTSEG2 renamed to **DTSEG2** and range expanded from 0...7 (3 bit) to 0...15 (4 bit).

FSJW renamed to **DSJW** and range expanded from 0...3 (2 bit) to 0...15 (4 bit).

2. Register TEST restructured

R3.0.1 software which evaluates **TDCV** has to be updated.

2.1 Transmitter delay compensation value moved to new register (opt)

TDCV moved to Protocol Status Register **PSR.TDCV** (see section 5).

3. Register CCCR restructured

The function of bits 13...8 was changed to fulfil ISO requirements and to optimize handling of mode changes between Classic CAN, CAN FD, and CAN FD with bit rate switching operation. Software written for R3.0.1 has to be updated accordingly.

With the changes listed below switching between CAN operation modes for frame transmission is simplified. Now it is possible to switch between transmission of Classic CAN, CAN FD, and CAN FD with bit rate switching for each Tx Buffer by configuration of Tx Buffer element bits **FDF** and **BRS** (see section 11). With the new CAN operation mode handling, status flags **FDBS** and **FDO** are no more needed.

Those parts of R3.0.1 software dealing with message transmission have to be updated. Frame reception is not affected.

3.1 Control bit EFBI to enable edge filtering during bus integration added (iso)

Edge filtering during bus integration is disabled after reset. Bit **EFBI** replaces R3.0.1 bit **FDBS** which is no more required.

3.2 Control bit PXHD to disable Protocol Exception Event Handling added (iso)

Protocol Exception Event handling is enabled after reset. Bit **PXHD** replaces R3.0.1 bit **FDO** which is no more required.

3.3 CMR removed (opt)

The transmit mode is now individually configured for each Tx Buffer via bits **FDF** and **BRS** of the Tx Buffer elements (see section 11).

3.4 CME replaced by BRSE and FDOE (opt)

When **BRSE** = 0 and **FDOE** = 0, received frames are strictly interpreted as Classic CAN frames, which leads to the transmission of an error frame when receiving a CAN FD frame. In case **BRSE** = 0 and **FDOE** = 1, transmission of CAN FD frames without bit rate switching and reception of all CAN FD frames is enabled. With **BRSE** = 1 and **FDOE** = 1, transmission and reception of all CAN FD frames is enabled. Figure 1 below shows the mapping of **CME** (R3.0.1) to the new bits **BRSE** and **FDOE** (R3.1.0).

CME	BRSE	FDOE
0 0	0	0
0 1	0	1
1 0	1	1
1 1	1	1

Figure 1: Mapping **CME** to **BRSE**, **FDOE**

4. Register BTP renamed to NBTP and restructured

Register completely restructured, R3.0.1 software has to be updated.

4.1 Reduced configuration range for baud rate prescaler (opt)

BRP renamed to **NBRP** and range reduced from 0...1023 (10 bit) to 0...511 (9 bit).

4.2 Increased configuration range for nominal bit timing (iso)

TSEG1 renamed to **NTSEG1** and range expanded from 1...63 (6 bit) to 1...255 (8 bit).

TSEG2 renamed to **NTSEG2** and range expanded from 0...15 (4 bit) to 0...127 (7 bit).

SJW renamed to **NSJW** and range expanded from 0...15 (4 bit) to 0...127 (7 bit).

5. Register PSR updated

R3.0.1 software which evaluates PSR has to be updated.

5.1 Transmitter delay compensation value moved from register TEST (opt, iso)

TDCV has been moved from TEST register to **PSR.TDCV**. Range expanded from 0...63 mtq (6 bit) to 0...127 mtq (7 bit).

5.2 Flag PXE for signalling of Protocol Exception Event added (iso)

The status flag **PXE** was added to signal a Protocol Exception Event.

5.3 REDL renamed (opt)

Received a CAN FD Message flag **REDL** renamed to **RFDF**.

5.4 FLEC renamed (opt)

Fast Last Error Code **FLEC** renamed to Data Phase Last Error Code **DLEC**.

6. Register TDCR added

R3.0.1 software which configures **TDCO** has to be updated.

6.1 Transmitter delay compensation offset moved from register DBTP (opt, iso)

TDCO has been moved from register DBTP to **TDCR.TDCO**. Range expanded from 0...31 mtq (5 bit) to 0...127 mtq (7 bit).

6.2 Configuration for transmitter delay compensation filter window length (iso)

The configuration parameter **TDCF** defines the minimum value for the SSP position. Dominant edges on **m_(tt)can_rx** that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when **TDCF** is configured to a value greater than **TDCO**. Valid values are 0...127 mtq.

7. Register IR updated

R3.0.1 software which evaluates interrupt flags **STE**, **FOE**, **ACKE**, **BE**, **CRCE** has to be updated.

7.1 Interrupt flags STE, FOE, ACKE, BE, CRCE repl. by ARA, PED, PEA (opt)

Interrupt flag **ARA** added to signal a Host access to a reserved register address in the M_CAN / M_TTCAN register map.

Interrupt flag **PED** added to signal a protocol error in the data phase. The flag is set when **PSR.DLEC** is updated to other values than 0b000 or 0b111.

Interrupt flag **PEA** added to signal a protocol error in the arbitration phase. The flag is set when **PSR.LEC** is updated to other values than 0b000 or 0b111.

8. Register IE updated

R3.0.1 software which configures interrupt enable bits **STEE**, **FOEE**, **ACKEE**, **BEE**, **CRCEE** has to be updated.

8.1 Interrupt enable bits STEE, FOEE, ACKEE, BEE, CRCEE repl. by ARAE, PEDE, PEAE (opt)

Changed to keep IE register aligned with updated IR register.

9. Register ILS updated

R3.0.1 software which configures interrupt line select bits **STEL**, **FOEL**, **ACKEL**, **BEL**, **CRCEL** has to be updated.

9.1 Interrupt line select bits STEL, FOEL, ACKEL, BEL, CRCEL repl. by ARAL, PEDL, PEAL (opt)

Changed to keep ILS register aligned with updated IR register.

10. Rx Buffer and FIFO Element updated

No impact on R3.0.1 software.

10.1 Bit EDL renamed to FDF (iso).

Naming updated to comply with ISO11898-1 WD.

11. Tx Buffer Element updated

R3.0.1 software has to be updated with respect to handling of transmit messages. The configuration of Tx Buffer elements and enabling of CAN operation modes has been changed for M_CAN / M_TTCAN R3.1.

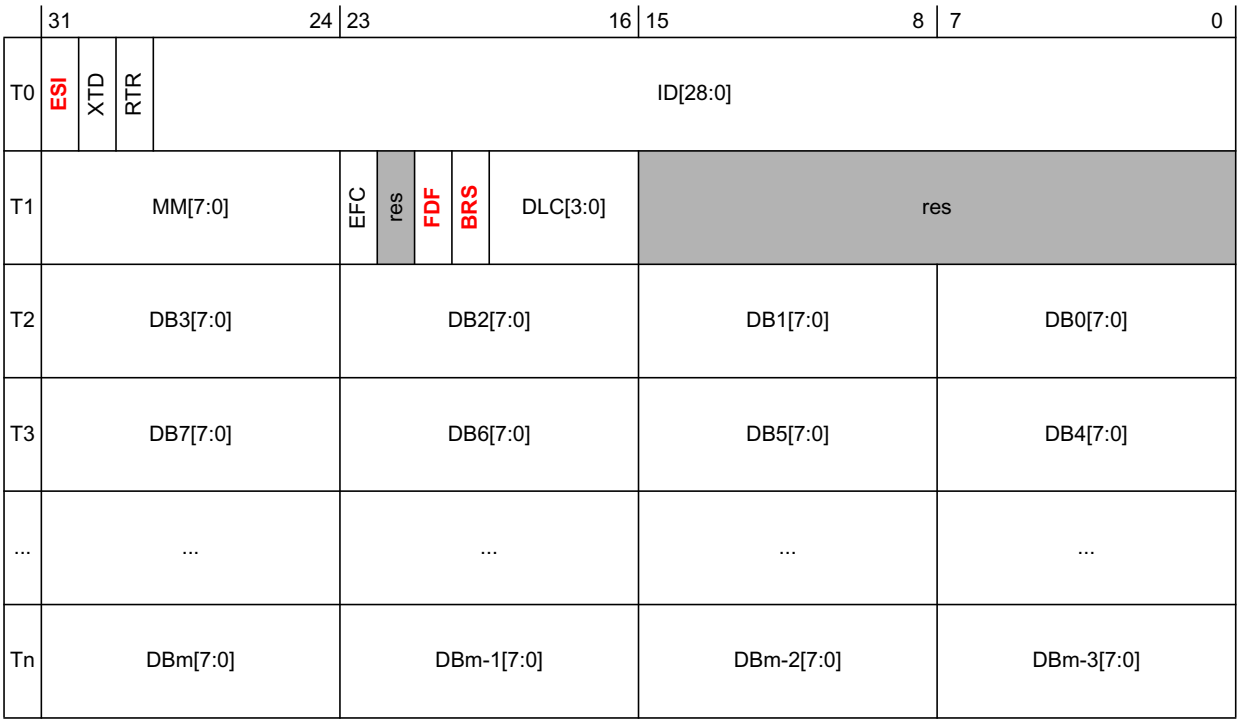

Figure 2: Tx Buffer Element

11.1 Transmission of bit ESI recessive configurable (iso)

Configuration bit **ESI** added. The **ESI** bit of the Tx Buffer element is or'ed with the error passive flag to decide the value of the **ESI** bit in the transmitted frame. As required by the CAN FD protocol specification, an error active node may optionally transmit the **ESI** bit recessive, but an error passive node will always transmit the **ESI** bit recessive. This feature can be used in gateway applications when a message from an error passive node is routed to another CAN network.

11.2 Selection of Classic/FD format transmission per Tx Buffer element (opt)

Configuration bits **FDF** and **BRS** added. Now the transmit mode can be configured individually for each Tx Buffer element. Bit **FDF** of a Tx Buffer element decides whether the frame is transmitted in FD format. In addition bit **BSR** configures transmission with bit rate switching.

The Tx Buffer element bits **FDF** and **BRS** replace the global CAN operation mode control **CCCR.CMR** of R3.0.1.

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x18	res															
	R-0x0															

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	res	TXP	EFBI	PXHD	res		BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
	R-0	RP-0	RP-0	RP-0	R-0x0		RP-0	RP-0	Rp-0	RP-0	Rp-0	RW-0	R-0	Rp-0	RP-0	RW-1

Figure 3: CC Control Register

Transmission of FD frames has to be enabled by configuration bits **CCCR.FDOE** and **CCCR.BRSE**. Figure 4 lists the possible configurations for frame transmission.

CCCR		Tx Buffer Element		Frame Transmission
BRSE	**FDOE**	**FDF**	**BRS**	
ignored	0	ignored	ignored	Classic CAN
0	1	0	ignored	Classic CAN
0	1	1	ignored	FD without bit rate switching
1	1	0	ignored	Classic CAN
1	1	1	0	FD without bit rate switching
1	1	1	1	FD with bit rate switching

Figure 4: Possible Configurations for Frame Transmission

An application of this new feature would be to transmit wakeup messages for CAN Partial Networking in Classic CAN format while all other frames are transmitted in FD format.

12. Overview on modified / added Registers

REL	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FBTP -> DBTP (0x00C)

3.0.1				TDCO					TDC			FBRP									FTSEG1					FTSEG2					FSJW	
3.1.0									TDC			DBRP								DTSEG1				DTSEG2				DSJW				

TEST (0x010)

3.0.1																			TDCV					RX	TX		LBCK					
3.1.0																								RX	TX		LBCK					

CCCR (0x018)

																		TXP	FDBS	FDO	CMR		CME		TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
3.1.0																		TXP	EFBI	PXHD			BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT

BTP -> NBTP (0x01C)

3.0.1							BRP												TSEG1							TSEG2					SJW		
3.1.0	NSJW								NBRP								NTSEG1										NTSEG2						

PSR (0x044)

																			REDL	RBRS	RESI	FLEC		BO	EW	EP	ACT	LEC				
3.1.0										TDCV								PXE	RFDF	RBRS	RESI	DLEC		BO	EW	EP	ACT	LEC				

TDCR (0x048)

3.0.1																																
3.1.0																		TDCO							TDCF							

IR (0x050)

3.0.1	STE	FOE	ACKE	BE	CRCE	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW	TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
3.1.0			ARA	PED	PEA	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW	TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N

IE (0x054)

3.0.1	STEE	FOEE	ACKEE	BEE	CRCEE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
3.1.0			ARAE	PEDE	PEAE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE

ILS (0x058)

3.0.1	STEL	FOEL	ACKEL	BEL	CRCEL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
3.1.0			ARAL	PEDL	PEAL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL

Figure 5: Registers modified / added from M_CAN / M_TTCAN R3.0.1 to R3.1.0

1. Appendix

1.1 List of Figures