ASSIGNMENT SET – III

Submission before 23/11/2020 at 00:00:00 hrs

Assignment Set III has to done after completing the Assignment Set I & II successfully. If you haven't done the Assignment Set I & II, please do this after completing Assignment Set I & II.

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all integrated circuits (IC) digital logic families.

The objective in Assignment- III is to build all the Sequential chips presented below. The only building blocks that you can use are primitive `DFF` gates, chips that you will build on top of them, and chips that you have built on ASSIGNMENT-I & ASSIGNMENT-II.

The only tool that you need for this project is the ModelSim - Intel FPGA Starter Edition. All the chips should be implemented in the HDL language using Verilog code.

The only building blocks that you can use are primitive `D Flip Flop`, chips that you will build on top of them, and chips described and developed in previous Assignments. As the assignment progress, students has to call / use the basic logical functions that is already implemented by him / her for building other logical functions.

The list of questions are shown below.

1. D Flip-Flop
    a. Rising-Edge
    b. Rising-Edge with Synchronous Reset
    c. Rising-Edge with Asynchronous Reset High Level
    d. Rising-Edge with Asynchronous Reset Low Level
    e. Falling-Edge
    f. Falling-Edge with Synchronous Reset
    g. Falling-Edge with Asynchronous Reset High Level
    h. Falling-Edge with Asynchronous Reset Low Level
2. 1-bit binary cell
3. 16-bit Register
4. RAM8 16-bit / 8-register memory
5. RAM64 16-bit / 64-register memory
6. RAM512 16-bit / 512-register memory
7. RAM4K 16-bit / 4096-register memory
8. RAM16K 16-bit / 16384-register memory
9. PC 16-bit Program Counter