Sense on Power Detection – Pin 21 (SOP2)

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Texas Instruments

Details of Issue

- Issue :
  - One of the LP3.x with PG1.32, SOP2 (PIN 21) which is pulled down with10K value is not getting detected value 0 correctly. Due to this, CC3200 stucks in UART Load Mode and do not execute the application.

- Root Cause:
  - It was found that strong (100uA nom, 300uA strong corner) internal pullup or pull down of the IO was getting triggered when the chip is applied power for the very first time.
  - When VDD_DIG is zero, if VDDIO is applied first time, the level-shifter latch inside the IO can get into an un-predictable state and enable the associated internal pull. The resulting pad voltage then gets latched at powerup (before digital core is powered up).

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Solution and Other Implications

- Solution :
  - SOP2/Pin 21pull-down to 2.7K for Functional Mode.
  - SOP2/Pin 21pull-up to 2.7K for UART Load Mode.

- Implications of Change
  - SOP2 can be used as Output Only pins for other functions. In active state of MCU and GPIO configured as output, it will drain ~1.25 mA.
  - For using external TCXO, this pin is used for TCXO Enable and will drain current as well.
  - When used as IO, it shall be driven by minimum 6 mA strength to swing it high up to 95%

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Similar behavior on other pins as well ?

- ***SOP 1(Pin 31) and SOP 0 (35)***
  - No Impact. SOP1, SOP0 has analog muxes in series that keeps them HIZ until reset completes.

- ***Other IOs***
  - *The state of the IOs are undefined in the time period between first time application of power to the chip and release of nRESET. If a certain set of pins are required to have a definite value during this pre-reset period, then an appropriate pull-up or down must be used at the board level. Recommended value of such external pull is 2.5Kohm."*

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