CC3101R SimpleLink™ – ARM® Cortex™ M4 Microcontroller With On-Chip 802.11bgn Wi-Fi® Network Processor

1 CC3101R SimpleLink – ARM Cortex M4 Microcontroller With On-Chip 802.11bgn Wi-Fi Network Processor

1.1 Features

- Application Processor
  - ARM Cortex M4
  - 80-MHz Operation
  - Up to 256 KB Local RAM
  - Support of Rich Peripherals Including:
    - I²C™ (Both Master and Slave)
    - Two SPIs: One Master Only and One Master and Slave
    - Two UARTs
    - Audio Serial Port (I2S)
    - Up to 24 GPIOs
    - 4 GPTs With PWM Functionality
    - 4-Channel ADC
    - Fast Parallel Input (For Example, Camera Interface)
- Hardware Crypto Engine for Fast State-of-the-Art Security
  - AES, DES, and 3DES
  - SHA and MD5
  - CRC and Checksum
- Wi-Fi
  - 802.11 b/g/n Station With Fully Integrated Radio, Baseband, and MAC
  - WPA2 Personal and Enterprise Security
  - Smart Config™ and WPS for Easy Provisioning
  - TX Power
    - 19.5 dBm @ 1 DSSS and 19.0 dBm @ 11 CCK
    - 14.5 dBm @ 54 OFDM
  - RX Sensitivity
    - –96.5 dBm @ 1 DSSS
    - –88.0 dBm @ 11 CCK
    - –74 dBm @ 54 OFDM
- Power Management
  - Integrated DC-DC With a Wide-Range Single Supply:
    - VBAT/Wide Voltage Mode: 2.1 to 3.6 V
    - Preregulated 1.8-V Mode
  - Low-Power Consumption
    - Hibernate with RTC: < 4 µA
    - Low-Power Deep Sleep: < 85 µA
    - RX Traffic: 53 mA @ 54 OFDM
    - TX Traffic: 210 mA @ 54 OFDM
- Clock Source
  - 40.0-MHz Crystal with Internal Oscillator
  - 32.768-kHz Crystal or External RTC Clock
- Easy Hardware Design
  - 0.5-mm Pitch, 64-Pin, 9-mm × 9-mm QFN Package for Easy Assembly and Low-Cost PCB Design
- Operating Conditions
  - Temperature Range: –40°C to 85°C (1)
- System Solution Features
  - Application Processor for Exclusive Application Development
  - Embedded Wi-Fi Connection Manager With No Application Processor Involvement
  - Smart Config Provisioning Utility for Configuring Displayless Devices Using a Smart Phone With a Single Click
  - BSD Socket APIs for Standard and Easy Internet Applications Development
  - Programmable Packet Filters in MAC and IP Layer to Optimize Power Consumption

(1) Actual system temperature range support is subject to peripheral component selection choices. See Section 12, *Reference Schematics*.

PRODUCT PREVIEW

1.2 Applications

- **Home Automation and Security**
- **Connected Appliances**
- **Smart Energy**
- **Industrial Automation**
- **Door Bell Camera**
- **Asset Tracking**
- **Machine-to-Machine (M2M) Communications**
- **Toys**
- **Wi-Fi Audio Streaming**
- **Internet of Things (IOT)**

1.3 Description

The CC3101R SimpleLink device (an ARM Cortex M4 microcontroller with an on-chip 802.11bgn Wi-Fi network processor) has an ARM Cortex M4 applications processor that is fully available for application development and rich peripheral interfaces to support a wide variety of network connectivity-based applications. The CC3101R device is footprint-compatible with the CC3100R device and has all of the Wi-Fi and networking features of the CC3100R device.

1.4 Functional Block Diagram

Figure 1-1 shows a functional block diagram of the CC3101R device.

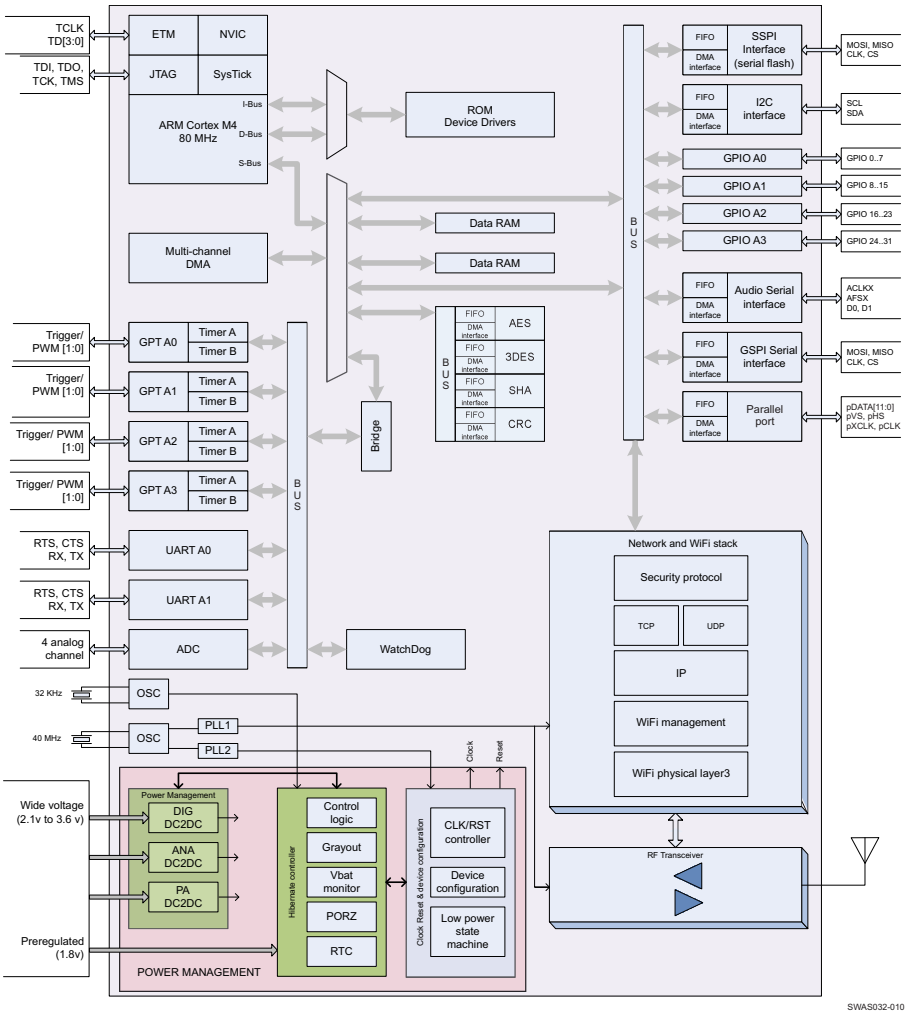


Figure 1-1. CC3101R Functional Block Diagram

PRODUCT PREVIEW

PRODUCT PREVIEW

2 Introduction

The CC3101R device has a rich set of peripherals for diverse application requirements. The device optimizes bus matrix and memory management to give needed advantage for the application developer. This section briefly highlights the internal details of the CC3101R device and offers suggestions for application configurations.

2.1 Application Diagram

Figure 2-1 shows the application diagram of the CC3101R SimpleLink Wi-Fi solution.

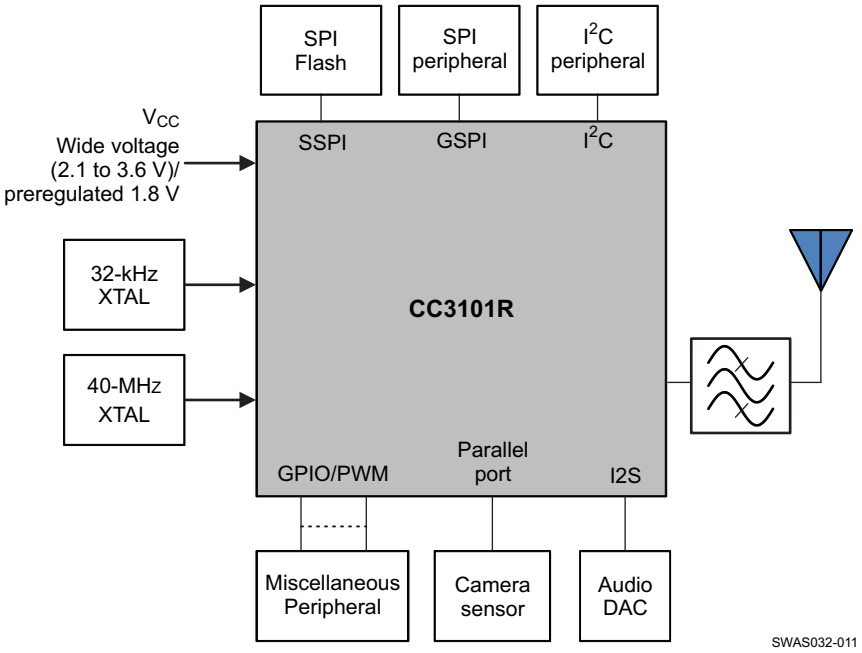


Figure 2-1. Application Diagram

2.2 Memory Map

Table 2-1 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

Table 2-1. Memory Map

Start Address	End Address	Description	Comment
0x0000.0000	0x0007.FFFF	On-chip ROM (Bootloader + DriverLib)	
0x2000.0000	0x2003.FFFF	Bit-banded on-chip SRAM	
0x2200.0000	0x23FF.FFFF	Bit-band alias of 0x2000.0000 through 0x200F.FFFF	
0x4000.0000	0x4000.0FFF	Watchdog timer A0	
0x4000.4000	0x4000.4FFF	GPIO port A0	
0x4000.5000	0x4000.5FFF	GPIO port A1	
0x4000.6000	0x4000.6FFF	GPIO port A2	
0x4000.7000	0x4000.7FFF	GPIO port A3	
0x4000.C000	0x4000.CFFF	UART A0	
0x4000.D000	0x4000.DFFF	UART A1	
0x4002.0000	0x4002.07FF	I^2C A0 (Master)	
0x4002.0800	0x4002.0FFF	I^2C A0 (Slave)	
0x4003.0000	0x4003.0FFF	General-purpose timer A0	
0x4003.1000	0x4003.1FFF	General-purpose timer A1	
0x4003.2000	0x4003.2FFF	General-purpose timer A2	
0x4003.3000	0x4003.3FFF	General-purpose timer A3	
0x400F.7000	0x400F.7FFF	Configuration registers	
0x400F.E000	0x400F.EFFF	System control	
0x400F.F000	0x400F.FFFF	µDMA	
0x4200.0000	0x43FF.FFFF	Bit band alias of 0x4000.0000 through 0x400F.FFFF	
0x4401.C000	0x4401.EFFF	McASP	
0x4402.0000	0x4402.0FFF	SSPI	Used for external serial flash
0x4402.1000	0x4402.2FFF	GSPI	Used by application processor
0x4402.5000	0x4402.5FFF	MCU reset clock manager	
0x4402.6000	0x4402.6FFF	MCU configuration space	
0x4402.D000	0x4402.DFFF	Global power, reset, and clock manager (GPRCM)	
0x4402.E000	0x4402.EFFF	MCU shared configuration	
0x4402.F000	0x4402.FFFF	Hibernate configuration	
0x4403.0000	0x4403.FFFF	Crypto range (includes apertures for all crypto-related blocks as follows)(1)	
0x4403.0000	0x4403.0FFF	DTHE registers and TCP checksum(1)	
0x4403.5000	0x4403.5FFF	MD5/SHA(1)	
0x4403.7000	0x4403.7FFF	AES(1)	
0x4403.9000	0x4403.9FFF	DES(1)	
0xE000.0000	0xE000.0FFF	Instrumentation trace Macrocell™	
0xE000.1000	0xE000.1FFF	Data watchpoint and trace (DWT)	
0xE000.2000	0xE000.2FFF	Flash patch and breakpoint (FPB)	
0xE000.E000	0xE000.EFFF	Nested vectored interrupt controller (NVIC)	
0xE004.0000	0xE004.0FFF	Trace port interface unit (TPIU)	
0xE004.1000	0xE004.1FFF	Reserved for embedded trace macrocell (ETM)	
0xE004.2000	0xE00F.FFFF	Reserved	

(1) Available with CC3101R1-S2RTD[T/R] part number

PRODUCT PREVIEW

2.3 CC3101 Variants

Table 2-2 lists the CC3101R variants, which are designed to address the varying memory requirements of diverse applications.

Table 2-2. CC3101R Variants

Part Number(1) (2)	RAM	NWP Security	MCU Security	Wi-Fi (2.4 GHz)
CC3101R1-M2RTD[T/R]	256K(3)	√		√
CC3101R1-S2RTD[T/R]	256K(3)	√	√	√
CC3101R1-M1RTD[T/R]	128K	√		√

(1) T = tape; R = reel
(2) The prototype device is identified by the letter X prefixed to the part number.
(3) The prototype device supports only 192K.

PRODUCT PREVIEW

3 ARM Cortex-M4 Processor Core

The high-performance ARM Cortex-M4 processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The ARM Cortex-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit ARM Cortex Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for ARMv6 little-endian accesses
  - Support for ARMv6 unaligned accesses
- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - Bits of priority configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  - Wake-up interrupt controller (WIC) providing ultra-low power sleep mode support
- Bus interfaces:
  - Three advanced high-performance bus (AHB-Lite) interfaces: ICode, DCode, and system bus interfaces
  - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Low-cost debug solution featuring:
  - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted
  - Serial wire debug port (SW-DP) or serial wire JTAG® debug port (SWJ-DP) debug access
  - Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

4 Internal Memory

The CC3101R device includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. To select the appropriate SRAM configuration, see the device variants listed in Table 2-2. The micro direct memory access (µDMA) controller can transfer data to and from SRAM and various peripherals. The CC3101R ROM holds the rich set of peripheral drivers, which saves precious SRAM memory space. For more information on drivers, see the CC3101R application programming interface (API) list.

4.1 SRAM

The CC3101R family provides up to 256KB of zero wait state, on-chip SRAM. Internal RAM has selective retention capability during low-power, deep-sleep mode. This internal SRAM is located at offset 0x2000.0000 of the device memory map.

The SRAM is also mapped to the bit-band region of the Cortex-M4 processor, thereby simplifying read-modify-write (RMW) operations that are otherwise very time consuming. With a bit-band enabled, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in a single, atomic operation.

With a bit band enabled, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in a single, atomic operation. The bit-band base is located at address 0x2200.0000.

The bit-band alias is calculated using the formula:

bit-band alias = bit-band base + (byte offset × 32) + (bit number × 4)

For example, To modify bit 3 at address 0x2000.1000, the bit-band alias is calculated as:

0x2200.0000 + (0x1000 × 32) + (3 × 4) = 0x2202.000C

With the alias address calculated, an instruction performing a read/write to address 0x2202.000C allows direct access only to bit 3 of the byte at address 0x2000.1000.

Use the µDMA controller to transfer data to and from the SRAM.

When the device enters low power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64 KB. For more information, see the API guide.

4.2 ROM

The internal zero-wait-state ROM of the CC3101R device is located at address 0x0000.0000 of the device memory and programmed with the following components:

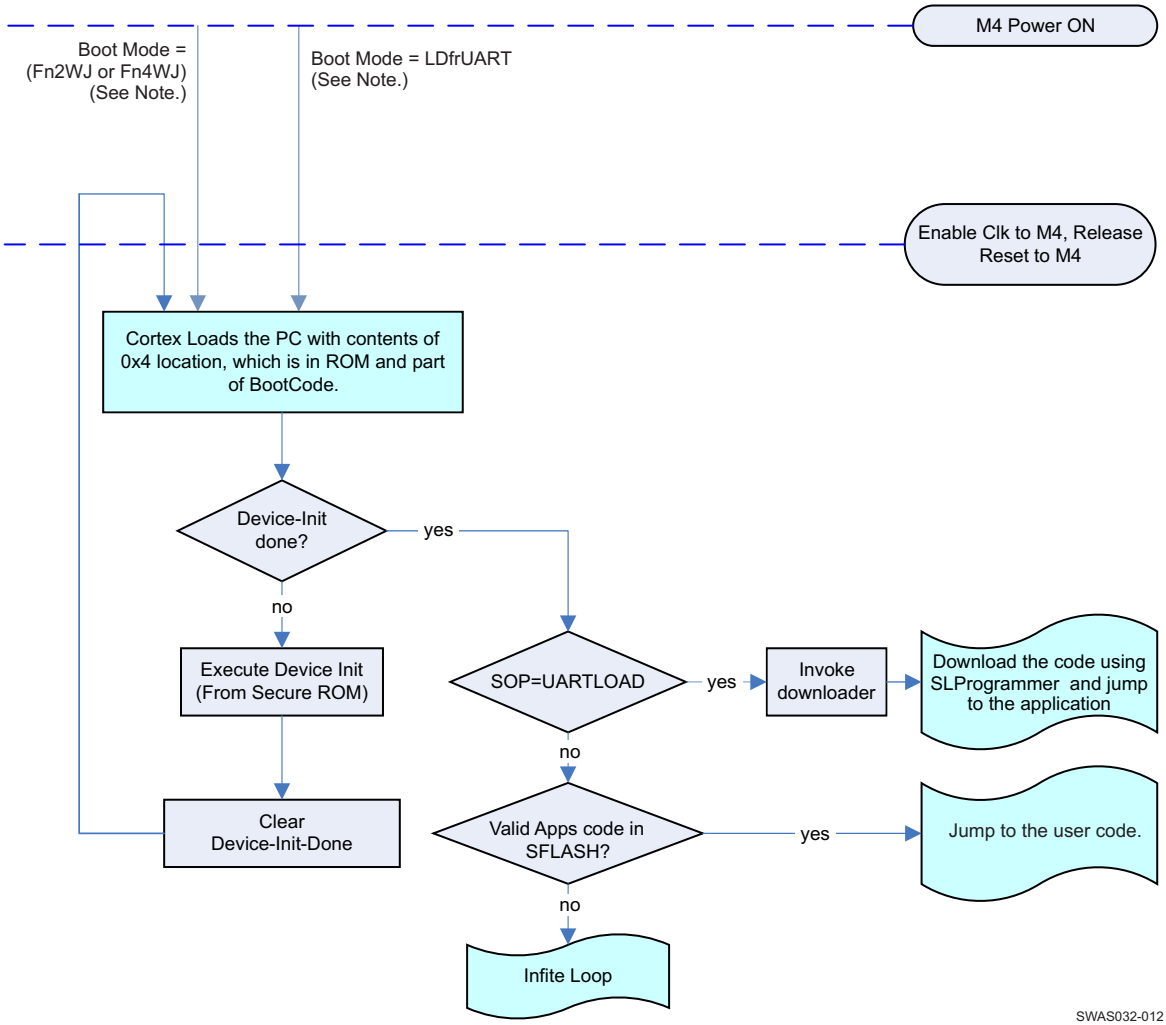
- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The boot loader is used as an initial program loader (when the serial flash memory is empty). The CC3101R DriverLib is a software library that controls on-chip peripherals with a boot-loader capability. The library performs both peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce flash memory requirements and free the flash memory to be used for other purposes.

4.3 Boot Overview

The boot process of the application processor includes two phases: the first phase consists of unrestricted access to all register space and configuration of the specific device setting. In the second phase, the application processor executes user-specific code.

Figure 4-1 shows the bootloader flow chart.



Note: For definitions of the SoP mode functional configurations, see Table 4-1.

Figure 4-1. Bootloader Flow Chart

The following events occur during the Cortex processor boot:

1. After power-on-reset (POR), the processor starts execution.
2. The processor jumps to the first few lines (FFL) of code in the ROM to determine if the current boot is the first device-init boot or the second MCU boot. The determination is based on the Device-Init flag in a secure register. The Device-Init flag is set out of POR. The registers in the secure region are accessible only in the device-init mode.
3. If the current boot is the first boot, the processor executes the device-init code from ROM.
4. At the end of the boot, the processor clears the Device-Init flag and changes the master ID of the processor and the DMA. These registers are part of the secure region.
5. The processor resets itself, initiating a second boot.
6. During the second boot, the processor rereads the Device-Init flag, the bit is cleared, and the processor obtains a different master ID.
7. After executing FFL and the unsecure boot code, the processor jumps to the developer code (application).
8. For the rest of the operation (until the next power cycle), the Cortex mode is designated MCU. During this phase, access to the secure region is restricted.

4.4 Boot Modes

Sense on Power (SoP) values are sensed from the device pin during power up. This encoding determines the boot flow. Three pins are used for this purpose. Before the device is taken out of reset, the SoP values are made available on a register and determine the device character while powering up. For production mode, use SoP mode Fn2WJ or Fn4WJ (see Table 4-1).

The SoP setting determines the device functional mode and does not define pin multiplexing. Table 4-1 defines the various functional configurations available for the CC31x1R device.

Table 4-1. CC31x1R Functional Configurations

SoP Mode	SoP[2]	SoP[1]	SoP[0]	Name	Comment
LDfrUART	Pullup	Pulldown	Pulldown	UARTLOAD (4-wire JTAG)	Factory/Lab Flash/SRAM load through UART
Fn2WJ	Pulldown	Pulldown	Pullup	FUNCTIONAL_2WJ	Functional development mode. In this mode, two-pin JTAG is available to the developer. TMS and TCK are available for debugger connection.
Fn4WJ	Pulldown	Pulldown	Pulldown	FUNCTIONAL_4WJ	Functional development mode. In this mode, four-pin JTAG is available to developer. TDI, TMS, TCK, and TDO are available for debugger connection.

5 Device Configuration

5.1 Pin Multiplexing

The device makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at device reset) and register control.

NOTE

TI highly recommends using the CC3101R pin multiplexing utility to obtain the desired pin out.

The hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used. The board and software designers are responsible for the proper pin multiplexing configuration.

Table 5-1 presents an overview of pin multiplexing. All pin multiplexing options are configurable using the pin mux registers that reside in the system control module.

Each pin can be configured in several ways. The mode number marks the function in which the pin is set to the particular mode.

NOTE

- All I/Os support driver strengths of 2, 4, 6, 8, 10, 12, and 14 mA. Driver strength is configurable individually for each pin.

  Some loading and speed restrictions apply to driver strengths of 8,10,12, and 14 mA.
- All I/Os support pullups and pulldowns of 10 µA.
- All I/Os operate on input supply (for details on input supply, see Section 10.1, *Input Supply Range*).

Table 5-1. CC3101R Pin Multiplexing

Pin	Signal Name	Description	Reset State
01	GPIO10	GPIO	Z
	I2C_SCL	I2C SCL	
	GT_PWM06	Pulse-width modulated output	
	COEX01	Coexistence interface	
	UART1_TX	UART TX	
	GT_CCP01	GP timer capture port	
02	GPIO11	GPIO	Z
	I2C_SDA	I2C SDA	
	GT_PWM07	Pulse-width modulated output	
	pXCLK	Parallel port clock	
	COEX00	Coexistence interface	
	UART1_RX	UART RX	
	GT_CCP02	GP timer capture port	
	McAFSX	Audio port frame sync	

PRODUCT PREVIEW

Table 5-1. CC3101R Pin Multiplexing (continued)

Pin	Signal Name	Description	Reset State
03	GPIO12	GPIO	Z
	McACLK	Audio port clock	
	pVS	Parallel port vertical sync	
	I2C_SCL	I2C SCL	
	UART0_TX	UART TX	
	GT_CCP03	GP timer capture port	
04	GPIO13	GPIO	Z
	pHS	Parallel port horizontal sync	
	I2C_SDA	I2C SDA	
	UART0_RX	UART RX	
	GT_CCP04	GP timer capture port	
05	GPIO14	GPIO	Z
	pDATA8	Parallel port data	
	I2C_SCL	I2C SCL	
	GSPI_CLK	General SPI clock	
	GT_CCP05	GP timer capture port	
06	GPIO15	GPIO	Z
	pDATA9	Parallel port data	
	I2C_SDA	I2C SDA	
	GSPI_MISO	General SPI MISO	
	GT_CCP06	GP timer capture port	
07	GPIO16	GPIO	Z
	pDATA10	Parallel port data	
	UART1_TX	UART TX	
	GSPI_MOSI	General SPI MOSI	
	GT_CCP07	GP timer capture port	
08	GPIO17	GPIO	Z
	pDATA11	Parallel port data	
	UART1_RX	UART RX	
	GSPI_CS	General SPI chip-select	
09	VDD_DIG1	Digital core supply. Connected to DIG DCDC output.	Z
10	VIN_IO1	VIO supply. Connected to VBAT.	Z
11	GPIO18	GPIO	Z
	SSPI_CLK	Flash SPI clock	
	GT_PWM00	Pulse-width modulated output	
12	GPIO19	GPIO	Z
	SSPI_MOSI	Flash SPI MOSI	
	GT_PWM01	Pulse-width modulated output	
13	GPIO20	GPIO	Z
	SSPI_MISO	Flash SPI MISO	
	GT_PWM02	Pulse-width modulated output	
	I2C_SCL	I2C SCL	

PRODUCT PREVIEW

Table 5-1. CC3101R Pin Multiplexing (continued)

Pin	Signal Name	Description	Reset State
14	GPIO21	GPIO	Z
	SSPI_CS	Flash SPI chip-select	
	GT_CCP03	GP timer capture port	
	GT_PWM03	Pulse-width modulated output	
	McAXR1	Audio port data	
	I2C_SDA	I2C SDA	
15	GPIO22	GPIO	Z
	GT_CCP04	GP timer capture port	
	McAFSX	Audio port frame synchronizer	
16	GPIO23	GPIO	Input
	TDI	JTAG TDI	
	UART1_TX	UART TX	
	McAHCLKX	Audio port clock(1)	
	McAXR1	Audio port data	
	COEX00	Coexistence interface	
	I2C_SCL	I2C SCL	
17	GPIO24	GPIO	Output
	TDO	JTAG TDO	
	UART1_RX	UART RX	
	SSPI_MISO	Flash SPI MISO	
	GT_CCP06	GP timer capture port	
	GT_PWM00	Pulse-width modulated output	
	McAFSX	Audio port frame synchronizer	
	COEX01	Coexistence interface	
	McAHCLKX	Audio port clock(1)	
	I2C_SDA	I2C SDA	
18	SSPI_CLK	Flash SPI clock	Z
	SSPI_MOSI	Flash SPI MOSI	
	McAHCLKX	Audio port clock(1)	
	COEX03	Coexistence interface	
	GT_CCP04	GP timer capture port	
19	GPIO28	GPIO	Input
	TCK	JTAG TCK	
	McAHCLKX	Audio port clock(1)	
	UART1_RX	UART RX	
	GT_PWM03	Pulse-width modulated output	
20	GPIO29	GPIO	Input
	TMS	JTAG TMS	
	UART1_TX	UART TX	
	GT_CCP00	GP timer capture port	

(1) Restricted use. Contact TI before using.

PRODUCT PREVIEW

Table 5-1. CC3101R Pin Multiplexing (continued)

Pin	Signal Name	Description	Reset State
21 (1)	GPIO25	GPIO	Z
	McAFSX	Audio port frame synchronizer	
	SSPI_MOSI	Flash SPI MOSI	
	COEX03	Coexistence interface	
	GT_PWM02	Pulse-width modulated output	
	COEX02	Coexistence interface	
	SOP2	See (2).	
22	WLAN_XTALM	Oscillator input	
23	WLAN_XTALP	Oscillator input	
24	VDD_PLL		
25	LDO_IN2	Analog RF supply. Connected to analog DC-DC output. (3)	
26	NC	Not connected	Z
27	NC	Not connected	Z
28	NC	Not connected	Z
29	GPIO26 (4)	Restricted use case	Z
30	GPIO27 (4)	Restricted use case	Z
31	RF_BG	RF BG band	
32	nRESET	Master chip reset (5)	
33	VDD_PA_IN	PA supply voltage. Connected to PA DC-DC output.	
34	SOP1	See (2).	Z
35	SOP0	See (2)	Z
36	LDO_IN1	Analog RF supply. Connected to analog DC-DC output. (3)	
37	VIN_DCDC_ANA	Analog buck converter input. Connected to external supply.	
38	DCDC_ANA_SW	Analog buck converter switching node. Connected to LC filter.	
39	VIN_DCDC_PA	PA buck converter input. Connected to external supply.	
40	DCDC_PA_SW_P	PA buck switching node. Connected to L+.	
41	DCDC_PA_SW_N	PA buck switching node. Connected to L–.	
42	DCDC_PA_OUT	PA buck converter output	
43	DCDC_DIG_SW	Digital buck converter switching node. Connected to LC filter.	

(1) This pin has dual functions: (a) as SOP[2] (device operation mode); and (b) as external TCXO enable. As TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is tristated but pulled down for SOP mode to disable TCXO. Because of SOP functionality, the pin must be used as output only.
(2) SOP is not a dedicated pin function: during power up, the state of the I/O is sensed to determine the device mode.
(3) For the LDO_IN and VDD_RAM connection, see Section 10.2, *Power Management Architecture*.
(4) These pins are used by the networking engine for antenna diversity. Use of these pins is restrictive. Updates will be provided in later versions.
(5) See the reference schematics (Figure 12-1).

PRODUCT PREVIEW

Table 5-1. CC3101R Pin Multiplexing (continued)

Pin	Signal Name	Description	Reset State
44	VIN_DCDC_DIG	Digital buck converter input. Connected to VBAT.	
45	GPIO31	GPIO	Z
	UART1_RX	UART RX	
	SSPI_CLK	Flash SPI clock	
	McAXR0	Audio port data	
	GSPI_CLK	General SPI clock	
	UART0_RX	UART RX	
	McAFSX	Audio port frame synchronizer	
	DCDC_ANA2_SW_P(1)	Buck boost converter switching node. Connected to L+.	
46	DCDC_ANA2_SW_N	Buck boost converter switching node. Connected to L+.	
47	VDD_ANA2	Buck boost converter output	
48	VDD_ANA1	Analog supply. Connected to analog DC-DC output.	
49	VDD_RAM	SRAM LDO output.(2)	
50	GPIO0	GPIO	Z
	UART0_RTS	UART request to send	
	McAFSX	Audio port frame synchronizer	
	McAXR1	Audio port data	
	GT_CCP00	GP timer capture port	
	GSPI_CS	General SPI chip-select	
	UART1_RTS	UART request to send	
	UART0_CTS	UART clear to send	
51	RTX_XTAL_P	RTC oscillator input	Z
52	GPIO32	GPIO	Z
	McACLK	Audio port clock	
	McAXR0	Audio port data	
	UART0_RTS	UART request to send	
	GSPI_MOSI	General SPI MOSI	
53	GPIO30	GPIO	Z
	SSPI_MISO	Flash SPI MISO	
	McACLK	Audio port clock	
	McAFSX	Audio port frame synchronizer	
	GT_CCP05	GP timer capture port	
	GSPI_MISO	General SPI MISO	
	McAHCLKX	Audio port clock(3)	
	UART0_TX	UART TX	
54	VIN_IO2	VIO supply. Connected to VBAT.	

(1) To use this pin as a digital function, pin 47 (VDD_ANA2) must be driven with VBAT. For details, see the reference schematics (Figure 12-1).
(2) For the LDO_IN and VDD_RAM connection, see Section 10.2, *Power Management Architecture*.
(3) Restricted use. Contact TI before using.

PRODUCT PREVIEW

Table 5-1. CC3101R Pin Multiplexing (continued)

Pin	Signal Name	Description	Reset State
55	GPIO1	GPIO	Z
	UART0_TX	UART TX	
	pCLK	Parallel port clock	
	UART1_TX	UART TX	
	GT_CCP01	GP timer capture port	
	COEX00	Coexistence interface	
56	VDD_DIG2	Digital core supply. Connected to DIG DC-DC output.	
57	GPIO2	GPIO	Z
	UART0_RX	UART RX	
	UART1_RX	UART RX	
	GT_CCP02	GP timer capture port	
	COEX01	Coexistence interface	
	ADC_CH0	ADC channel 0.(1)	
58	GPIO3	GPIO	Z
	pDATA7	Parallel port data	
	UART1_TX	UART TX	
	COEX02	Coexistence interface	
	ADC_CH1	ADC channel 1.(1)	
59	GPIO4	GPIO	Z
	pDATA6	Parallel port data	
	UART1_RX	UART RX	
	COEX03	Coexistence interface	
	ADC_CH2	ADC channel 2.(1)	
60	GPIO5	GPIO	Z
	pDATA5	Parallel port data	
	McAXR1	Audio port data	
	GT_CCP05	GP timer capture port	
	ADC_CH3	ADC channel 3.(1)	
61	GPIO6	GPIO	Z
	UART1_CTS	UART clear to send	
	pDATA4	Parallel port data	
	UART0_RTS	UART request to send	
	UART0_CTS	UART clear to send	
	GT_CCP06	GP timer capture port	
62	GPIO7	GPIO	Z
	UART1_RTS	UART request to send	
	UART0_RTS	UART request to send	
	UART0_TX	UART TX	
	McACLKX	Audio port clock	
63	GPIO8	GPIO	Z
	COEX03	Coexistence interface	
	McAFSX	Audio port frame synchronizer	
	GT_CCP06	GP timer capture port	

(1) To configure this pin as an ADC channel, see the API guide.

Table 5-1. CC3101R Pin Multiplexing (continued)

Pin	Signal Name	Description	Reset State
64	GPIO9	GPIO	Z
	GT_PWM05	Pulse-width modulated output	
	COEX02	Coexistence interface	
	McAXR0	Audio port data	
	GT_CCP00	GP timer capture port	

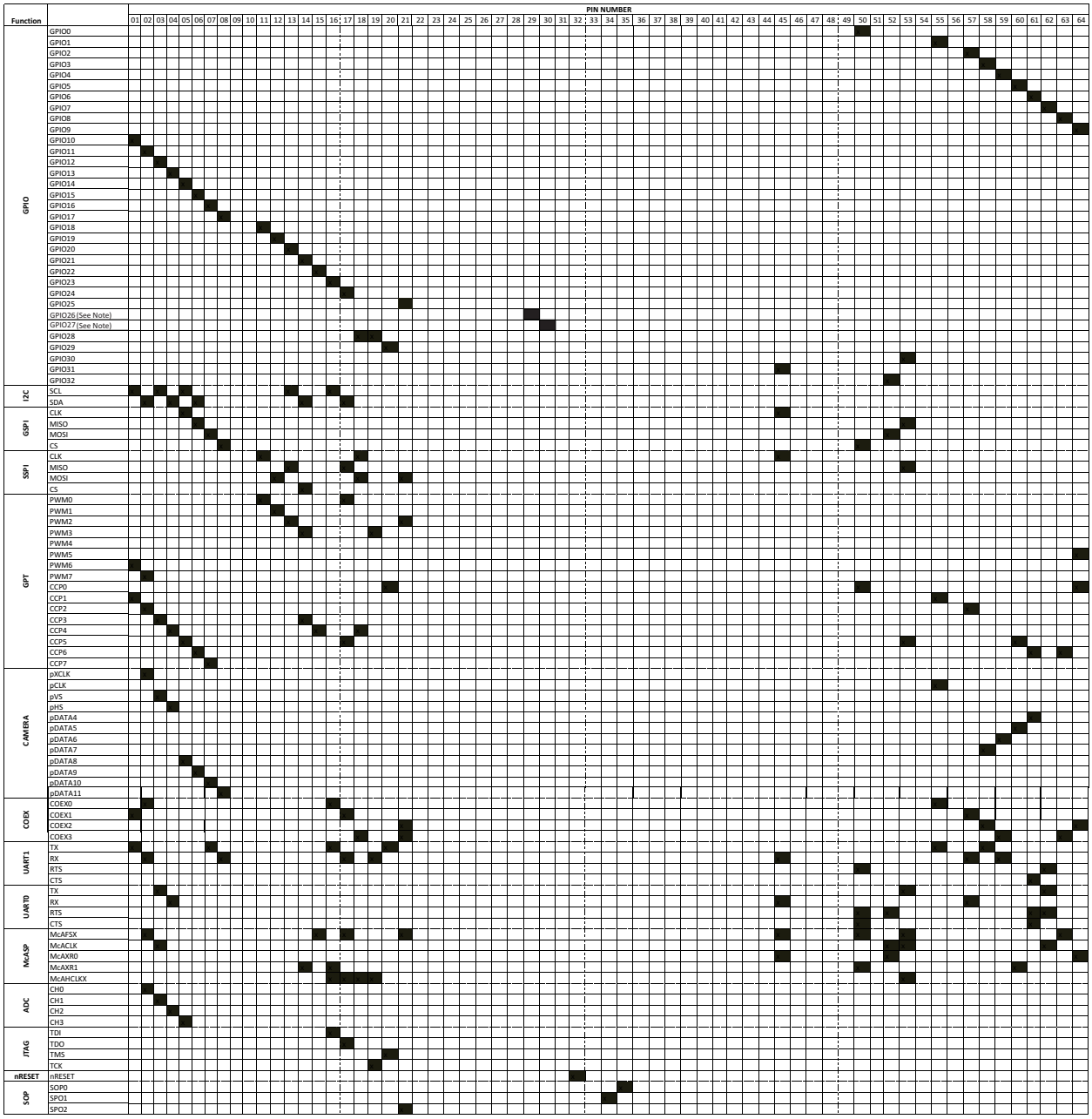
5.2 Pin Multiplexing – Matrix View

Table 5-2 and Table 5-3 present a matrix of the CC3101R pin multiplexing.

NOTE

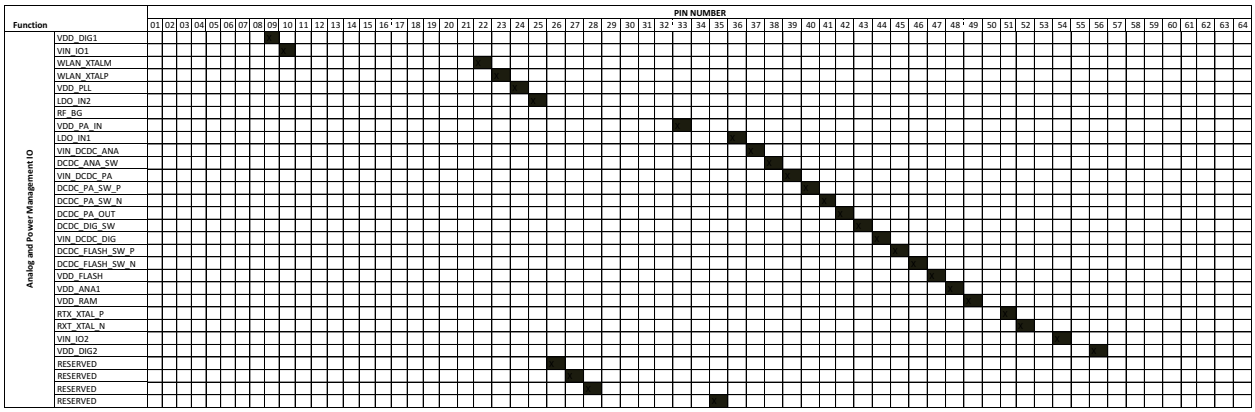
Use of GPIO26 and GPIO27 pins is restrictive.

Table 5-2. Pin Multiplexing – Matrix View (1 of 2)



Note: Restricted use

Table 5-3. Pin Multiplexing – Matrix View (2 of 2)



5.3 Suggested Use Cases

This section suggests pin multiplexing configurations for audio and video use cases.

NOTE

Alternate pin configurations are possible for similar use cases. For details, see the pin multiplexing matrix presented in Table 5-2 and Table 5-3.

5.3.1 Audio-Video Use Cases

Table 5-4 presents two examples of typical multiplexing configurations for audio and video use cases.

Table 5-4. Two Example Use Cases

Pin #	GPIO	CC3101R Device	
		Example 1: Wi-Fi Microphone	**Example 2: Wi-Fi Door Bell With Image Capture Device on Parallel Port**
		Audio + SPI + SPI + I2C + UART	**Audio + CAM + SPI + I2C**
1	GPIO10	I2CSCL	UART1_TX
2	GPIO11	I2CSDA	pXCLK
3	GPIO12		pVS
4	GPIO13		pHS
5	GPIO14	GSPI_CLK	pDATA[8]
6	GPIO15	GSPI_DIN	pDATA[9]
7	GPIO16	GSPI_DOUT	pDATA[10]
8	GPIO17	GSPI_CS	pDATA[11]
11	GPIO18	SSPI_CLK	SSPI_CLK
12	GPIO19	SSPI_DOUT	SSPI_DOUT
13	GPIO20	SSPI_DIN	SSPI_DIN
14	GPIO21	SSPI_CS	SSPI_CS
15	GPIO22		
16	GPIO23	TDI	I2CSCL
17	GPIO24	TDO	I2CSDA
18	GPIO28		
19	GPIO28	TCK	TCK
20	GPIO29	TMS	TMS

PRODUCT PREVIEW

Table 5-4. Two Example Use Cases (continued)

Pin #	GPIO	CC3101R Device	
		Example 1: Wi-Fi Microphone	Example 2: Wi-Fi Door Bell With Image Capture Device on Parallel Port
		Audio + SPI + SPI + I2C + UART	Audio + CAM + SPI + I2C
21	GPIO25		
29	GPIO26	Restricted use (see Figure 12-1)	
30	GPIO27		
45	GPIO31	Used as DCDC_ANA2_SW_P in prototype part	
50	GPIO0	McAXR1	McAXR1
52	GPIO32	Used as RTC_XTAL_N for RTC clock	
53	GPIO30	McACLKX/McACLKR	McACLKX/McACLKR
55	GPIO1	UART0_TX	pCLK
57	GPIO2	UART0_RX	pPWRDN
58	GPIO3	RTTT_TX	pDATA[7]
59	GPIO4	RTTT_RX	pDATA[6]
60	GPIO5	WL_LOGGER	pDATA[5]
61	GPIO6		pDATA[4]
62	GPIO7	NWP-LOGGER	NWP-LOGGER
63	GPIO8	McAFSX/McAFSR	McAFSX/McAFSR
64	GPIO9	McAXR0	McAXR0

Example 1 is an audio-only use case and supports GSPI for data storage. UART0 is available for other use cases, such as communicating to a *Bluetooth* device.

TI recommends bringing up various debug interfaces, the following of which are available:

- RTTT (UART port): interfaces with the radio test tool for radio tests (for example, placing the radio in basic test modes, such as continuous TX and RX modes at a specified rate and power). Radio tests are run though this interface to measure performance and identify issues.
- WLAN logger (UART logger): logs and prints debug messages in real time to help debug the layer 2 stack (MAC).
- Application logger (UART1-TX) UART interface: customers can use this interface to print debug messages for their own development.
- NWP logger (UART logger): prints real-time messages to help debug the layer 3 and layer 4 (TCP/IP) stacks.
- JTAG (debugger connection): supports 2-wire and 4-wire modes.

NOTE

Because example 2 uses the parallel port for image capture, only the application logger and the NWP logger are available for debug. The customer can use the 2-wire or the 4-wire debugger connection. The 4-wire connection uses the TCK, TMS, TDI, and TDO pins. The 2-wire connection uses the TCK and TMS pins. Using the 2-wire debug mode allows pins to be used for other use cases. TI recommends bringing up the debug interface on a connector or test port.

Configuration 2 is suitable for a camera use case requiring audio. The external storage available in this mode is SSPI. Pins not marked for use in Table 5-4 can be configured as GPIOs.

6 Secure Devices

The CC3101R family of devices offers secure device variants that let application developers protect the confidentiality of their intellectual property from external attacks. The CC3101R flash programmer encrypts the code using a device-specific key before writing the code to flash. The device-specific encryption and decryption key is detected only by the bootloader and cannot be accessed by any part of the application code. For more information, contact your Texas Instruments representative.

7 System Components

7.1 SysTick Timer

The SysTick integrated system timer provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter is clocked on the system clock.

SysTick makes OS porting between Cortex-M4 devices much easier because there is no need to change the OS system timer code. The SysTick timer integrates with the NVIC and can be used to generate a SysTick exception (exception type 15). In many OSs, a hardware timer generates interrupts so that the OS can perform task management (for example, to allow multiple tasks to run at different time slots and to ensure that no single task can lock up the entire system). To perform this function, the timer must be able to generate interrupts and, if possible, be protected from user tasks so that user applications cannot change the timer behavior.

Aside from being a system tick timer to the OS, the SysTick timer can be used in a number of ways (for example, an alarm timer, to measure time, and so on).

7.2 Nested Vector Interrupt Controller

The NVIC and Cortex-M4 processor prioritize and handle all exceptions in handler mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the interrupt service routine (ISR). The NVIC and the processor core interface are closely coupled to enable low-latency interrupt processing and efficient processing of late-arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail chaining of interrupts. The user can fully access the NVIC only from privileged mode.

The NVIC supports:

- Programmable priority level for each interrupt
- Low-latency interrupt and exception handling
- Level and pulse detection of interrupt signals
- Grouping of interrupts into group priority and subpriority interrupts
- Tail chaining of interrupts

Table 7-1 summarizes the interrupts supported by the device.

Table 7-1. Interrupts Supported

Interrupt	Description	Comments
0	GPIO Port A0	GPIO 0–7
1	GPIO Port A1	GPIO 8–15
2	GPIO Port A2	GPIO 16–23
3	GPIO Port A3	GPIO 24–31
5	UART A0	
6	UART A1	
8	I^2C A0	
14	ADC0 sequence 0	
15	ADC0 sequence 1	
16	ADC0 sequence 2	
17	ADC0 sequence 3	
18	Watchdog	
19	Timer A0A	
20	Timer A0B	
21	Timer A1A	
22	Timer A1B	

Table 7-1. Interrupts Supported (continued)

Interrupt	Description	Comments
23	Timer A2A	
24	Timer A2B	
35	Timer A3A	
36	Timer A3B	
46	µDMA software	µDMA0 completion interrupt
47	µDMA error	µDMA0 error interrupt
148	SHA(1)	SHA
151	AES(1)	AES
153	DES(1)	DES
161	McASP	
163	Camera parallel port	Camera parallel port interrupt
168	RAM WR error	Error interrupt generated if access is beyond the range of the specified data RAM allowed
171	NWP-IC	Interprocessor communication interrupt from NWP
172	PRCM	Power, reset, and clock controller
175	SSPI	
176	GSPI	
177	LSPI	Host interface (link between APPS and NWP)

(1) Available with the secure CC3101R variant

7.3 General-Purpose Timer

Programmable GPTs can be used to count or time external events that drive the timer input pins. Each GPT module (GPTM) block provides two 16-bit timers or counters that can be configured to operate independently as timers or event counters, or configured to operate as one 32-bit timer.

The GPTM contains GPTM blocks with the following functional options:

- Operating modes:
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 16-bit input-edge count- or time-capture modes
  - 16-bit pulse-width modulation (PWM) mode with software-programmable output inversion of the PWM signal
- Count up or down
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the ISR
- GPT can be used to trigger efficient transfers using the µDMA.
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt

7.4 Watchdog Timer

A watchdog timer is used to regain control when a system fails due to a software error or when an external device does not respond as expected. The watchdog timer can generate an interrupt or a reset when a time-out value is reached. In addition, the watchdog timer is ARM FiRM-compliant and can be configured to generate an interrupt to the microcontroller on its first time-out, and to generate a reset signal on its second time-out. Once the watchdog timer is configured, the lock register can be written to prevent the timer configuration from being inadvertently altered.

The watchdog timer provides the following features:

- 32-bit down-counter with a programmable load register

PRODUCT PREVIEW

- Programmable interrupt generation logic with interrupt masking
- Lock register protection from runaway software
- Reset generation logic with an enable and disable

7.5 Micro Direct Memory Access

The CC3101R microcontroller includes a DMA controller, or µDMA. The µDMA controller provides a way to offload data-transfer tasks from the Cortex-M4 processor, allowing more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfers between memory and peripherals and has dedicated channels for each supported on-chip module. The µDMA controller can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

The µDMA controller provides the following features:

- 32 configurable channels
- 80-MHz operation
- Support for memory to memory, memory to peripheral, and peripheral to memory in multiple transfer modes
  - Basic for simple transfer scenarios
  - Ping-pong for continuous data flow
  - Scatter-gather for a programmable list of arbitrary transfers initiated from a single request
- Highly flexible and configurable channel operation
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules
  - One channel each for receive and transmit path for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable bus arbitration scheme
  - Software-initiated requests for any channel
- Two levels of priority
- Design optimizations for improved bus access performance between the µDMA controller and the processor core
  - µDMA controller access subordinate to core access
  - Simultaneous concurrent access
- Data sizes of 8, 16, and 32 bits
- Transfer size is programmable in binary steps from 1 to 1024
- Source and destination address increment size of byte, half-word, word, or no increment
- Maskable peripheral requests
- Interrupt on transfer completion, with a separate interrupt per channel

7.5.1 Channel Assignment

Table 7-2 describes the µDMA channel allocation, with 32 channels assigned to various peripherals. Peripherals are mapped at multiple places to address the application needs in which any combination of peripherals can be used in tandem.

Table 7-2. µDMA Channel Assignment(1)

DMA Channel Map Encoding	0	1	2	3
Channel				
0	GPTimer A0-A	MD5/SHA Adv Cin(2)		Software
1	GPTimer A0-B	MD5/SHA Adv Din(2)		Software
2	GPTimer A1-A	MD5/SHA Adv Cout(2)		Software
3	GPTimer A1-B	DES Cin(2)		Software
4	GPTimer A2-A	DES Din(2)	McASP A0 (RX)	Software
5	GPTimer A2-B	DES Dout(2)	McASP A0 (RX)	Software
6	GPTimer A3-A	GSPI (RX)	GPIO A2	Software
7	GPTimer A3-B	GSPI (TX)	GPIO A3	Software
8	UART A0 (RX)	GPTimer A0-A	GPTimer A2-A	Software
9	UART A0 (TX)	GPTimer A0-B	GPTimer A2-B	Software
10	UART A1 (RX)	GPTimer A1-A	GPTimer A3-A	Software
11	UART A1 (TX)	GPTimer A1-B	GPTimer A3-B	Software
12	LSPI (RX) (link)			Software
13	LSPI (TX) (link)			Software
14	ADC 0			Software
15	ADC 2			Software
16	ADC 4	GPTimer A2-A		Software
17	ADC 6	GPTimer A2-B		Software
18	GPIO A0	AES Cin(2)	McASP A0 (RX)	Software
19	GPIO A1	AES Cout(2)	McASP A0 (RX)	Software
20	GPIO A2	AES Din(2)		Software
21	GPIO A3	AES Dout(2)		Software
22	Parallel port			
23		GPTimer A3-A	GPTimer A2-A	Software
24		GPTimer A3-B	GPTimer A2-B	Software
25	SSPI (RX) (shared)	I^2C A0 RX (shared)		Software
26	SSPI (TX) (shared)	I^2C A0 TX (shared)		Software
27		GPIO A0		Software
28		GPIO A1		Software
29				Software
30	GSPI (RX)		I^2C S0 RX (shared)	Software
31	GSPI (TX)		I^2C S0 TX (shared)	Software

(1) Gray cells denote reserved. All other cells are CC3101R-specific DMA requests.
(2) Available with the secure CC3101R variant

PRODUCT PREVIEW

7.5.2 Transfer Mode

The µDMA controller supports several transfer modes. Two of the modes support simple one-time transfers. Several complex modes support a continuous flow of data.

7.5.2.1 Stop Mode

Although not a transfer mode, stop mode is a valid value for the mode field of the control word. When the mode field has this value, the µDMA controller does not perform any transfers and disables the channel if enabled.

7.5.2.2 Basic Mode

In basic mode, the µDMA controller performs transfers as long as there are items to transfer and a transfer request is present. Basic mode is used with peripherals that assert a µDMA request signal whenever the peripheral is ready for a data transfer. Basic mode must not be used in any situation where the request is momentary even though the entire transfer must be completed. For example, a software-initiated transfer creates a momentary request and, in basic mode, only the number of transfers specified by the ARBSIZE field in the DMA Channel Control Word register is transferred on a software request, even if there is more data to transfer. When all of the items are transferred using basic mode, the µDMA controller sets that channel to stop mode.

7.5.2.3 Auto Mode

Auto mode is similar to basic mode, except that once a transfer request is received, the transfer runs to completion, even if the µDMA request is removed. This mode is suitable for software-triggered transfers. Generally, auto mode is not used with a peripheral. When all items are transferred using auto mode, the µDMA controller sets that channel to stop mode.

7.5.2.4 Ping-Pong Mode

Ping-pong mode supports a continuous data flow to or from a peripheral (see Figure 7-1). To use ping-pong mode, both the primary and alternate data structures must be implemented. Both structures are set up by the processor for data transfer between memory and a peripheral. The transfer is started using the primary control structure. When the transfer using the primary control structure is complete, the µDMA controller reads the alternate control structure for that channel to continue the transfer. Each time this happens, an interrupt is generated, and the processor can reload the control structure for the just-completed transfer. Data flow can continue indefinitely this way, using the primary and alternate control structures to switch back and forth between buffers as the data flows to or from the peripheral.

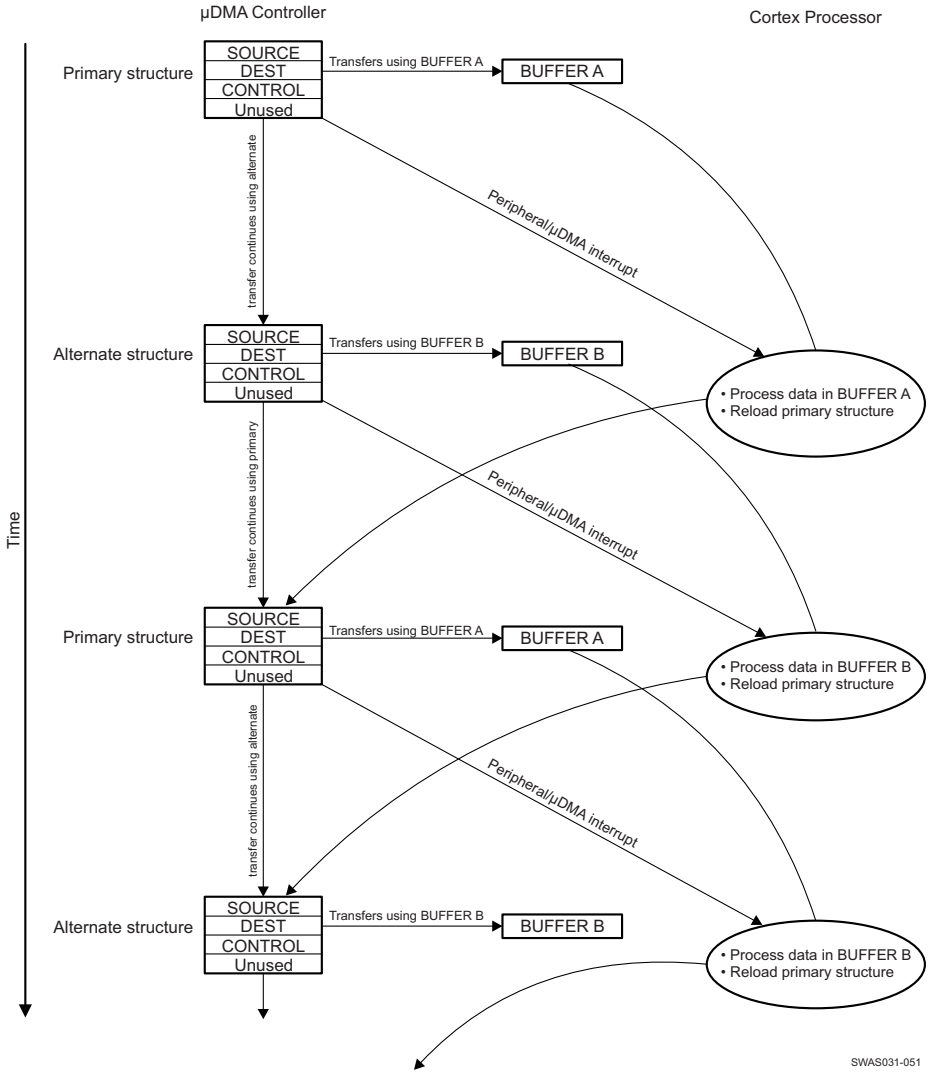


Figure 7-1. Ping-Pong Mode Transfer Flow

7.5.2.5 Memory Scatter-Gather Mode

Memory scatter-gather mode is a complex mode used when data must be transferred to or from varied locations in memory rather than a set of contiguous locations in a memory buffer (see Figure 7-2). For example, a gather µDMA operation can be used to selectively read the payload of several stored packets of a communication protocol and store them together in sequence in a memory buffer. In memory scatter-gather mode, the primary control structure is used to program the alternate control structure from a table in memory. The table is set up by the processor software and contains a list of control structures, each containing the source and destination end pointers along with the control word for a specific transfer. The mode of each control word must be set to scatter-gather mode. Each entry in the table is copied in turn to the alternate structure where it is then executed. The µDMA controller alternates between using the primary control structure to copy the next transfer instruction from the list and then executing the new transfer instruction. The end of the list is marked by programming the control word for the last entry to use basic transfer mode.

Once the last transfer is performed using basic mode, the µDMA controller stops. A completion interrupt is generated only after the last transfer. Looping the list is possible by having the last entry copy the primary control structure to point back to the beginning of the list (or to a new list).

PRODUCT PREVIEW

In addition, a set of other channels can be triggered to perform a transfer, either directly by programming a write to the software trigger for another channel, or indirectly by causing a peripheral action that results in a µDMA request.

By programming the µDMA controller using this method, a set of arbitrary transfers can be performed based on a single µDMA request.

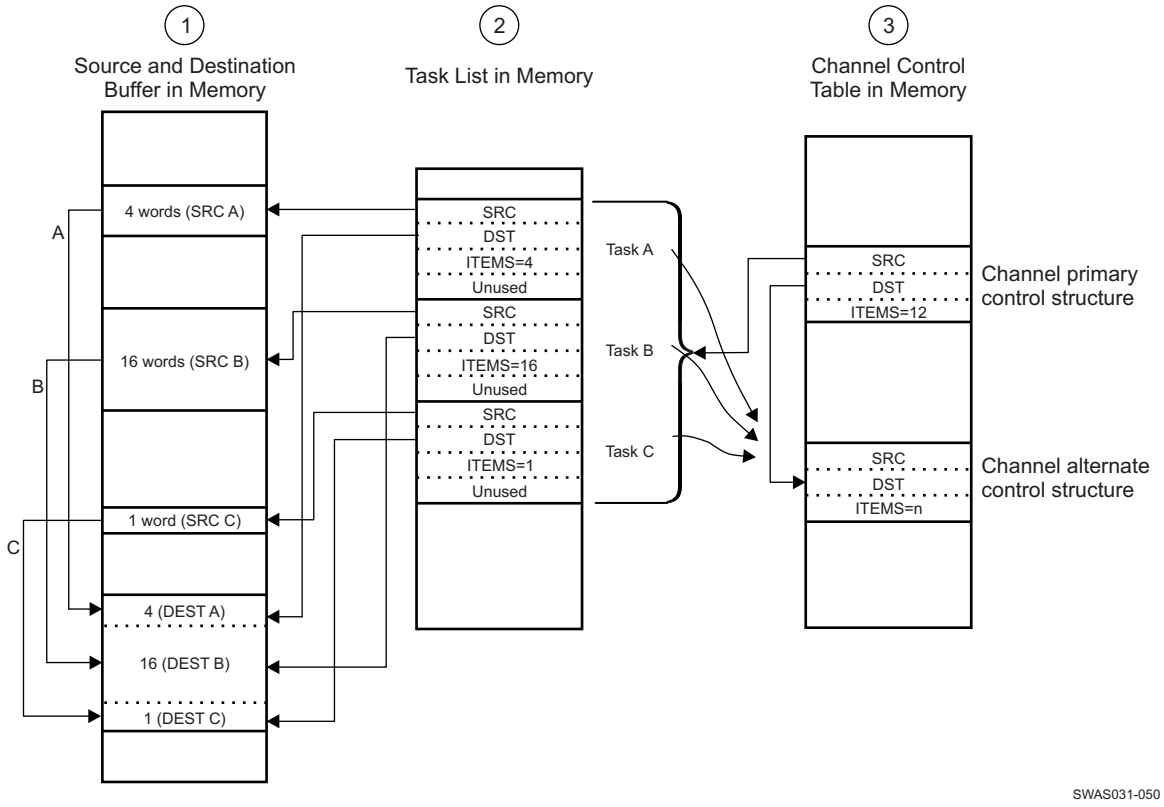


Figure 7-2. Memory Scatter-Gather Mode

NOTE

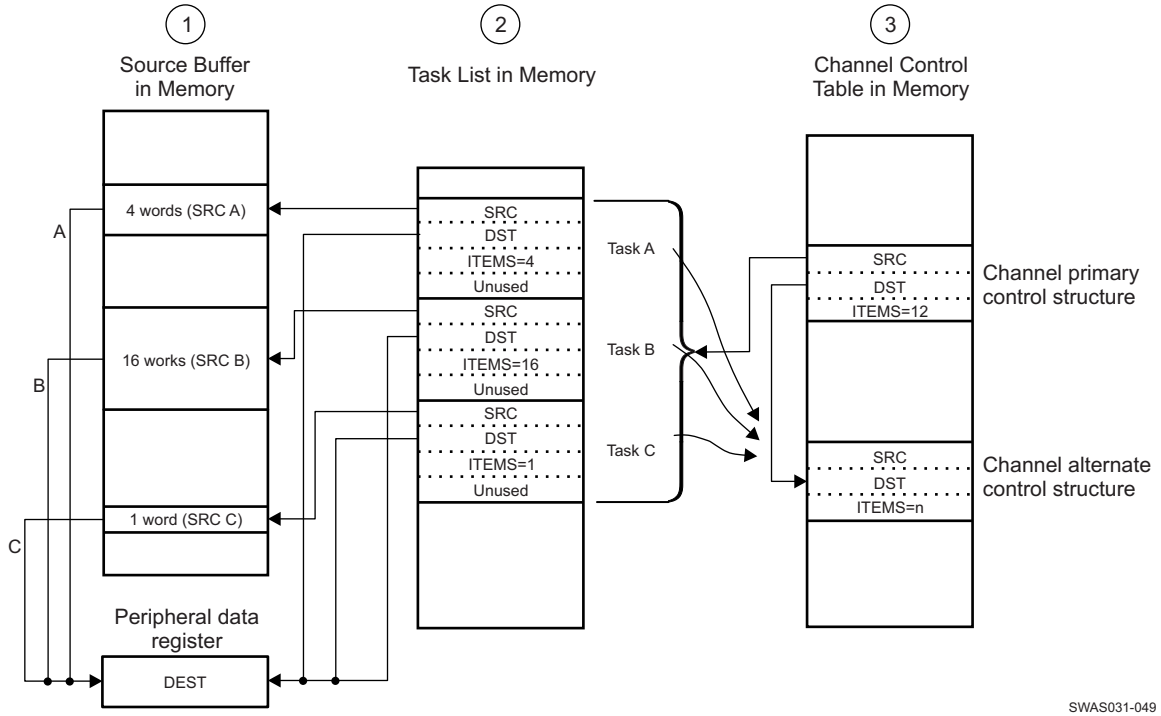
In Figure 7-2:

- Column 1: The application must copy data items from three separate locations in memory into one combined buffer.
- Column 2: The application sets up a µDMA task list in memory, which contains the pointers and control configuration for three µDMA copy tasks.
- Column 3: The application sets up the channel primary control structure to copy each task configuration, one at a time, to the alternate control structure, where the task configuration is executed by the µDMA controller.

7.5.2.6 Peripheral Scatter-Gather Mode

Peripheral scatter-gather mode is similar to memory scatter-gather mode, except that a peripheral making a µDMA request controls the transfers (see Figure 7-3). When a request from the peripheral is detected, the µDMA controller uses the primary control structure to copy one entry from the list to the alternate control structure and then performs the transfer. At the end of this transfer, the next transfer is started only if the peripheral again asserts a µDMA request. The µDMA controller continues to perform transfers from the list only when the peripheral is making a request until the last transfer is complete. A completion interrupt is generated only after the last transfer.

Using this method lets the µDMA controller transfer data to or from a peripheral from a set of arbitrary locations whenever the peripheral is ready to transfer data.



A.

1. Column 1: The application must copy data items from three separate locations in memory into a peripheral data register.
2. Column 2: The application sets up a µDMA task list in memory, which contains the pointers and control configuration for three µDMA copy tasks.
3. Column 3: The application sets up the channel primary control structure to copy each task configuration, one at a time, to the alternate control structure, where it is executed by the µDMA controller.

Figure 7-3. Peripheral Scatter-Gather Mode

7.6 Data Hashing and Transform Engine

Cryptographic accelerators are available to the application processor only in the secure variant (CC3101R1-S2RTD). For more information about the secure variant, contact your TI representative.

PRODUCT PREVIEW

8 Peripherals

This section describes the peripherals that the CC3101R device supports.

8.1 General-Purpose Input/Output

All digital pins of the device can be used as a general-purpose input/output (GPIO). GPIOs can be used for various purposes. The GPIO module consists of four GPIO blocks:

- GPIO A0
- GPIO A1
- GPIO A2
- GPIO A3

Each GPIO block provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used.

Figure 8-1 shows the GPIO module block diagram.

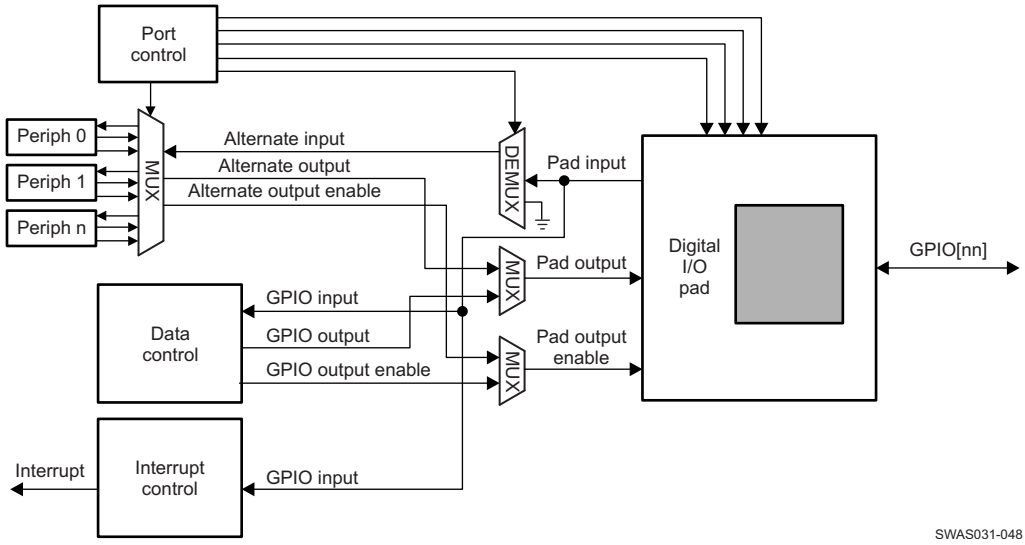


Figure 8-1. GPIO Module Block Diagram

The GPIO module provides the following features:

- CC3101R support for up to 24 GPIOs, depending on the configuration
- Interrupt capability for all GPIO pins
  - Level or edge sensitive
  - Rising or falling edge
  - Selective interrupt masking
- Can be used to trigger DMA operation
- Programmable pad configurable
  - Configurable pullup and pulldown strength: Weak is 10 µA
  - Configurable drive strength
    - 2, 4, 6, 8, 10, 12, and 14 mA
    - Open-drain enable
- GPIO register readable through the high-speed internal bus matrix

PRODUCT PREVIEW

8.2 Universal Asynchronous Receivers/Transmitters

A universal asynchronous receivers/transmitter (UART) is an integrated circuit used for RS-232 serial communications. UARTS contain a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter), each clocked separately.

Figure 8-2 shows a block diagram of the UART.

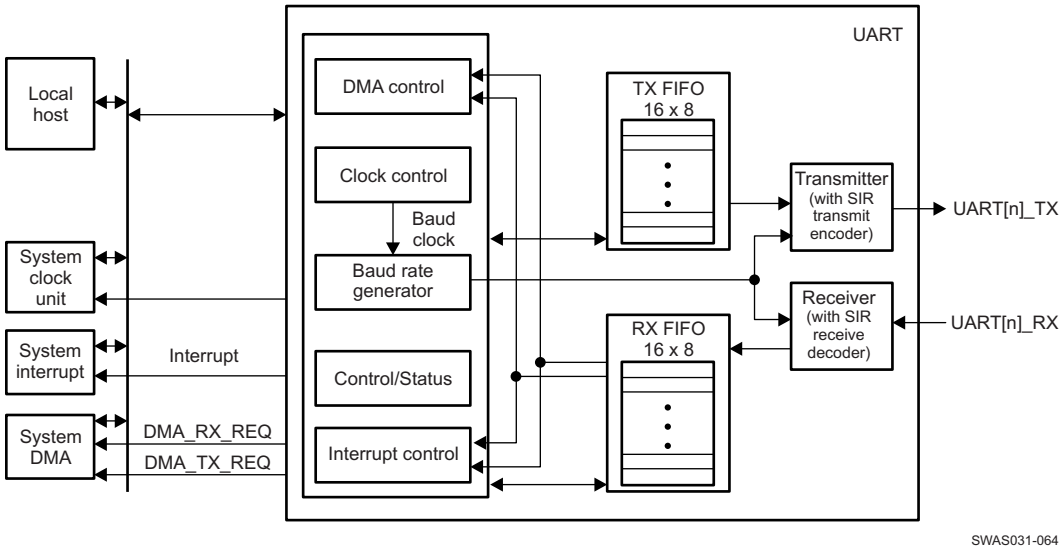


Figure 8-2. UART Block Diagram

The CC3101R device includes two fully programmable UARTs. The UART can generate individually masked interrupts from the RX, TX, modem status, and error conditions. The module generates a single combined interrupt when any of the interrupts are asserted and unmasked.

The UARTs include the following features:

- Programmable baud-rate generator allowing speeds up to 3 Mbps
- Separate 16 x 8 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation/detection
  - 1 or 2 stop-bit generation
- RTS and CTS modem handshake support
- Standard FIFO-level and end-of-transmission interrupts
- Efficient transfers using µDMA
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level

PRODUCT PREVIEW

8.3 Serial Peripheral Interface

The serial peripheral interface (SPI) is a four-wire bidirectional communications interface that converts data between parallel and serial. The SPI module performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data transmitted to a peripheral device.

The SPI module can be configured as either a master or slave device. As a slave device, the SPI module can also be configured to disable its output, which allows a master device to be coupled with multiple slave devices. The TX and RX paths are buffered with separate internal FIFOs.

The SPI module also includes a programmable bit rate clock divider to generate the output serial clock derived from the input clock of the SPI module. Bit rates are generated based on the input clock and the maximum bit rate is determined by the connected peripheral.

The SPI allows a duplex serial communication between a local host and SPI-compliant external devices (slaves and masters). Figure 8-3 shows a high-level overview of the SPI system.

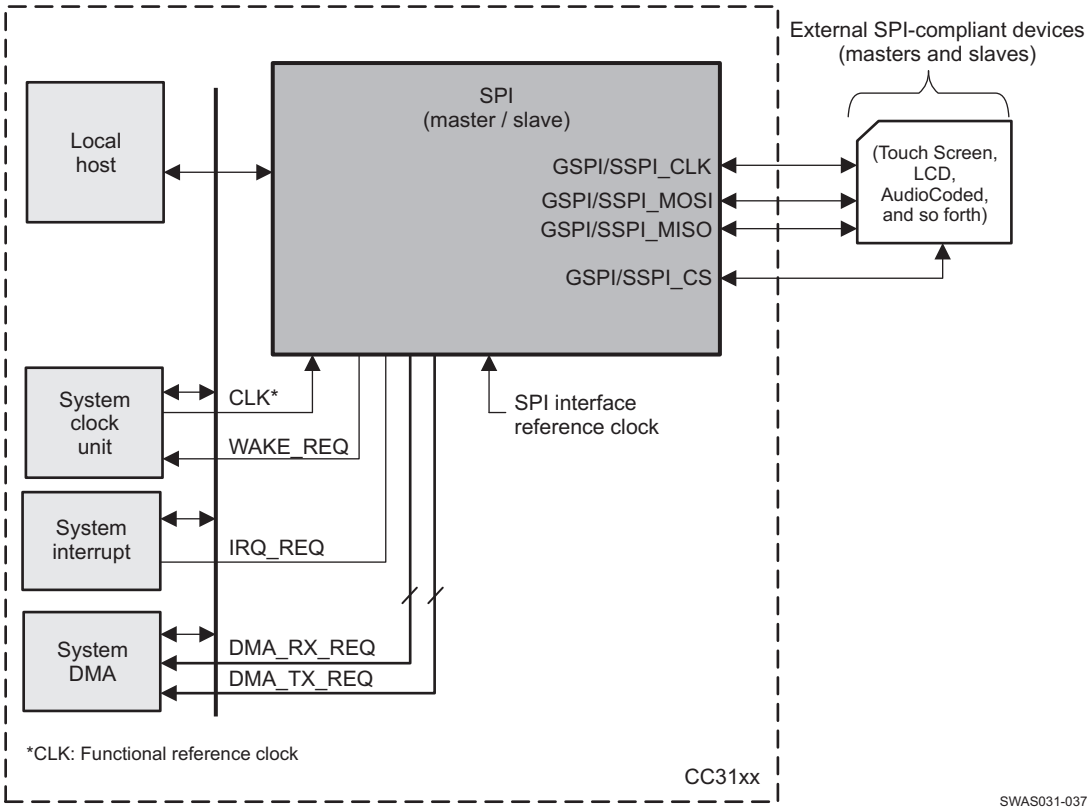


Figure 8-3. SPI Block Diagram

The SPI includes these distinctive features:

- Serial clock with programmable frequency, polarity, and phase
- Clock frequency granularity can be changed to power of 2.
- SPI enable
  - Generation programmable
  - Programmable polarity
- Wide selection of SPI word lengths continuous at 8, 16, and 32 bits
- Support of both master and slave modes

- Mode of operation
  - Support of full duplex and half duplex
  - Support of transmit and receive modes
- Independent DMA requests for read and write
- Programmable delay before the first SPI word is transmitted.
- No dead cycle between two successive words in slave mode
- Multiple SPI word access with a channel using an enabled FIFO
- Programmable timing control between chip select and external clock generation

The SPI allows a duplex serial communication between a local host and SPI-compliant external devices (slaves and masters).

8.3.1 SPI Modes

The SPI is a serial protocol that allows a master device to initiate serial communication with a slave device.

8.3.1.1 Two Data-Pin Interface Mode

The two data-pin interface mode allows a full-duplex SPI transmission in which data is transmitted (shifted out serially) and received (shifted in serially) simultaneously on separate data lines (SPIDAT[0] and SPIDAT[1]). Data leaving the master exits on a transmit serial data line also known as MasterOutSlaveIn (MOSI). Data leaving the slave exits on a receive data line also known as MasterInSlaveOut (MISO).

Figure 8-4 shows the SPI full-duplex transmission.

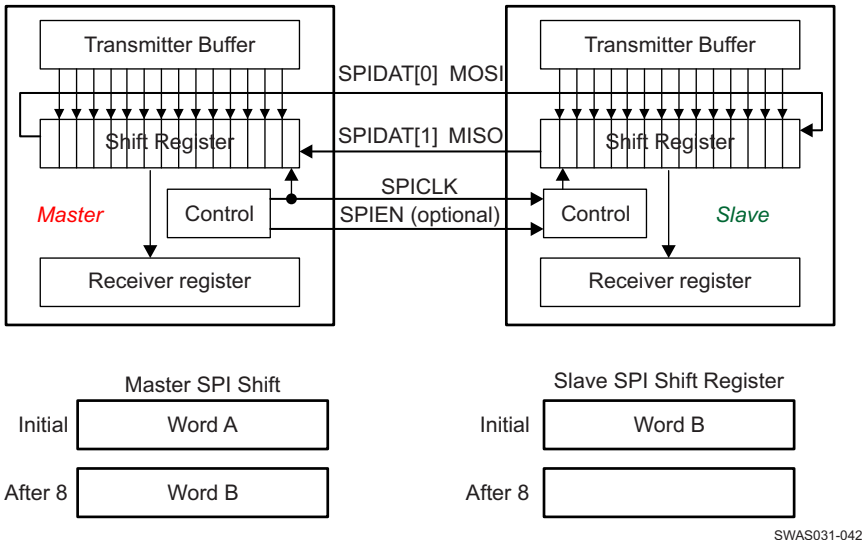


Figure 8-4. SPI Full-Duplex Transmission

8.3.2 3-Pin or 4-Pin SPI

The external SPI bus interface can be configured to use a restricted set of pins depending on the targeted application:

- The SPI can be configured to use three pins only based on pin constraint.
- The pins used in 3-pin mode are CLKSPI, MOSI, and MISO.

Figure 8-5 shows the 3-pin SPI mode.

PRODUCT PREVIEW

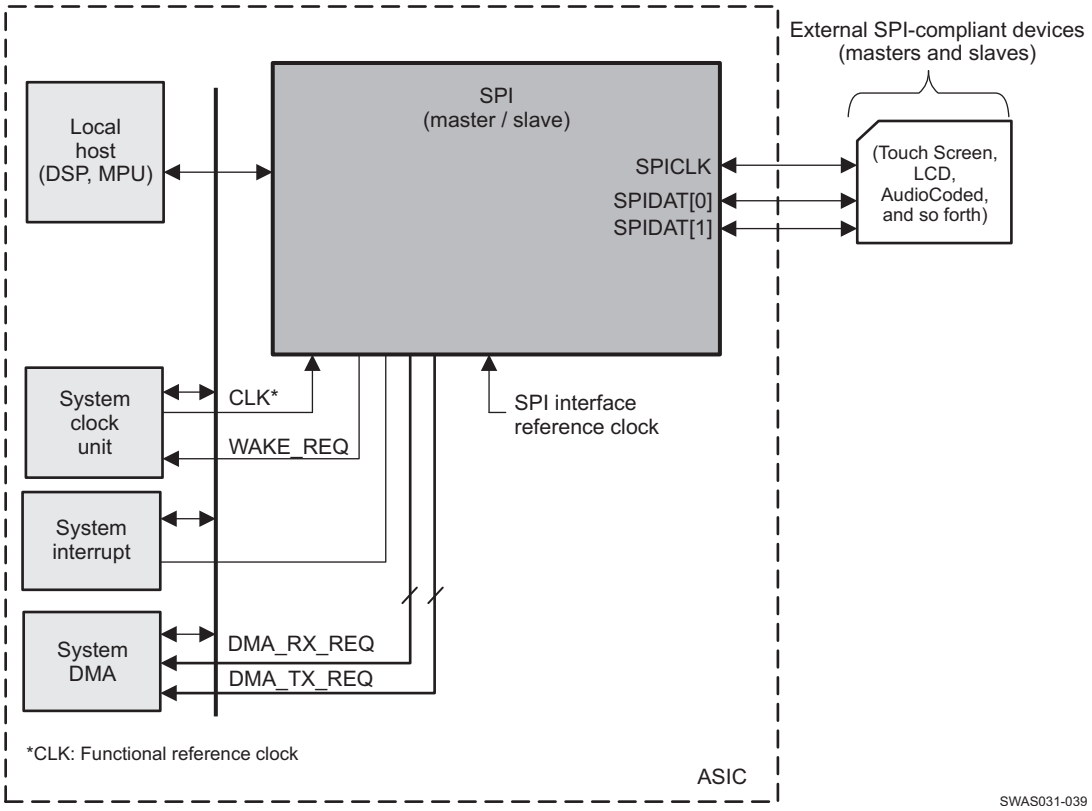


Figure 8-5. 3-Pin SPI Mode

8.4 I²C Interface

The inter-integrated circuit (I^2C) bus provides bidirectional data transfer through a two-wire design (a serial data line SDA and a serial clock line SCL). The I^2C bus interfaces to external I^2C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on.

Figure 8-6 shows the I^2C block diagram.

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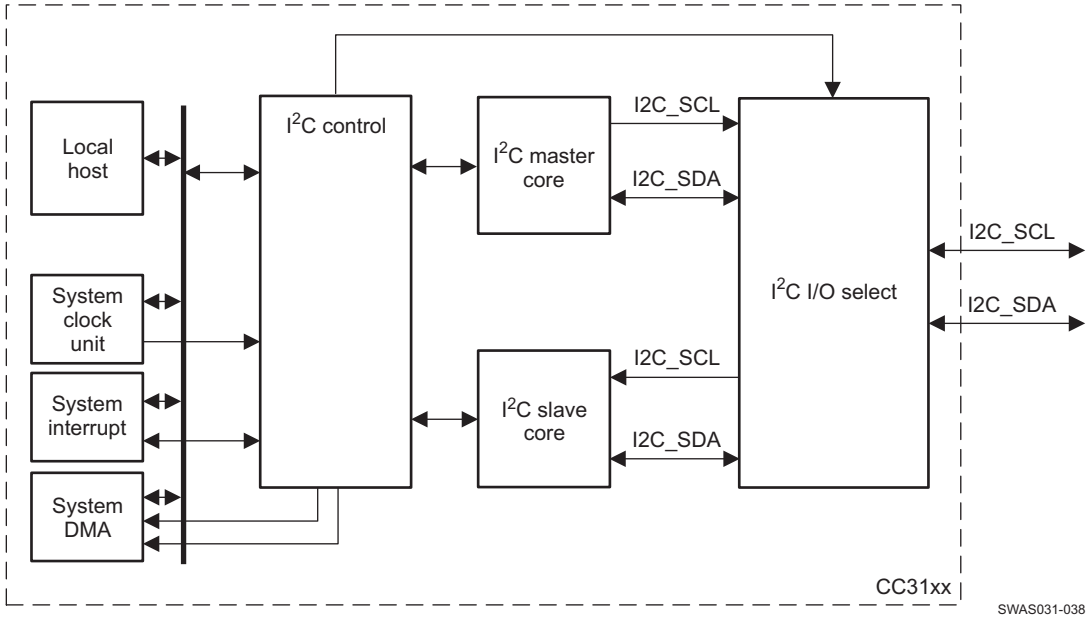


Figure 8-6. I²C Block Diagram

Each device on the I²C bus can be designated as either a master or a slave. Each I²C module supports both sending and receiving data as either a master or a slave and can operate simultaneously as both a master and a slave. Both the I²C master and slave can generate interrupts.

The CC3101R microcontroller includes one I²C module with the following features:

- Devices on the I²C bus can be designated as either a master or a slave.
  - Supports both transmitting and receiving data as either a master or a slave
  - Supports simultaneous master and slave operation
- Four I²C modes
  - Master transmit
  - Master receive
  - Slave transmit
  - Slave receive
- Two transmission speeds
  - Standard (100 Kbps)
  - Fast (400 Kbps)
- Master and slave interrupt generation
  - Master generates interrupts when a transmit or receive operation completes (or aborts due to an error).
  - Slave generates interrupts when data is transferred or requested by a master or when a START or STOP condition is detected.
- Master with arbitration and clock synchronization, multimaster support, and 7-bit addressing mode

The I²C bus uses only two signals:

- SDA
- SCL

PRODUCT PREVIEW

SDA is the bidirectional serial data line and SCL is the bidirectional serial clock line. The bus is considered idle when both lines are high. Every transaction on the I^2C bus is 9 bits long, consisting of 8 data bits and 1 acknowledge bit. The number of bytes per transfer (defined as the time between a valid START and STOP condition) is unrestricted, but each byte must be followed by an acknowledge bit, and data must be transferred MSB first. When a receiver cannot receive another complete byte, the receiver can hold the clock line SCL low and force the transmitter into a wait state. The data transfer continues when the receiver releases the clock SCL.

For proper operation, the SDA and SCL pins must be connected to bidirectional open-drain pads. Figure 8-7 shows a typical I^2C bus configuration.

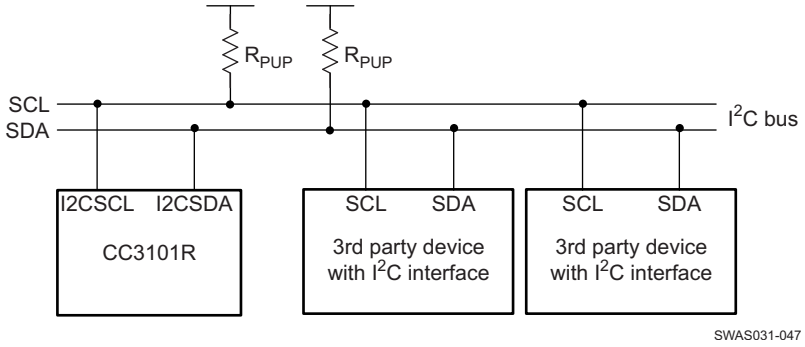


Figure 8-7. I^2C Bus Configuration

8.5 Multichannel Audio Serial Port Interface

The multichannel audio serial port (McASP) interface functions as a general-purpose audio serial port optimized for multichannel audio applications.

The McASP consists of transmit and receive sections that operate synchronized. The McASP module also includes two serializers that can be individually enabled to either transmit or receive.

The McASP is intended to be flexible enough so that it can connect gluelessly to audio A/D, D/A, CODEC, and DIR transmit physical layer components.

The McASP includes the following features:

- Glueless connection to audio analog-to-digital converters (ADCs), digital-to-analog converters (DACs), codec, and digital audio interface receiver (DIR)
- Support of a fractional divider for bit-clock generation. The bit clock is the product of sample rate, bits per sample, and number of channel.
- Wide variety of I2S and similar bitstream format
- Transmit section supports a wide variety of I2S and similar bitstream formats.
- Receive section supports a wide variety of I2S and similar bitstream formats.
- The transmit and receive sections are programmable to the following:
  - Clock and frame-sync polarity (rising or falling edge)
  - Word length (bits per word): 16 and 24 bits

Figure 8-8 shows the McASP block diagram.

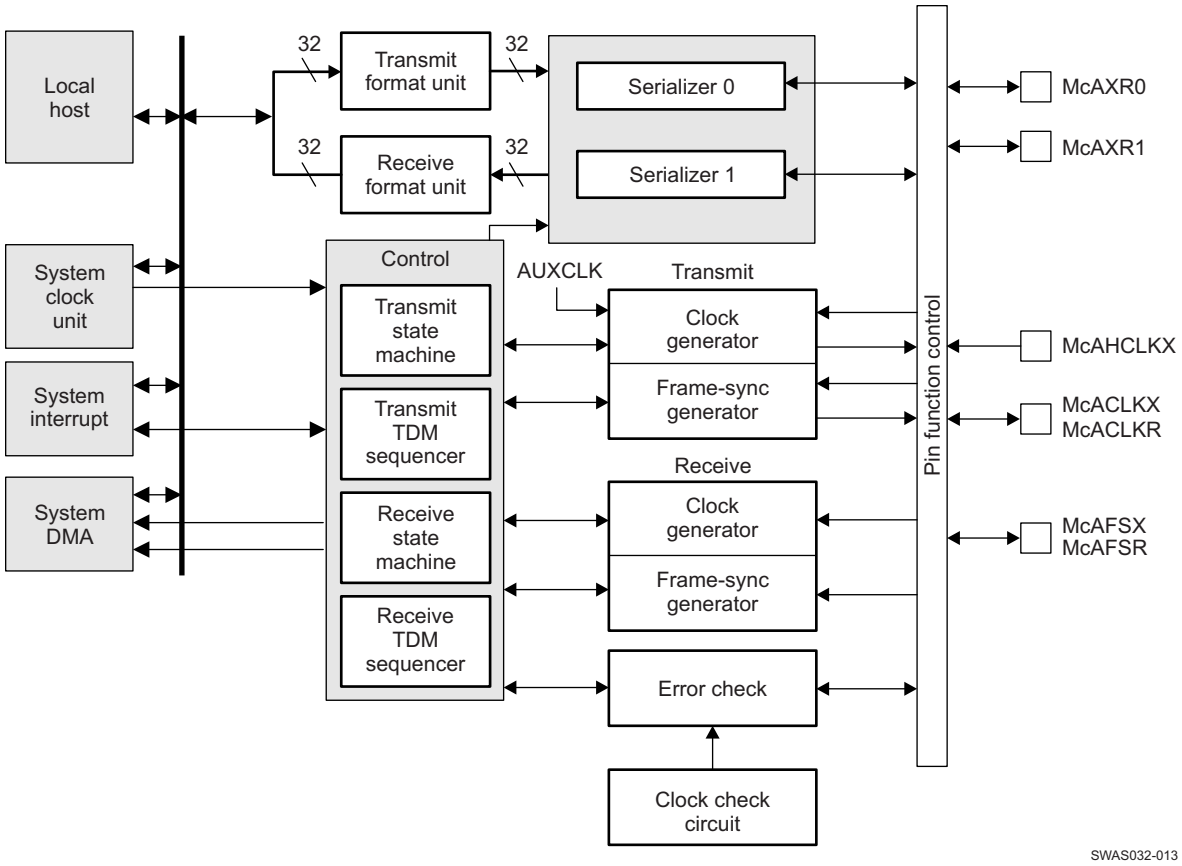


Figure 8-8. McASP Block Diagram

The McASP has independent receive and transmit clock generators and frame sync generators, error-checking logic, and two serial data pins. The McASP includes the following pins:

- Serializers: Data pins AXR[n]
- Transmit clock generator
  - AHCLKX: McASP transmit high-frequency master clock (input)
  - ACLKX: McASP transmit bit clock (input or output)
- Transmit frame-sync generator: AFSX: McASP transmit frame-sync or left and right clock (input or output)
- Receive clock generator: ACLKR: McASP receive bit clock (input)
- Receive frame-sync generator: Receive frame-sync generator AFSR (input)

PRODUCT PREVIEW

8.5.1 System Level Connection

Figure 8-9 shows the McASP using a digital audio decoder system.

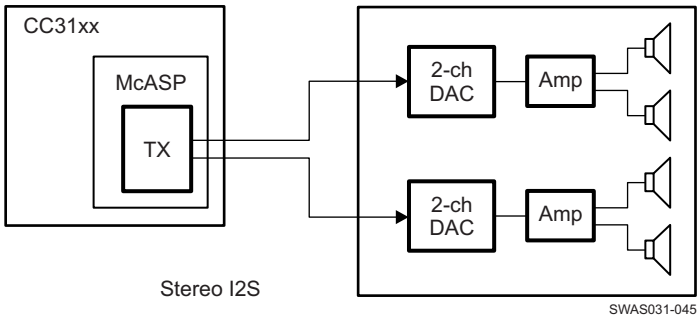


Figure 8-9. McASP With 2 Parallel Channel DAC

8.5.2 I2S Format

The I2S format is used extensively in audio interfaces. The TDM transfer mode of the McASP supports the I2S format when configured to two slots per frame. The I2S format is specifically designed to transfer a stereo channel (left and right) over a single data pin. Slots are also commonly referred to as channels. The frame-width duration in the I2S format is the same as the slot size. The frame signal is also referred to as word select in the I2S format.

The McASP supports transfer of two stereo channels over two data pins.

8.6 Fast Parallel Input

The fast parallel interface interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The parallel interface supports 8 bits.

Figure 8-10 shows the parallel port block diagram.

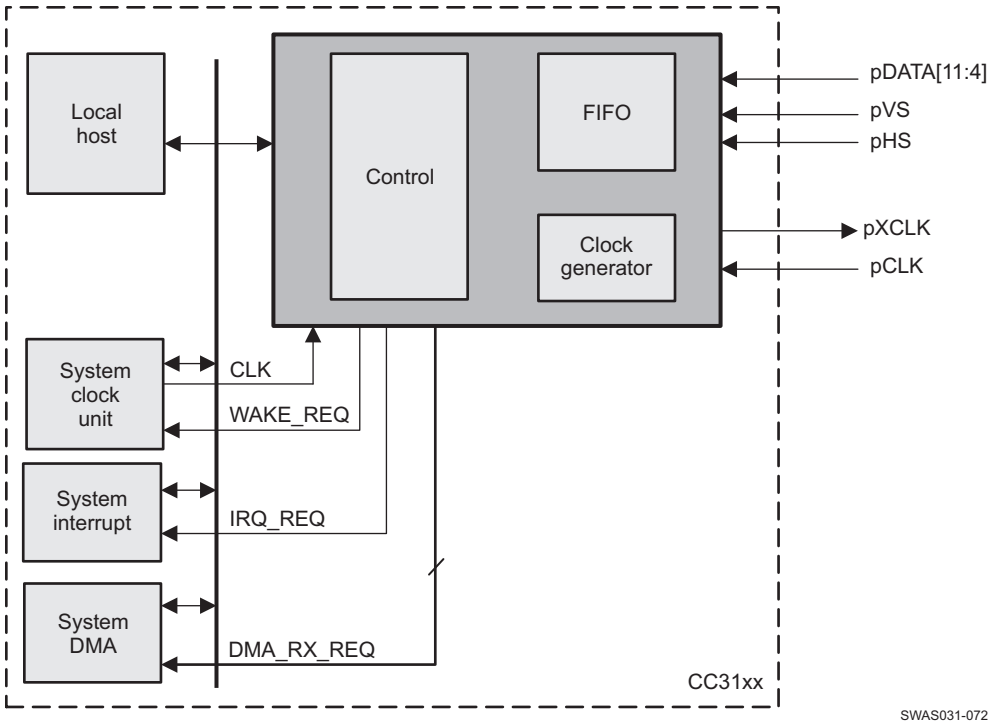


Figure 8-10. Parallel Port Block Diagram

The pixel data is presented on pDATA one pixel for every pCLK rising edge or falling depending on the polarity configuration. There are additional pixel times between rows that represent a blanking period. The active pixels are identified by a combination of two additional timing signals: horizontal synchronization (pHS) and vertical synchronization (pVS). During the image sensor readout, these signals define when a row of valid data begins and ends and when a frame starts and ends.

Figure 8-11 shows how the storage of image data in the FIFO depends on the order setting.

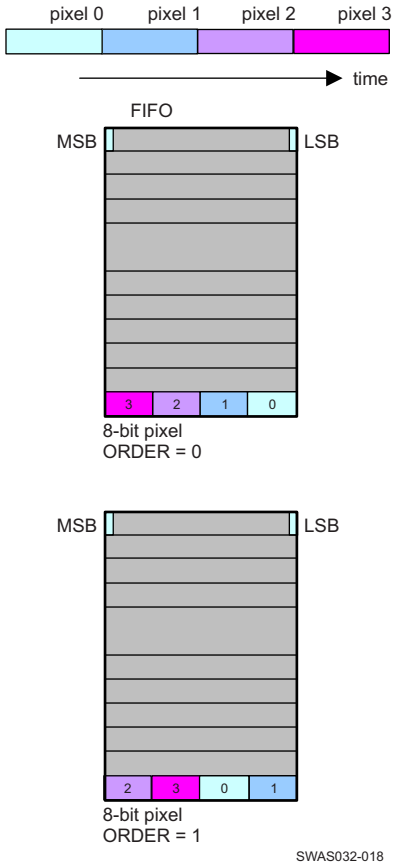


Figure 8-11. Parallel Port Data Storage

8.7 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. The TAP, instruction register (IR), and data registers (DRs) can be used to test the interconnections of assembled printed circuit boards and obtain manufacturing information on the components. The JTAG port also provides a means of accessing and controlling design-for-test features such as I/O pin observation and control, scan testing, and debugging. The JTAG port is comprised of four pins:

- TCK
- TMS
- TDI
- TDO

Data is transmitted serially into the controller on TDI and out of the controller on TDO. The interpretation of this data is dependent on the current state of the TAP controller. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1-Test Access Port and Boundary-Scan Architecture.

PRODUCT PREVIEW

8.8 Analog-to-Digital Converter (ADC)

The ADC peripheral converts a continuous analog voltage to a discrete digital number. The CC3101R device includes ADC modules with four input channels. Each ADC module features 12-bit conversion resolution for the four input channels.

Figure 8-12 shows a block diagram of the ADC module.

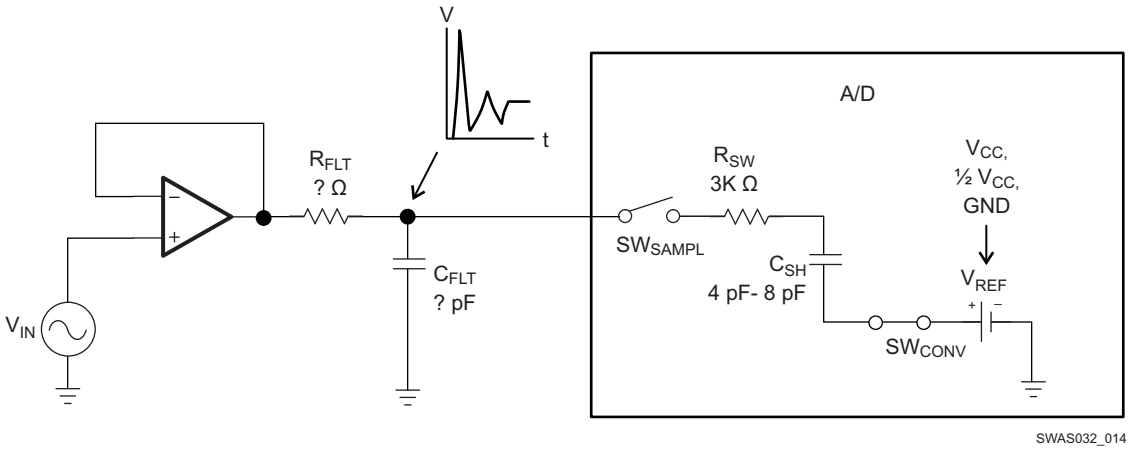


Figure 8-12. ADC Module

The CC3101R microcontroller features include:

- 12-bit ADC
- Four analog input channels
- Sampling rate of 16 µs per channel
- DMA interface to transfer data to the application RAM: Dedicated channel for each channel
- Power and ground for the analog circuitry separate from the digital power and ground

PRODUCT PREVIEW

9 Timing Specifications

This section describes the interface timing requirements for the peripherals.

9.1 SPI

9.1.1 SPI Master

Figure 9-1 shows the timing diagram for the SPI master.

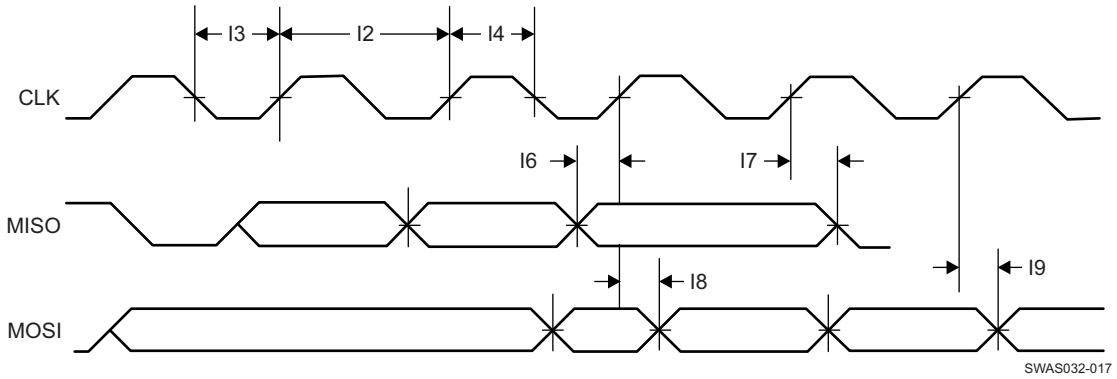


Figure 9-1. SPI Master Timing Diagram

Table 9-1 lists the timing parameters for the SPI master.

Table 9-1. SPI Master Timing Parameters

Parameter Number	Parameter[1]	Parameter Name	Min	Max	Unit
I1	F	Clock frequency		20	MHz
I2	Tclk	Clock period	25		ns
I3	tLP	Clock low period		12.5	ns
I4	tHT	Clock high period		12.5	ns
I5	D	Duty cycle	45	55	%
I6	tIS	RX data setup time	1		ns
I7	tIH	RX data hold time	2		ns
I8	tOD	TX data output delay		8.5	ns
I9	tOH	TX data hold time		8	ns

(1) Timing parameter has a maximum load of 20 pf.

PRODUCT PREVIEW

9.1.2 SPI Slave

Figure 9-2 shows the timing diagram for the SPI slave.

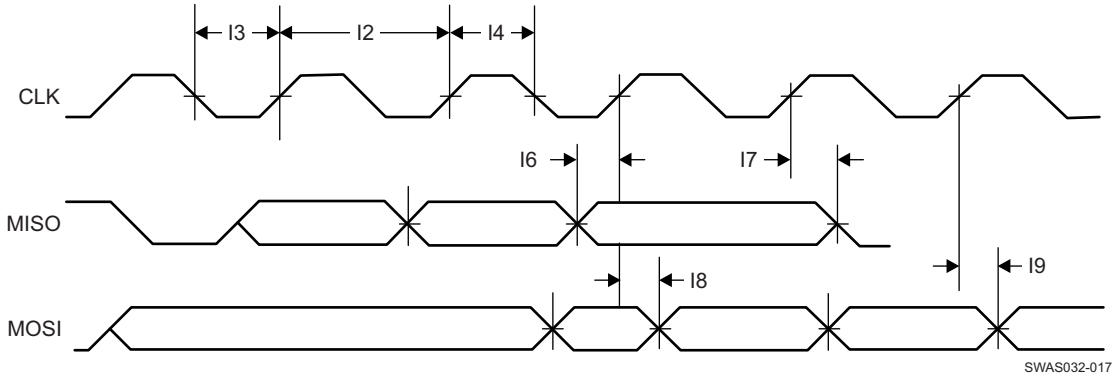


Figure 9-2. SPI Slave Timing Diagram

Table 9-2 lists the timing parameters for the SPI slave.

Table 9-2. SPI Slave Timing Parameters

Parameter Number	Parameter(1)	Parameter Name	Min	Max	Unit
I1	F	Clock frequency		20	MHz
I2	Tclk	Clock period	25		ns
I3	tLP	Clock low period		12.5	ns
I4	tHT	Clock high period		12.5	ns
I5	D	Duty cycle	45	55	%
I6	tIS	RX data setup time	4		ns
I7	tIH	RX data hold time	4		ns
I8	tOD	TX data output delay		20	
I9	tOH	TX data hold time		24	ns

(1) Timing parameter has a maximum load of 20 pf at 3.3 V.

9.2 McASP

9.2.1 I2S Transmit Mode

Figure 9-3 shows the timing diagram for the I2S transmit mode.

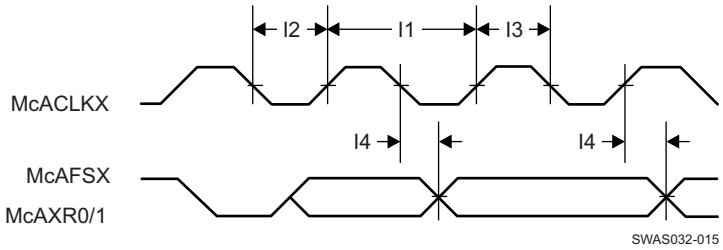


Figure 9-3. I2S Transmit Mode Timing Diagram

Table 9-3 lists the timing parameters for the I2S transmit mode.

Table 9-3. I2S Transmit Mode Timing Parameters

Parameter Number	Parameter(1)	Parameter Name	Min	Max	Unit
I1	fclk	Clock frequency		9.216	MHz
I2	tLP	Clock low period		1/2 fclk	ns
I3	tHT	Clock high period		1/2 fclk	ns
I4	tOH	TX data output delay		22	ns

(1) Timing parameter has a maximum load of 20 pf.

9.2.2 I2S Receive Mode

Figure 9-4 shows the timing diagram for the I2S receive mode.

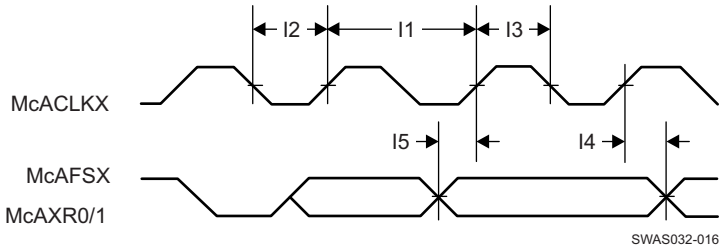


Figure 9-4. I2S Receive Mode Timing Diagram

Table 9-4 lists the timing parameters for the I2S receive mode.

Table 9-4. I2S Receive Mode Timing Parameters

Parameter Number	Parameter(1)	Parameter Name	Min	Max	Unit
I1	fclk	Clock frequency		9.216	MHz
I2	tLP	Clock low period		1/2 fclk	ns
I3	tHT	Clock high period		1/2 fclk	ns
I4	tOH	RX data hold time		0	ns
I5	tOS	RX data setup time		15	ns

(1) Timing parameter has a maximum load of 20 pf.

9.3 GPIO

Figure 9-5 shows the GPIO timing diagram.

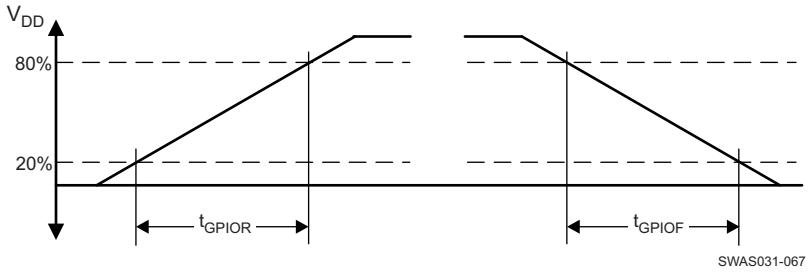


Figure 9-5. GPIO Timing

PRODUCT PREVIEW

Table 9-5 lists the GPIO timing parameters.

Table 9-5. GPIO Timing Parameters

Parameter	Parameter Name	Condition	Min	Max	Unit
t_{GPIOR}	GPIO rise time from 20% to 80 % of VDD	2-mA drive	TBD	TBD	ns
		4-mA drive	TBD	TBD	ns
		6-mA drive	TBD	TBD	ns
t_{GPIOF}	GPIO fall time from 80% to 20 % of VDD	2-mA drive	TBD	TBD	ns
		4-mA drive	TBD	TBD	ns
		6-mA drive	TBD	TBD	ns

9.4 I²C

Figure 9-6 shows the I²C timing diagram.

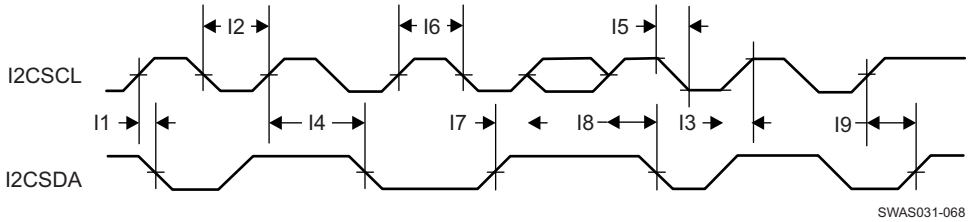


Figure 9-6. I²C Timing

Table 9-6 lists the ²C timing parameters.

Table 9-6. I²C Timing Parameters (1)

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
I2	tLP	Clock low period	See (2).	-	System clock
I3	tSRT	SCL/SDA rise time	–	See (3).	ns
I4	tDH	Data hold time	NA	–	
I5	tSFT	SCL/SDA fall time	–	3	ns
I6	tHT	Clock high time	See (2).	–	System clock
I7	tDS	Data setup time	tLP/2		System clock
I8	tSCSR	START condition setup time	36	–	System clock
I9	tSCS	STOP condition setup time	24	–	System clock

(1) All timing is with 8-mA drive and 20-pf load.
(2) This value depends on the value programmed in the clock period register of I²C. Maximum output frequency is the result of the minimal value programmed in this register.
(3) Because I²C is an open-drain interface, the controller can drive logic 0 only. Logic is the result of external pullup. Rise time depends on the external signal capacitance and external pull-up register value.

PRODUCT PREVIEW

9.5 IEEE 1149.1 JTAG

Figure 9-7 shows the JTAG timing diagram.

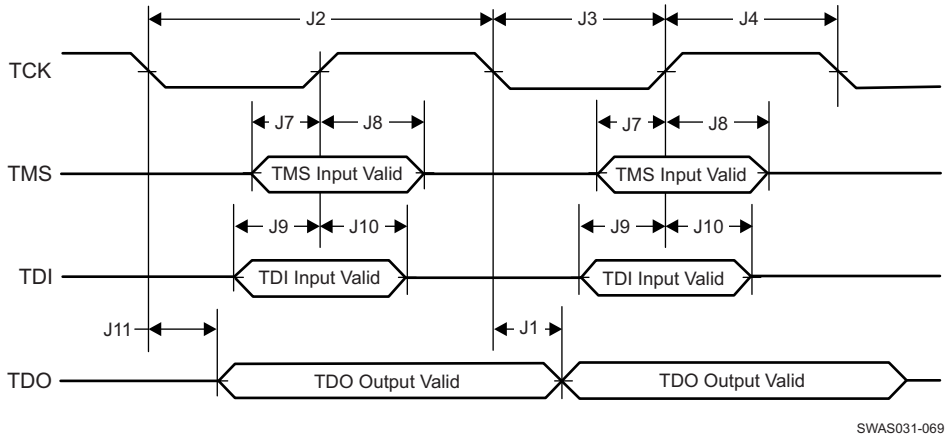


Figure 9-7. JTAG Timing

Table 9-7 lists the JTAG timing parameters.

Table 9-7. JTAG Timing Parameters

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
J1	fTCK	Clock frequency		15	MHz
J2	tTCK	Clock period		1/fTCK	ns
J3	tCL	Clock low period		tTCK/2	ns
J4	tCH	Clock high period		tTCK/2	ns
J7	tTMS_SU	TMS setup time	1		
J8	tTMS_HO	TMS hold time	16		
J9	tTDI_SU	TDI setup time	1		
J10	tTDI_HO	TDI hold time	16		
J11	tTDO_HO	TDO hold time		15	

9.6 ADC

Table 9-8 lists the ADC electrical specifications.

Table 9-8. ADC Electrical Specifications

Parameter	Description	Condition and Assumptions	Min	Typ	Max	Unit
Nbits	Number of bits	2n = number of levels of resolution		12		Bits
INL	Integral nonlinearity	Worst-case deviation from histogram method over full scale (not including first and last three LSB levels)	–1.5		2.0	LSB
DNL	Differential nonlinearity	Worst-case deviation of any step from ideal	–0.9		0.8	LSB
VREFP	Positive voltage reference(1)	VREFP = VDDA_1P8V		1.465		V
VREFN	Negative voltage reference VREFP	VREFN = VSSA		0		V
FCLK	Clock rate	Successive approximation input clock rate		10		MHz

(1) External reference not supported

PRODUCT PREVIEW

Table 9-8. ADC Electrical Specifications (continued)

Parameter	Description	Condition and Assumptions	Min	Typ	Max	Unit
Fsample	Throughput rate of ADC			0.5		MSPS
Number of channels				4 (2)		
Channel throughput				62.5		KSPS
Finput	The input signal frequency			300		Hz
STND	Signal-to-noise and distortion	Input frequency 300 Hz at FCLK and 20mVpp-1.4Vpp sine wave input		60		dB
Isupply-act	Active supply current	Average for analog-to-digital during conversion without reference current		1.5		mA
Isupply-pd VDDA	Power-down supply current for core supply	Total for analog-to-digital when not active (this must be the SoC level test)		1		µA
E0	Offset Error	FCLK = 10 MHz			6 (3)	LSB

(2) Channel 1 and channel 3 has degraded performance compared to channel 0 and channel 2. Details of channel degradation will be provided in a future revision.
(3) TI recommends using the ADC API functions, which automatically compensate for offset error.

9.7 Parallel Port

Figure 9-8 shows the timing diagram for the parallel port.

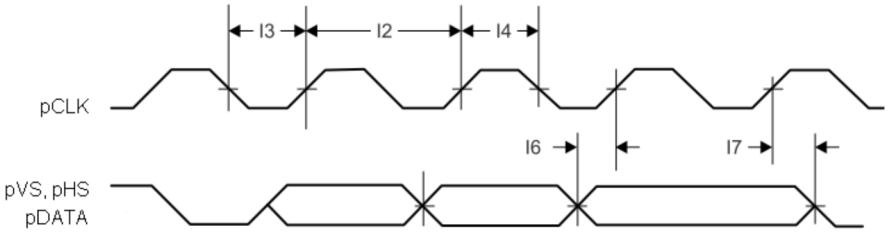


Figure 9-8. Parallel Port Timing Diagram

Table 9-9 lists the timing parameters for the parallel port.

Table 9-9. Parallel Port Timing Parameters

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
I1	F	Clock frequency		2	MHz
I2	T_{clk}	Clock period		1/F	ns
I3	t_{LP}	Clock low period		$T_{clk}/2$	ns
I4	t_{HT}	Clock high period		$T_{clk}/2$	ns
I7	D	Duty cycle		45 to 55	%
I8	t_{IS}	RX data setup time		2	ns
I9	t_{IH}	RX data hold time		2	ns

PRODUCT PREVIEW

10 Power Management and Clock Requirements

The CC3101R device supports the following modes of operation:

- VBAT/wide voltage mode (2.1 to 3.6 V)
- Preregulated 1.8-V mode

10.1 Input Supply Range

Table 10-1 through Table 10-2 list the supply ranges for various configurations in the CC3101R device.

Table 10-1. VBAT/Wide Voltage Range

Min	Nom	Max	Unit
2.1	3.3	3.6	V

Table 10-2. Preregulated 1.8-V Range

Min	Nom	Max	Unit
1.76	1.8	1.98	V

10.2 Power Management Architecture

The CC3101R power management has DC-DC to cater to the differing voltage or current requirements of the product.

- Digital DC-DC
  - Input: VBAT/wide voltage (2.1 to 3.6 V) or preregulated 1.8 V
- ANA1 DC-DC
  - Input: VBAT/wide voltage (2.1 to 3.6 V)
  - In regulated 1.8-V mode, ANA1 DC-DC is bypassed.
- PA DC-DC
  - Input: VBAT/wide voltage (2.1 to 3.6 V)
  - In regulated 1.8-V mode, PA DC-DC is bypassed.
- ANA2 DC-DC
  - Input: VBAT/wide voltage (2.1 to 3.6 V) or preregulated 1.8 V
  - Output: 3.3 V regulated (for use in restricted condition; for more information, contact TI)

In regulated 1.8-V mode, ANA1 DC-DC and PA DC-DC are bypassed. The CC3101R device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC-DC converters and LDOs, generate all of the voltages required for the device to operate from a wide variety of input sources. For maximum flexibility, the device can operate in the modes described in the following sections.

10.2.1 VBAT/Wide Voltage Connection

In the wide voltage battery connection, the device is powered directly from the battery or preregulated 3.3-V supply (see Figure 10-1). All other required voltages for operation of the device, including 3.3 and 1.8 V, are generated internally by the DC-DC converters. This scheme is the most common mode for the device as it supports wide voltage operation from 2.1 to 3.6 V.

PRODUCT PREVIEW

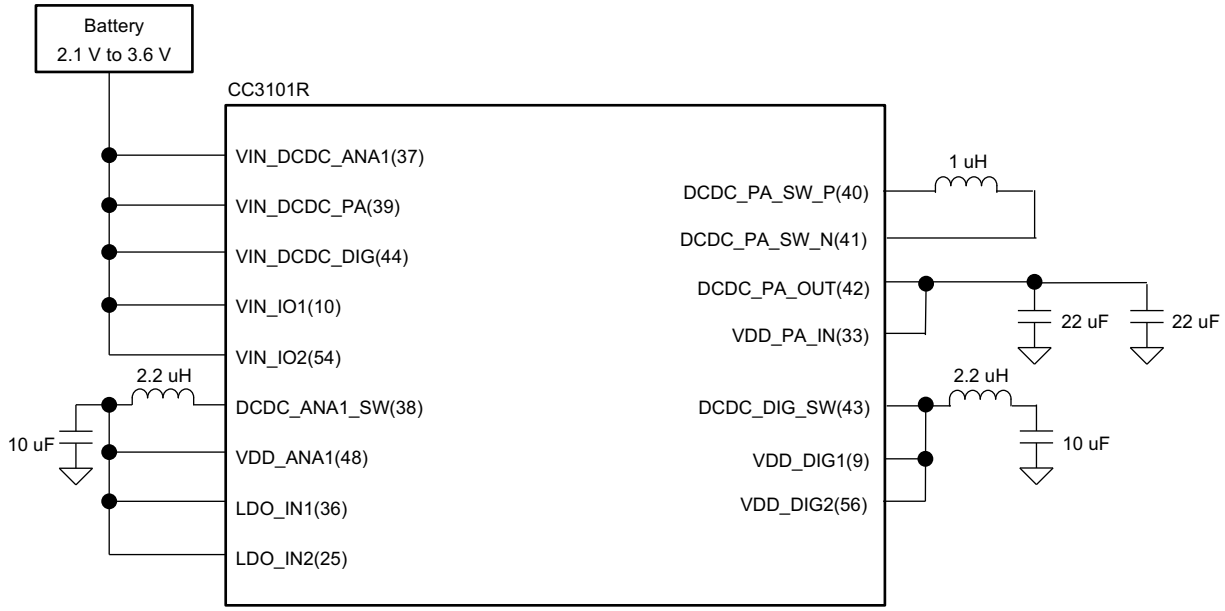


Figure 10-1. VBAT/Wide Voltage Connection

10.2.2 Preregulated 1.8 V

The preregulated 1.8-V mode of operation applies an external regulated 1.8 V directly at the VDD_ANA1 (48) pin of the device. The VBAT and the VDDIO are also connected to the 1.8 V supply. This mode provides the lowest BOM count version in which an inductor (2.2 µH) and a capacitor (10 µF) can be avoided.

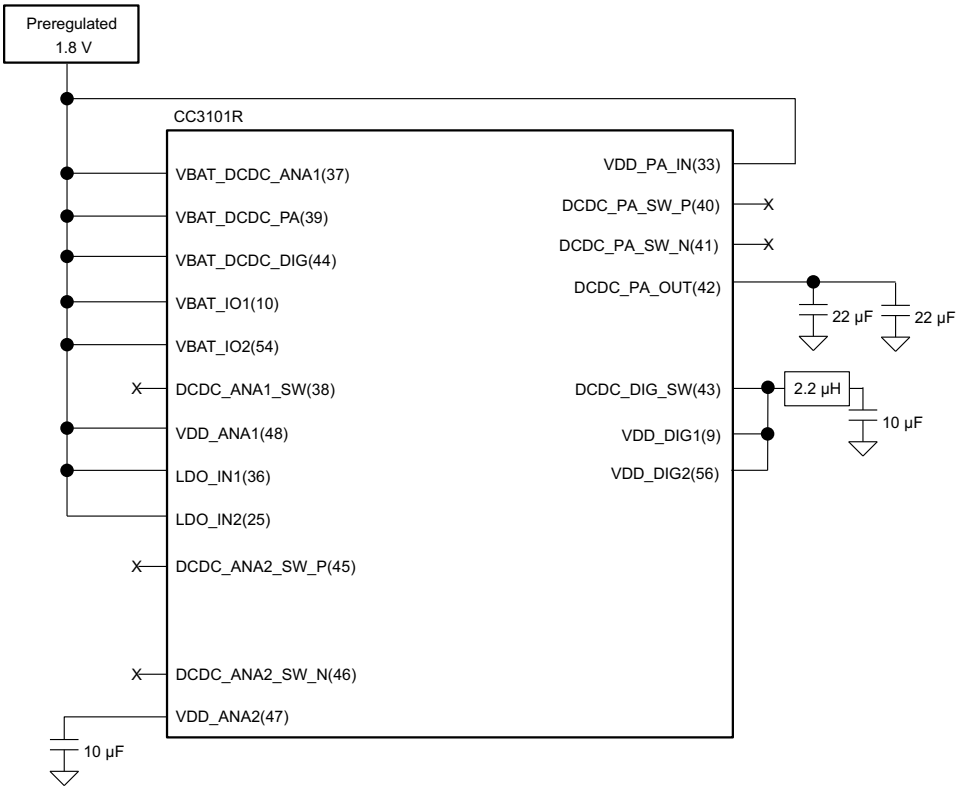


Figure 10-2. Preregulated 1.8 V Block Diagram

10.3 Low-Power Operating Mode

From a power management perspective, the CC3101R device is composed of the following two independent subsystems:

- Cortex M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Cortex M4 application processor runs the user application loaded from an external serial flash. The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem and can be in one of the five modes described in Table 10-3.

NOTE

Table 10-3 lists the modes by power consumption, with highest power modes listed first.

Table 10-3. User Program Modes

Application Processor (MCU) Mode	Description
MCU active mode	MCU executing code at 80-MHz state rate
MCU sleep mode	The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.
MCU deep sleep mode	The internal MCU core supply lowers to 1.1 V, the entire state of the MCU is preserved, and state information is not lost. The MCU can wake up from external events or by using an internal timer. (The wake-up time is approximately 100 µs.) Certain parts of memory can be switched off while the MCU is in deep-sleep mode to conserve the current and extend device life. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.
MCU LPDS mode	The internal core supply lowers to 0.9 V, state information is lost, and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is about 10 ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on a GPIO (GPIO0–GPIO6).
MCU hibernate mode	The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The real-time clock (RTC) clock keeps running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 60 ms. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO (GPIO0–GPIO6).

Table 10-4 describes the six modes of the networking subsystem.

Table 10-4. Networking Subsystem Modes

Network Processor Mode	Description
Network active mode processing layer 3, 2, and 1	Transmitting or receiving IP protocol packets
Network active mode (processing layer 2 and 1)	Transmitting or receiving MAC management frames; IP processing not required.
Network active listen mode	Special power optimized active mode for receiving beacon frames (no other frames supported)
Network connected Idle	A composite mode that implements 802.11 infrastructure power save operation. The CC3101R network processor automatically goes into LPDS mode between beacons and then wakes to active listen mode to receive a beacon and determine if there is pending traffic at the access point. If not, the network processor returns to LPDS mode and the cycle repeats.
Network LPDS mode	Low-power state between beacons in which the state is retained by the network processor, allowing for a rapid wake up.
Network disabled	

The operation of the application and network processor ensures that the CC3101R device remains in the lowest power mode most of the time to preserve battery life. Table 10-5 summarizes the important CC3101R chip-level power modes.

Table 10-5. Important Chip-Level Power Modes

Power States for Applications MCU and Network Processor	Network Processor Active Mode (Transmit, Receive, or Listen)	Network Processor LPDS Mode	Network Processor Disabled
MCU active mode	Chip = active (C)	Chip = active	Chip = active
MCU LPDS mode	Chip = active (A)	Chip = LPDS (B)	Chip = LPDS
MCU hibernate mode	Not supported because chip is hibernated by MCU; thus, network processor cannot be in active mode	Not supported because chip is hibernated by MCU; thus, network processor cannot be in LPDS mode	Chip = hibernate (D)

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power save mode but sends and receives little data spends most of the time in Connected idle, which is a composite of modes A (receiving a beacon frame) and B (waiting for the next beacon).
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data spends most of the time in mode D (hibernated), jumping briefly to mode C (active) to transmit data.

10.4 Clock Requirement

The CC3101R device requires two separate clocks for its operation:

- A slow clock running at 32.768 kHz is used for the RTC.
- A fast clock running at 40 MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators, which enables the use of cheaper crystals instead of dedicated TCXOs for these clocks. The RTC can also be fed externally to provide re-use of an existing clock on the system to save on overall cost.

10.4.1 Slow Clock Using Internal Oscillator

The slow clock is a free-running clock supplied using the RTC crystal connected on the device. The accuracy of the slow clock frequency must be 32.768 kHz ±150 ppm. In this mode of operation, the crystal is tied between the RTC_XTAL_P (51) and RTC_XTAL_N (51) pins of the device with a suitable load capacitance.

Figure 10-3 shows the crystal connections for the slow clock.

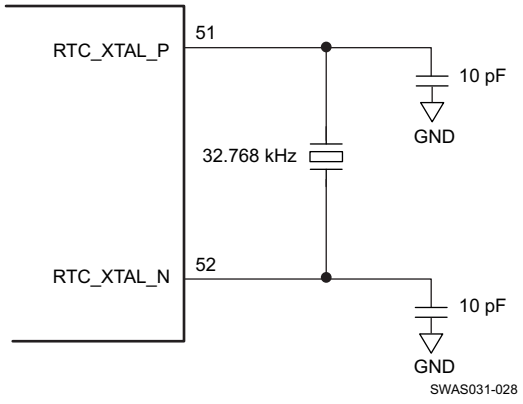


Figure 10-3. RTC Crystal Connections

10.4.2 Slow Clock Using External Clock

When an RTC clock oscillator is present in the system, the CC3101R device can accepts this clock directly as an input. The clock is fed on the RTC_XTAL_P line and the RTC_XTAL_N line is held to VDDIO. The clock must be a CMOS-level clock compatible with the VDDIO fed to the device.

Figure 10-4 shows the external RTC clock input connection.

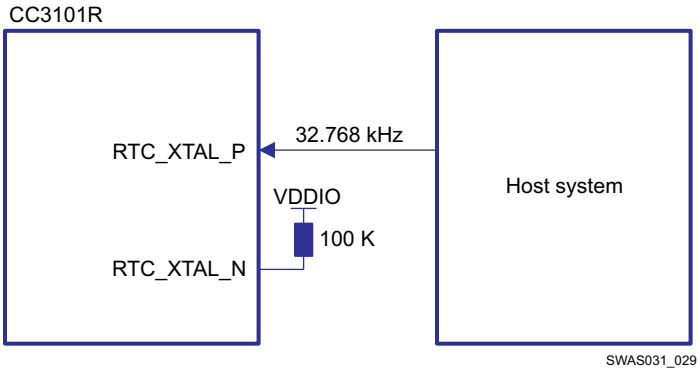


Figure 10-4. External RTC Clock Input

10.4.3 Fast Clock (Fref) Using an External Crystal

The CC3101R device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The XTAL is fed directly between the WLAN_XTAL_P (23) and WLAN_XTAL_N (22) pins of the device with suitable loading capacitors.

Figure 10-5 shows the fast clock crystal connections.

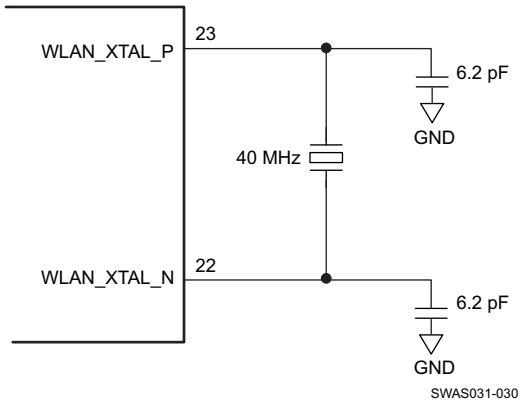


Figure 10-5. Fast Clock Crystal Connections

10.4.4 Fast Clock (FREF) Using External Oscillator

The CC3101R device can accept an external TCXO/XO for the 40-MHz clock. In this mode of operation, the clock is connected to the WLAN_XTAL_P. The WLAN_XTAL_N pin is connected to the I/O power supply. The external TCXO/XO can be enabled by the TCXO_EN pin from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

Figure 10-6 shows the connection.

PRODUCT PREVIEW

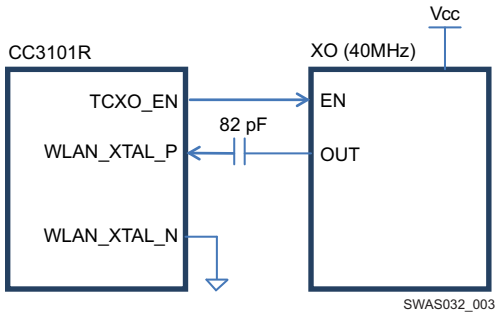


Figure 10-6. External TCXO Input

Table 10-6 lists the external FREF clock requirements.

Table 10-6. External FREF Clock Requirements (–40°C to +85°C)

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Frequency				40.00		MHz
Frequency accuracy (Initial + temp + aging)					±20	ppm
Input transition time T_r,T_f -10% to 90%		T_r,T_f			TBD	nS
Frequency input duty cycle			TBD	50	TBD	%
Clock voltage limits	Sine or /clipped sine wave, AC coupled	Vpp	TBD		TBD	V
Phase noise @ 40 MHz	@ 1 KHz				–125	dBc/Hz
	@ 10 KHz				–142	dBc/Hz
	@ 100 KHz				–145	dBc/Hz

PRODUCT PREVIEW

11 Specifications

This section describes the interface timing requirements for the peripherals.

11.1 Chip Requirements and Operation

11.2 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

Parameters	Pins	Min	Max	Unit
VBAT and VIO	37, 39, 44	–0.5	+3.8	V
VIO-VBAT (differential)	10, 54		0.0	V
Digital inputs		–0.5	VIO+0.5	V
RF pins			TBD	V
Analog pins (XTAL)			TBD	V
Operating ambient temperature range		–40	+85	°C
Storage temperature range	–	–40	+125	°C

11.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

Parameter	Pins	Conditions	Min	Typ	Max	Unit
Operating ambient temperature			–30	25	+85	°C
VBAT	39, 37, 44	Direct battery connection	2.1	3.3	3.6	V
VIO	10, 54		2.1	3.3	3.6	V
VBAT	39, 37, 44	Preregulated 3.3 V	3.0	3.3	3.6	V
VIO	10, 54		3.0	3.3	3.6	V
VBAT	39, 37, 44	Preregulated 1.8 V	1.76	1.8	1.98	V
VIO	10, 54		1.98	1.8	3.6	V

(1) Operating temperature is limited by crystal frequency variation.

11.4 Current Consumption

VBAT = 3.6 V

Parameter	Test Conditions	Typ	Max	Unit
802.11b TX	Po = 19 dBm Rate = 11 CCK Packet length = 2048 bytes Tdelay = 40 µs	280(1)		
802.11g TX	Po = 14.5 dBm Rate = 54 Mbps L = 2048 Tdelay = 40 µs	210(1)		
802.11bg RX	Rate = 54 Mbps	53(1)		mA
LPDS		85		µA
Hibernate		4		µA
MCU active and NWP in LPDS		TBD	TBD	mA
MCU in sleep state and NWP in LPDS		TBD	TBD	mA
MCU sleep and NWP active	NWP RX current with frames processed by the TCP IP stack (for example, large IP frames received)	TBD	TBD	

(1) Value applies to the MCU in LPDS mode. Add 5 mA if the MCU is in active mode.

PRODUCT PREVIEW

Current Consumption *(continued)*

VBAT = 3.6 V

Parameter	Test Conditions	Typ	Max	Unit
MCU sleep and NWP idle	RX current with frames not processed by the NWP TCP IP stack (for example, back-to-back MAC frames received)	TBD	TBD	
WLAN active	WLAN RX current in transceiver mode	TBD	TBD	mA

11.5 RTC Crystal Requirements

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Frequency				32.768		KHz
Frequency accuracy	Initial + temp + aging				±150	ppm
Crystal negative resistance	32.768 KHz, Cl = 10pF		TBD	TBD		Ω

11.6 External RTC Digital Clock Requirements

–40ºC to +85ºC

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Frequency				32768		Hz
Frequency accuracy (Initial + temp + aging)					±150	ppm
Input transition time T_r,T_f – 10% to 90%		T_r,T_f			100	nS
Frequency input duty cycle			20	50	80	%
Slow clock input voltage limits	Square wave, DC coupled	V_{ih}	0.65 × VDD_IO		VDD_IO	V
		V_{il}	0		0.35 × VDD_IO	V peak
Input impedance			1			MΩ
					5	pF

11.7 WLAN Fast Clock Crystal Requirements

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Frequency				40		MHz
Frequency accuracy	Initial + temp + aging				±20	ppm
Crystal negative resistance	40 MHz, Cl = 6.2 pF		TBD	TBD		Ω

11.8 WLAN RF Performance

PRODUCT PREVIEW

11.9 WLAN Receiver Characteristics

T_A = +25°C, V_{BAT} = 2.1 to 3.6 V. Parameters measured at SoC pin.

Parameter	Condition	Min	Typ	Max	Units
Sensitivity (10% PER)	1 DSSS		–96.5		dBm
	2 DSSS		–94.0		
	11 CCK		–88.0		
	6 OFDM		–90.0		
	9 OFDM		–89.0		
	18 OFDM		–86.0		
	36 OFDM		–80.5		
	54 OFDM		–74.0		
	MCS0 (GF)(1)		–89.0		
	MCS7 (GF)(1)		–71.0		
Maximum input level at 10% PER	802.11b		–4.0		
	802.11g		–10.0		

(1) Sensitivity for MM is 1-dB worse.

11.10 WLAN Transmitter Characteristics

T_A = +25°C, VBAT = 2.1 to 3.6 V. Parameters measured at SoC pin.

Parameter	Condition	Min	Typ	Max	Units
Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		19.5		dBm
	2 DSSS		19.5		
	11 CCK		19.0		
	6 OFDM		18.5		
	9 OFDM		18.5		
	18 OFDM		18.5		
	36 OFDM		16.5		
	54 OFDM		14.5		
	MCS7 (MM)		13.5		
Transmit center frequency accuracy		–20		20	ppm

PRODUCT PREVIEW

12 Reference Schematics

12.1 Reference Design for VBAT/Wide Voltage Connected Application

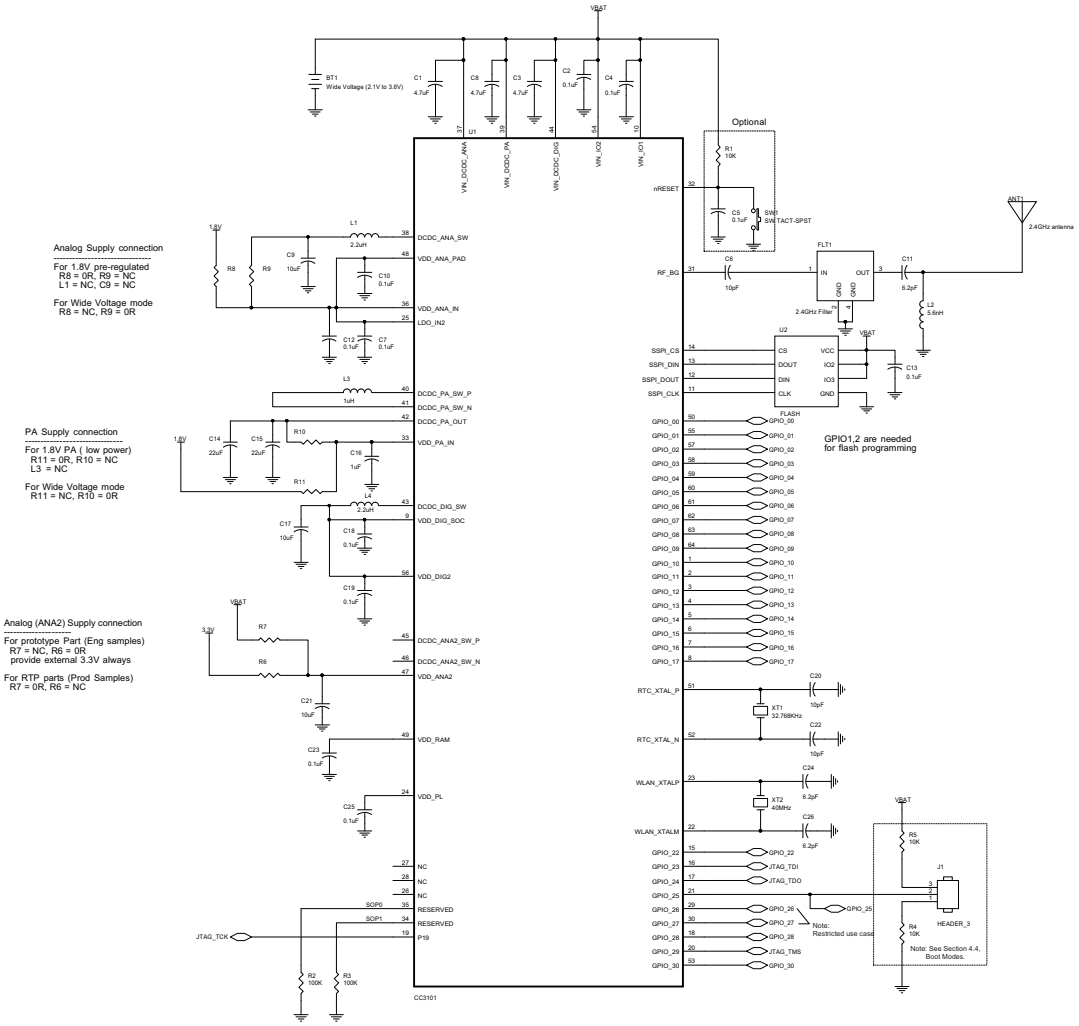


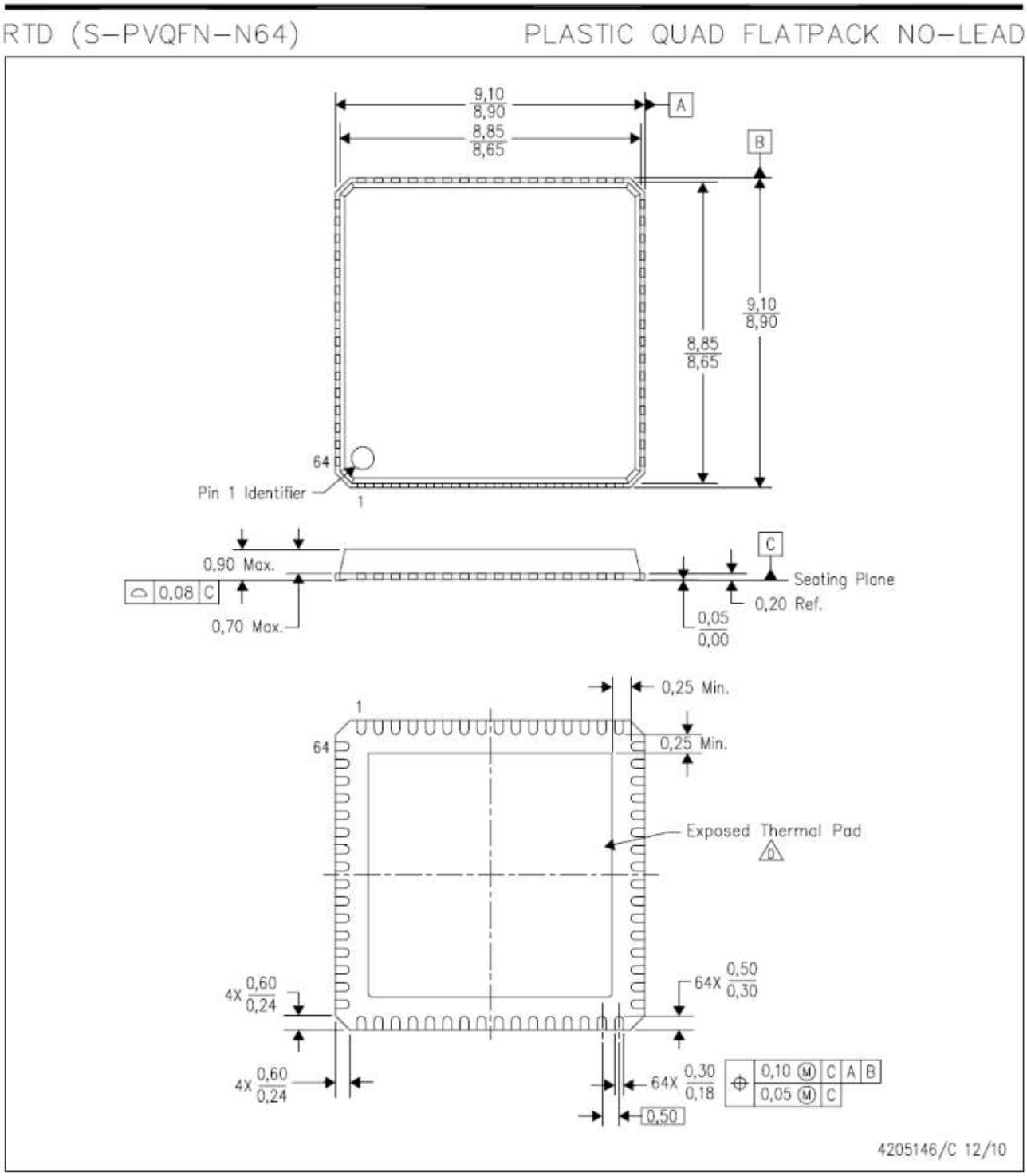
Figure 12-1. CC31001R Reference Schematics

PRODUCT PREVIEW

12.2 Bill of Materials

Item	Qty	Reference	Part	Manufacturer	Part Number	Description
1	1	ANT1	2.4-GHz antenna	Taiyo Yuden	AH316M245001-T	ANT *Bluetooth* W-LAN ZIGBEE WIMAX
2	3	C1,C3,C8	4.7 µF	Murata	GRM155R60J475ME47D	CAP CER 4.7 µF 6.3 V 20% X5R 0402
3	11	C2,C4,C5,C7,C10,C12,C13,C18,C19,C23,C25	0.1 µF	Taiyo Yuden	LMK105BJ104KV-F	CAP CER 0.1 µF 0402 X5R 10% 10V
4	3	C6,C20,C22	10 pF	Samsung	CL05C100JB5NNNC	CAP CER 10 pF 50 V 5% NP0 0402
5	3	C9,C17,C21	10 µF	Murata	GRM188R60J106ME47D	CAP CER 10 µF 6.3 V 20% X5R 0603
6	3	C11,C24,C26	6.2 pF	Murata	GRM1555C1H6R2BA01D	CAP CER 6.2 pF 50 V NP0 0402
7	2	C14,C15	22 µF	Murata	GRM188R60G226MEA0D	CAP CER 22 µF 4 V 20% X5R 0603
8	1	C16	1 µF	Taiyo Yuden	JMK105BJ105KV	CAP CER 1 µF 6.3 V 10% X5R 0402
9	1	FLT1	2.4-GHz filter	TDK-Epcos	DEA202450BT-1294B1-H	Filter Bandpass 2.45 GHZ WLAN SMD
10	2	L1,L4	2.2 µH	Murata	LQM2MPN2R2MG0	Ind 2.2 µH 0806 30% 1.2 A
11	1	L2	5.6 nH	Taiyo Yuden	HK10055N6S-T	Inductor Hifreq 5.6 ±0.3 nH 0402
12	1	L3	1 µH	Murata	LQM2HPN1R0MJ0L	Ind 1 µH 1008 20% 1.5 A
13	1	L5	10 µH	TDK	MLZ2012M100W	Ind, Multilayer 10 µH, 20% SMT, 0805
14	1	U1	CC3101	Texas Instruments	CC3101ZRTD	Wi-Fi Apps processor
15	1	U2	Flash	Winbond	W25Q80BLUXIG	IC flash 8 MB 50 MHz
16	1	XT1	32.768 kHz	Epson	Q13FC13500002	Crystal 32.768 kHz, 20 ppm, FC-135 SMD
17	1	XT2	40 MHz	Epson	Q24FA20H00396	Crystal 40 MHz 10 ppm, 8 pF , FA-20H, 2.5 x 2 mm SMD

13 Mechanical Information



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

SWAS031-017

PRODUCT PREVIEW

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