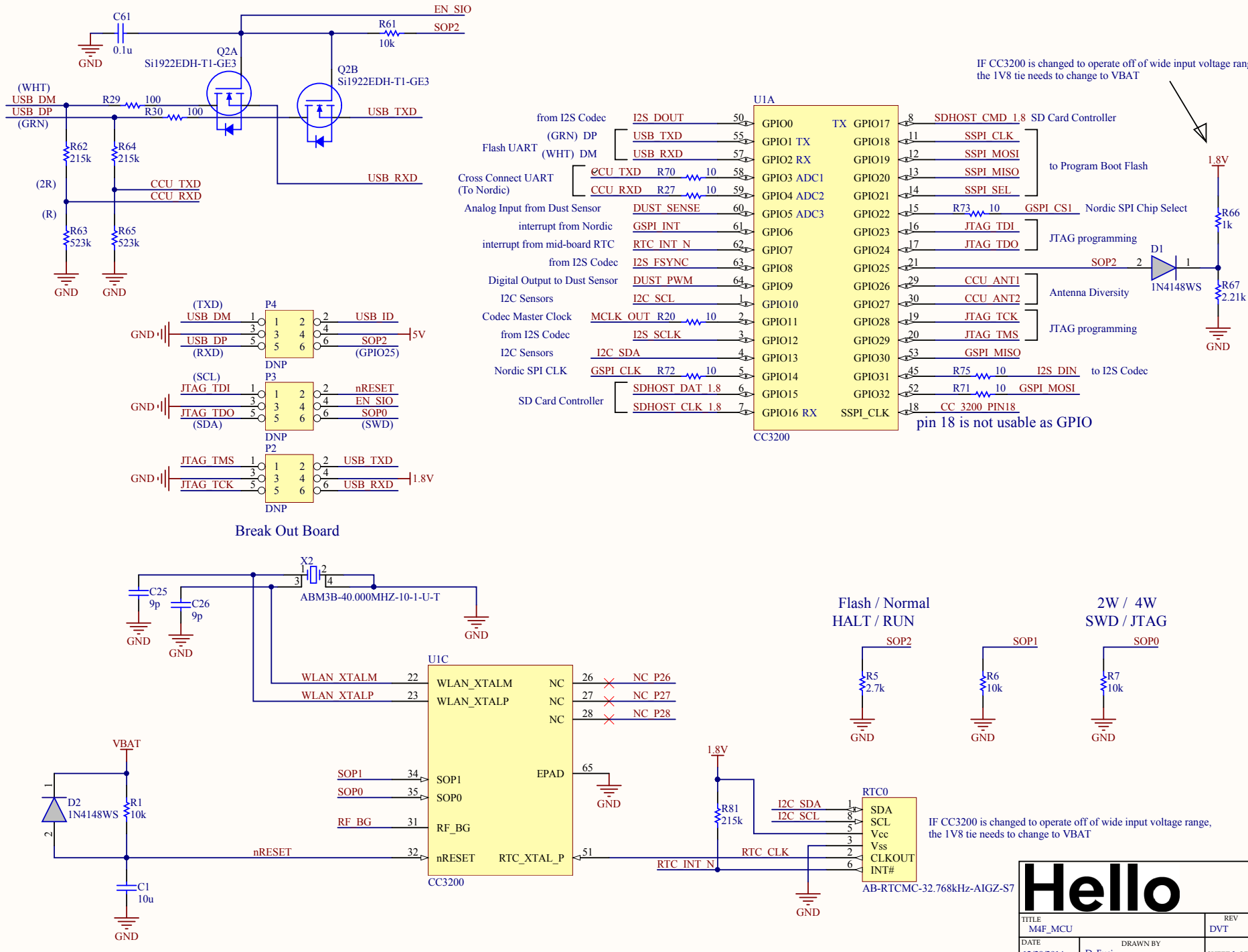
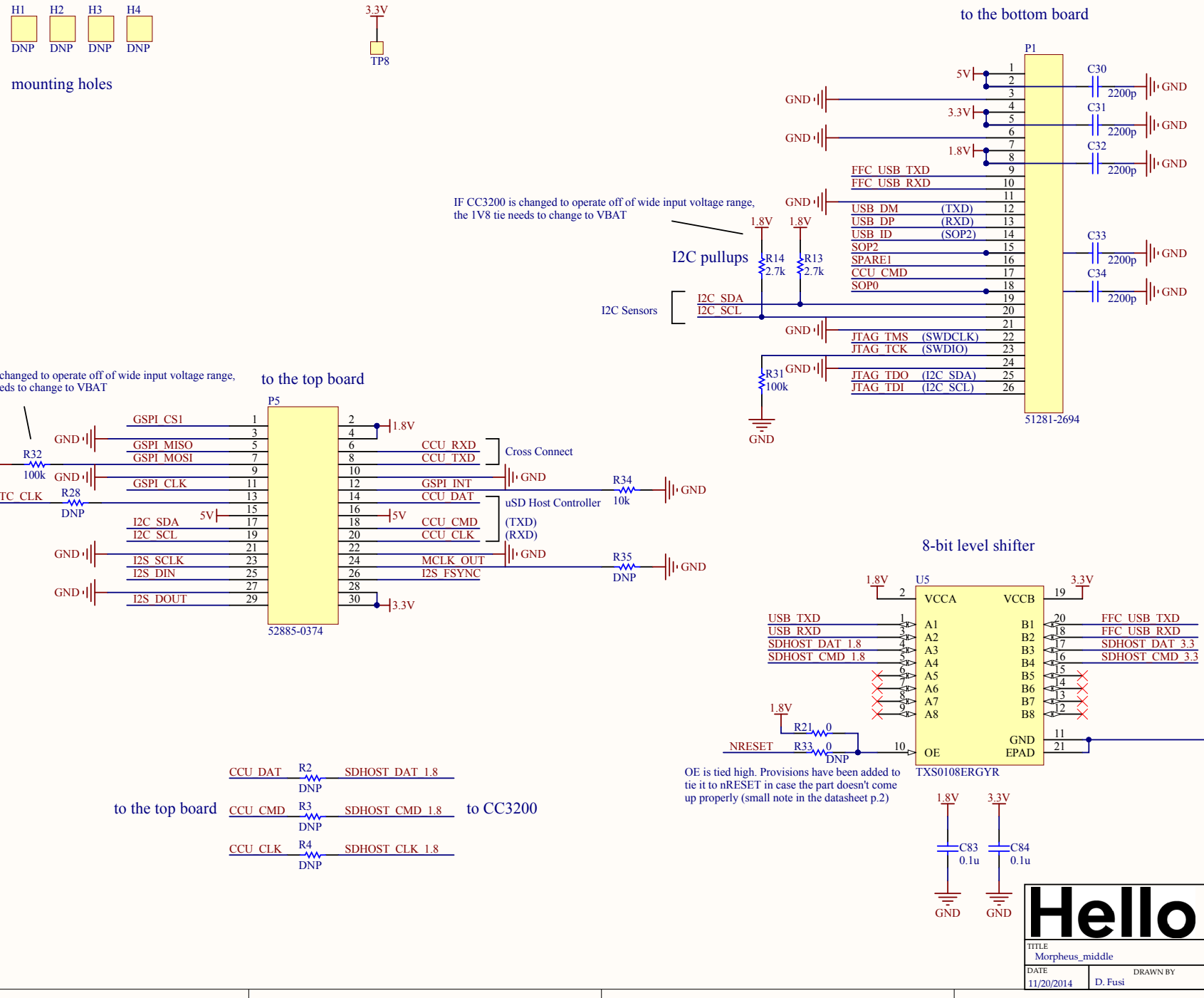
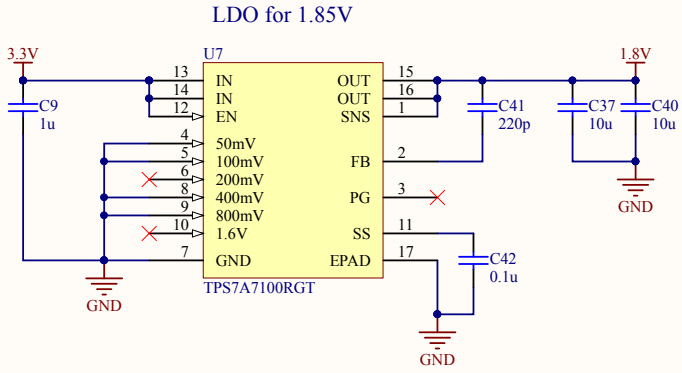
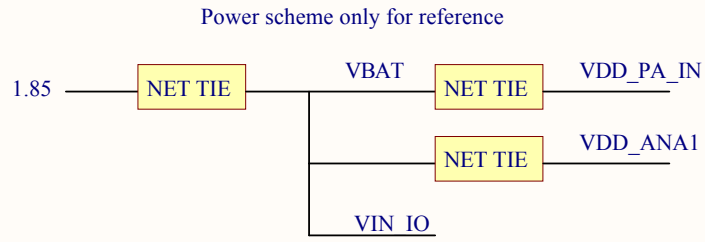
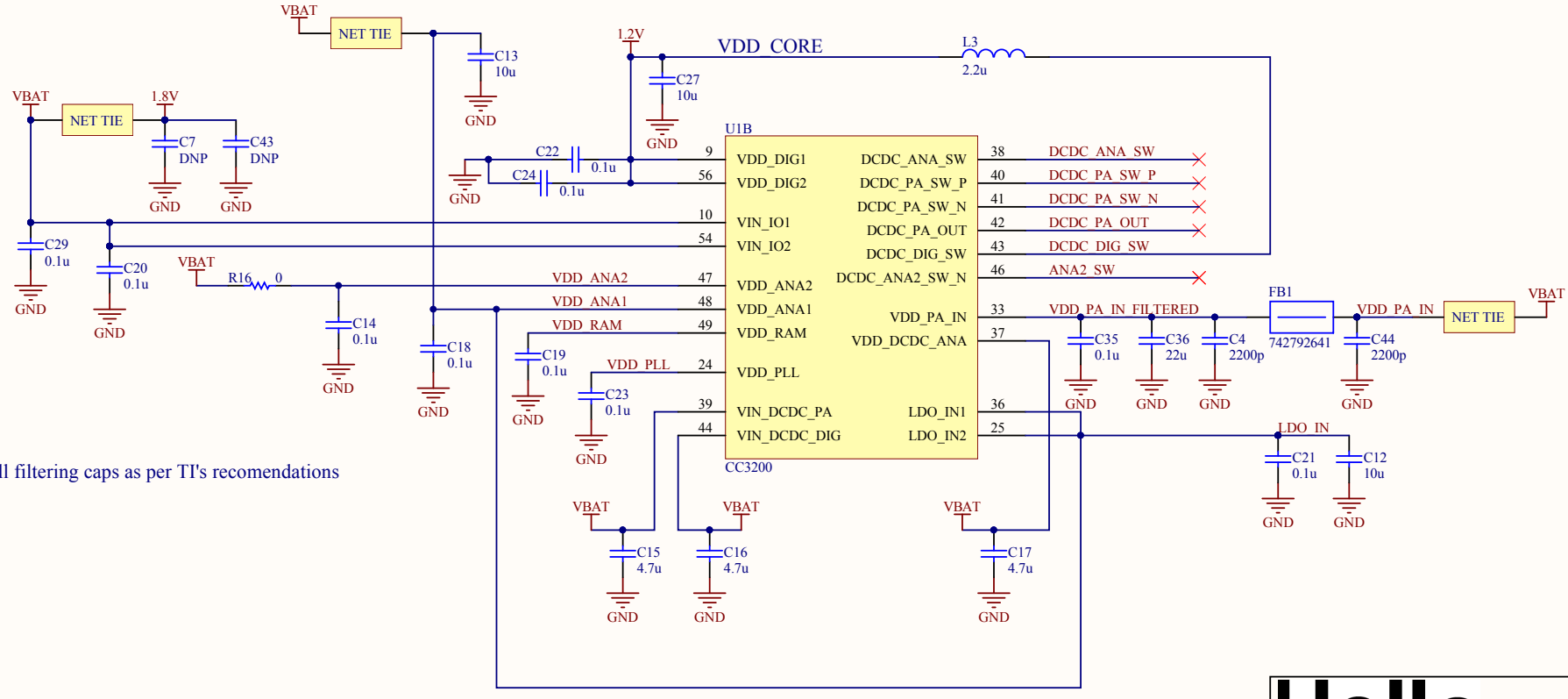

C61
0.1u
GND
EN_SIO
R61
SOP2
10k
Q2A
Si1922EDH-T1-GE3
Q2B
Si1922EDH-T1-GE3
(WHT)
USB_DM
USB_DP
(GRN)
R29
100
R30
100
USB_TXD
USB_RXD
R62
215k
R64
215k
(2R)
CCU_TXD
CCU_RXD
(R)
R63
523k
R65
523k
GND
GND
IF CC3200 is changed to operate off of wide input voltage range,
the 1V8 tie needs to change to VBAT
U1A
from I2S Codec
I2S_DOUT
50
GPIO0
TX GPIO17
8
SDHOST_CMD 1.8
SD Card Controller
(GRN) DP
USB_TXD
55
GPIO1 TX
GPIO18
11
SSPI_CLK
Flash UART
(WHT) DM
USB_RXD
57
GPIO2 RX
GPIO19
12
SSPI_MOSI
GPIO20
13
SSPI_MISO
to Program Boot Flash
Cross Connect UART
(To Nordic)
CCU_TXD
R70
10
58
GPIO3 ADC1
GPIO21
14
SSPI_SEL
CCU_RXD
R27
10
59
GPIO4 ADC2
Analog Input from Dust Sensor
DUST_SENSE
60
GPIO5 ADC3
GPIO22
15
R73
10
GSPI_CS1
Nordic SPI Chip Select
interrupt from Nordic
GSPI_INT
61
GPIO6
GPIO23
16
JTAG_TDI
JTAG programming
interrupt from mid-board RTC
RTC_INT_N
62
GPIO7
GPIO24
17
JTAG_TDO
from I2S Codec
I2S_FSYNC
63
GPIO8
GPIO25
21
SOP2
2
D1
1
1N4148WS
Digital Output to Dust Sensor
DUST_PWM
64
GPIO9
GPIO26
29
CCU_ANT1
Antenna Diversity
I2C Sensors
I2C_SCL
1
GPIO10
GPIO27
30
CCU_ANT2
Codec Master Clock
MCLK_OUT_R20
10
2
GPIO11
GPIO28
19
JTAG_TCK
JTAG programming
from I2S Codec
I2S_SCLK
3
GPIO12
GPIO29
20
JTAG_TMS
I2C Sensors
I2C_SDA
4
GPIO13
GPIO30
53
GSPI_MISO
Nordic SPI CLK
GSPI_CLK
R72
10
5
GPIO14
GPIO31
45
R75
10
I2S_DIN
to I2S Codec
SD Card Controller
SDHOST_DAT 1.8
6
GPIO15
GPIO32
52
R71
10
GSPI_MOSI
SDHOST_CLK 1.8
7
GPIO16 RX
SSPI_CLK
18
CC_3200_PIN18
CC3200
pin 18 is not usable as GPIO
1.8V
R66
1k
R67
2.21k
GND
(TXD)
P4
USB_DM
1
USB_ID
USB_DP
5
(RXD)
6
SOP2
(GPIO25)
5V
DNP
(SCL)
P3
JTAG_TDI
nRESET
JTAG_TDO
(SDA)
EN_SIO
SOP0
(SWD)
DNP
P2
JTAG_TMS
USB_TXD
JTAG_TCK
1.8V
USB_RXD
DNP
Break Out Board
X2
ABM3B-40.000MHZ-10-1-U-T
C25
9p
C26
9p
GND
GND
GND
U1C
WLAN_XTALM
22
WLAN_XTALM
NC
26
NC_P26
WLAN_XTALP
23
WLAN_XTALP
NC
27
NC_P27
NC
28
NC_P28
SOP1
34
SOP1
EPAD
65
SOP0
35
SOP0
GND
RF_BG
31
RF_BG
nRESET
32
nRESET
RTC_XTAL_P
51
CC3200
VBAT
D2
1N4148WS
R1
10k
C1
10u
GND
1.8V
R81
215k
RTC_CLK
RTC_INT_N
RTC0
I2C_SDA
I2C_SCL
SDA
SCL
Vcc
Vss
CLKOUT
INT#
AB-RTCMC-32.768kHz-AIGZ-S7
GND
Flash / Normal
HALT / RUN
SOP2
R5
2.7k
GND
SOP1
R6
10k
GND
2W / 4W
SWD / JTAG
SOP0
R7
10k
GND
IF CC3200 is changed to operate off of wide input voltage range,
the 1V8 tie needs to change to VBAT
Hello
TITLE
M4F_MCU
REV
DVT
DATE
12/29/2014
DRAWN BY
D. Fusi
SHEET 1 OF 7


H1 H2 H3 H4
DNP DNP DNP DNP
mounting holes
3.3V
TP8
to the bottom board
P1
5V
GND
3.3V
GND
1.8V
FFC_USB_TXD
FFC_USB_RXD
GND
USB_DM (TXD)
USB_DP (RXD)
USB_ID (SOP2)
SOP2
SPARE1
CCU_CMD
SOP0
GND
JTAG_TMS (SWDCLK)
JTAG_TCK (SWDIO)
GND
JTAG_TDO (I2C_SDA)
JTAG_TDI (I2C_SCL)
C30 2200p GND
C31 2200p GND
C32 2200p GND
C33 2200p GND
C34 2200p GND
51281-2694
IF CC3200 is changed to operate off of wide input voltage range,
the 1V8 tie needs to change to VBAT
1.8V 1.8V
I2C pullups
R14 2.7k
R13 2.7k
I2C Sensors
I2C_SDA
I2C_SCL
R31 100k
GND
IF CC3200 is changed to operate off of wide input voltage range,
the 1V8 tie needs to change to VBAT
to the top board
P5
GSPI_CS1
GND
GSPI_MISO
GSPI_MOSI
1.8V R32 100k
GND
GSPI_CLK
RTC_CLK R28 DNP
5V
I2C_SDA
I2C_SCL
GND
I2S_SCLK
I2S_DIN
GND
I2S_DOUT
1.8V
CCU_RXD
CCU_TXD
Cross Connect
GND
GSPI_INT
CCU_DAT
uSD Host Controller
(TXD)
(RXD)
5V
CCU_CMD
CCU_CLK
GND
MCLK_OUT
I2S_FSYNC
3.3V
R34 10k GND
R35 DNP GND
52885-0374
8-bit level shifter
U5
1.8V
3.3V
VCCA
VCCB
USB_TXD
USB_RXD
SDHOST_DAT_1.8
SDHOST_CMD_1.8
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
FFC_USB_TXD
FFC_USB_RXD
SDHOST_DAT_3.3
SDHOST_CMD_3.3
1.8V
R21 0
NRESET
R33 0 DNP
OE
GND
EPAD
TXS0108ERGYR
OE is tied high. Provisions have been added to
tie it to nRESET in case the part doesn't come
up properly (small note in the datasheet p.2)
GND
1.8V
3.3V
C83 0.1u
C84 0.1u
GND
GND
to the top board
CCU_DAT R2 DNP SDHOST_DAT_1.8
CCU_CMD R3 DNP SDHOST_CMD_1.8
CCU_CLK R4 DNP SDHOST_CLK_1.8
to CC3200
Hello
TITLE
Morpheus_middle
REV
DVT
DATE
11/20/2014
DRAWN BY
D. Fusi
SHEET 2 OF 7





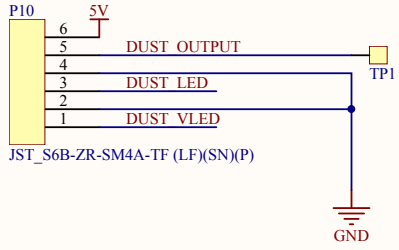


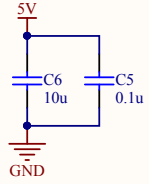
All filtering caps as per TI's recomendations

Route ground traces for C15, C16 and C17 to single vias on the EPAD. Isolate them from pours in inner layers

Hello		
TITLE: M4F_MCU_Power		REV: DVT
DATE: 11/20/2014	DRAWN BY: D. Fusi	SHEET 3 OF 7

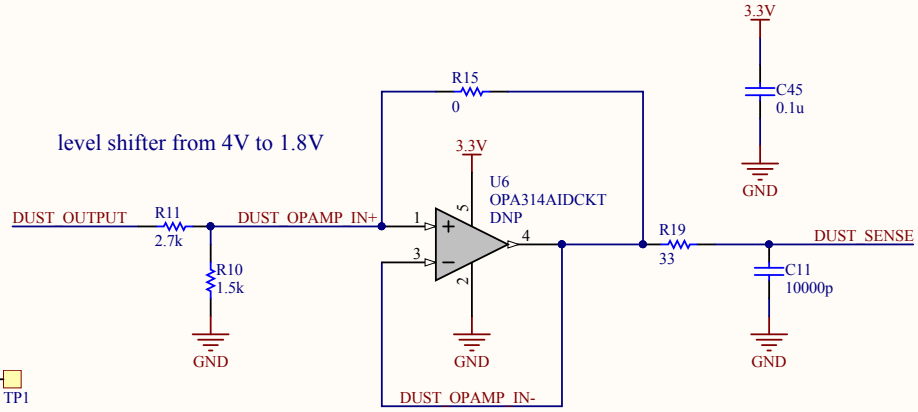
Connector for Sharp dust sensor GP2Y1010AU0F



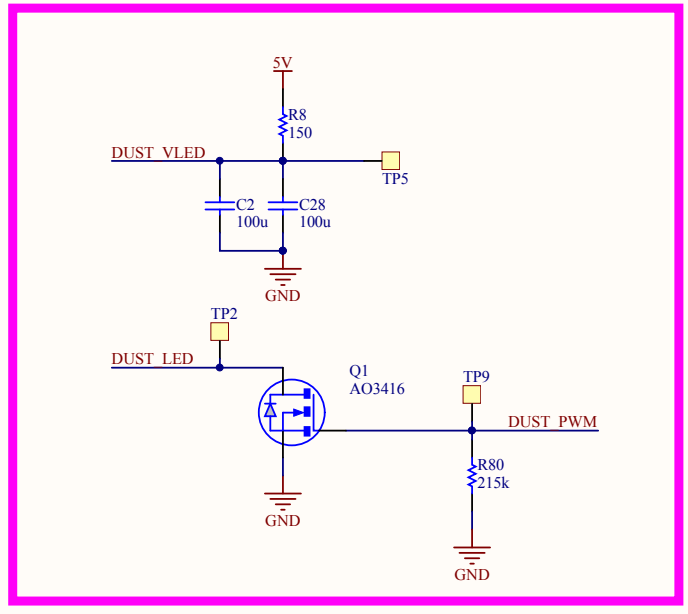


Filtering caps

level shifter from 4V to 1.8V

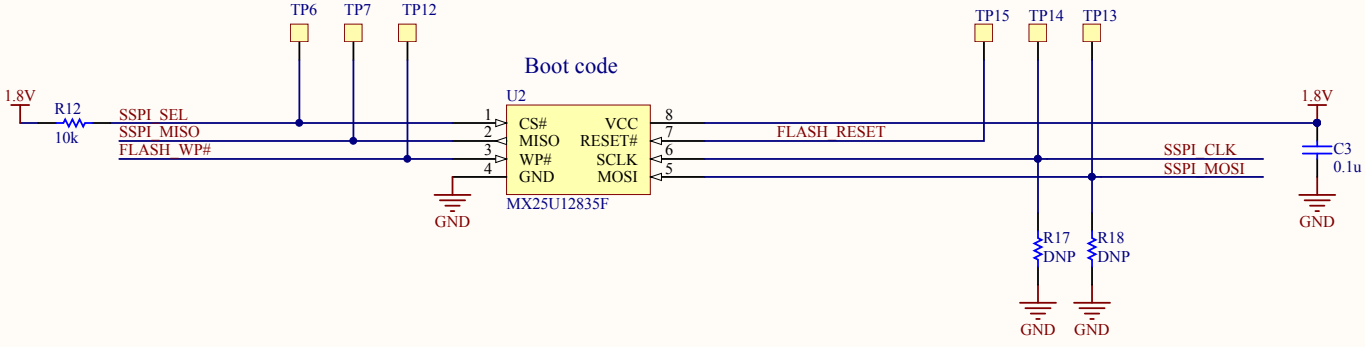


As on the GP2Y1010 datasheet

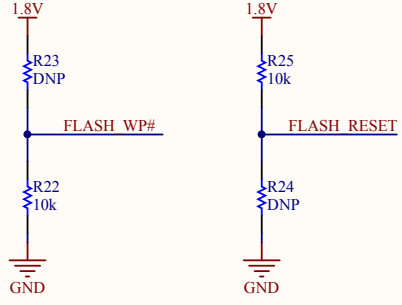


Hello

TITLE: Air_quality		REV: PVT
DATE: 12/30/2014	DRAWN BY: D. Fusi	SHEET 4 OF 7



TI wants 17 and R18 to be installed but we've always been good without

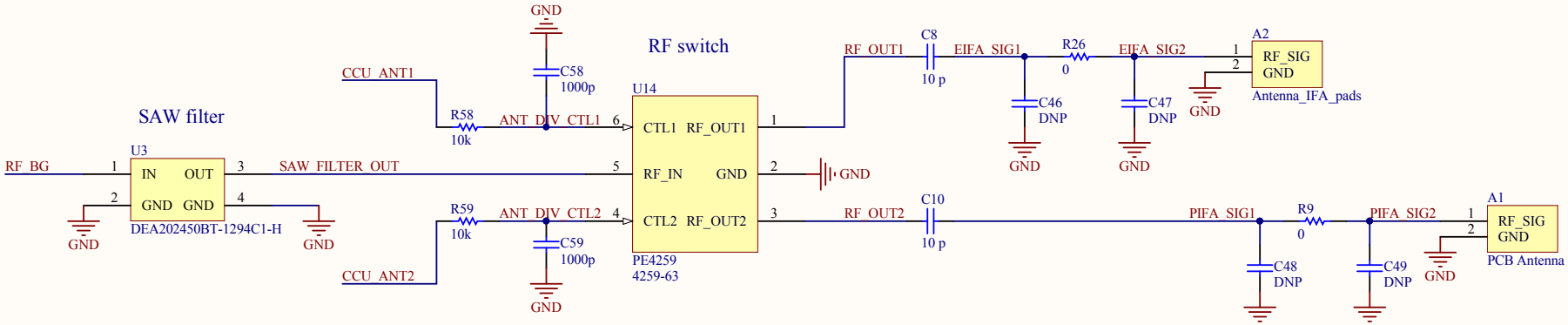


Datasheet is unclear, so for now we pull reset high and WP low

Hello

TITLE: Flash memory	REV: DVT
DATE: 11/20/2014	DRAWN BY: D. Fusi
	SHEET 5 OF 7

R9 and R26 will be inductors if needed. C46 and C47 DNP for now



RF components: Johanson 0201 L-05B0N6CV6S 250R05L0R2AV4S
Murata 0201 GJM0335C1ER20WB01

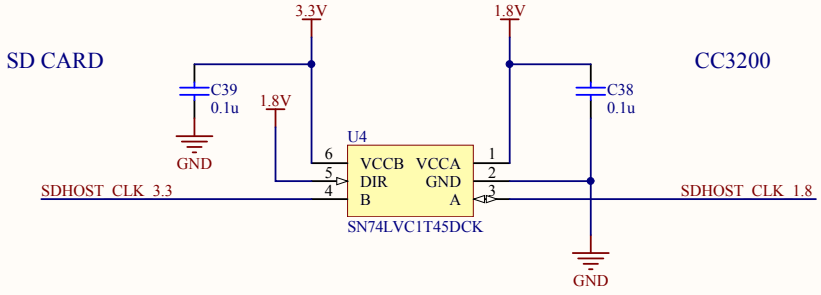
Murata 0402 GJM1555C1H100GB01D
Murata 0402 LQP15MN1N0B02

GJM series is better than GRM for RF

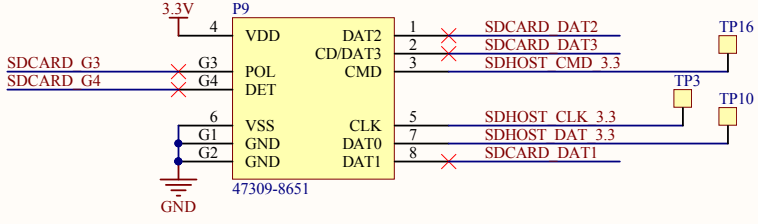
Hello

TITLE: M4F_MCU_Antennas	REV: DVT
DATE: 11/20/2014	DRAWN BY: D. Fusi
	SHEET 6 OF 7

CLK needs a dedicated level shifter beacuse of speed



CMD and DAT shifter on dedicated level shifter



SD Card connector

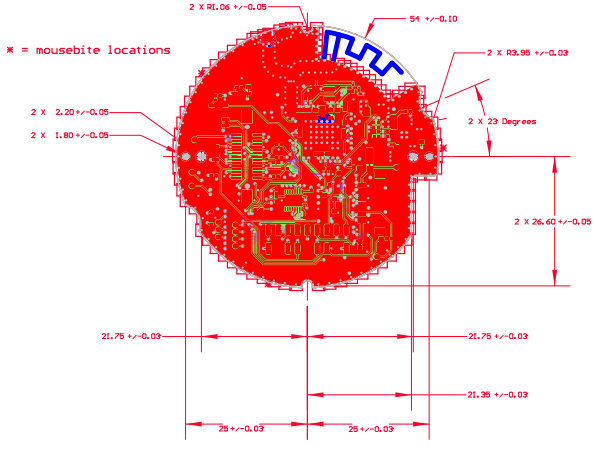
Hello

TITLE: SD_Card	REV: DVT
DATE: 11/20/2014	DRAWN BY: D. Fusi
	SHEET 7 OF 7

Fabrication / Assembly Notes

1. Material: Rigid FR-4, RoHS compliant: material should meet or exceed requirements of IPC 4101/126. ITEQ IT-180A Pre-approved.
2. Number of electrical layers: 6
3. Trace / Space minimum: 5mil (all layers)
4. Thickness: 0.782mm (31mils) +/- 0.1mm finished
5. Finish: ENIG plating on exposed copper
6. Soldermask: per IPC-SM-840, color matte black, registration within +/- 76um of circuit layer
7. Silkscreen: do printed silkscreen on top and bottom layers, color white. Clip on pads.
8. Board must be lead free process compatible and able to withstand minimum of
   5 cycles at 250 degrees celsius
9. All Test/QA/QC markings to be made on back side of PCB
10. x mousebites shall be no larger than 0.05 mm
11. All Dimensions are after plating/finishing
12. All components must be placed within +/- 0.10mm
13. This board has controlled impedences between Layers 5 and 6.
    0.45mm traces on Bottom layer (layer 6) are 50 ohm +/-5 Ohm controlled impedence traces referenced to layer 5.
    Fab vendor to adjust trace width as needed but no smaller than .125mm without approval.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Paste				
2	Top Overlay				
3	Top Solder	Solder Resist	0.010mm	3.5	
4	Top Layer	Copper	0.025mm		
5	Dielectric1	FR-4	0.102mm	4.2	
6	Signal Layer 1	Copper	0.025mm		
7	Dielectric 5		0.152mm	4.2	
8	Signal Layer 2	Copper	0.025mm		
9	Dielectric 4		0.102mm	4.2	
10	GND	Copper	0.025mm		
11	Dielectric2		0.152mm	4.2	
12	PWR	Copper	0.025mm		
13	Dielectric3		0.102mm	4.2	
14	Bottom Layer	Copper	0.025mm		
15	Bottom Solder	Solder Resist	0.010mm	3.5	
16	Bottom Overlay				
17	Bottom Paste				



Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
⊠	1	0.700mm (27.56mil)	NPTH	Round
▼	1	0.900mm (35.43mil)	NPTH	Round
✪	2	1.800mm (70.87mil)	NPTH	Round
○	2	2.200mm (86.61mil)	NPTH	Round
✲	33	0.300mm (11.81mil)	PTH	Round
⊠	122	0.305mm (12.01mil)	PTH	Round
□	317	0.200mm (7.87mil)	PTH	Round
	478 Total			

METRIC			
DIMENSIONS ARE IN MILLIMETERS			
TOLERANCES:			
0 > - < 2	0.10		
2 > - < 10	0.10		
10 > - < 50	0.10		
50 > - < 100	0.15		
100 > - < 200	0.20		
200 > -	0.20		
ANGLES	1.00		

DRAFTER	DATE
DESIGNER	DATE
rsb/dfusi	01/12/15

hello

TITLE:
Morpheus Middle Board

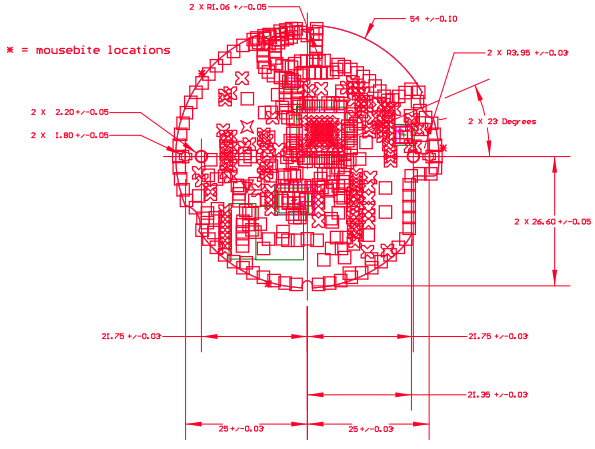
SIZE	DWG. NO.	REV
B	201-00004-A	

SCALE: 1:1	WEIGHT:	SHEET 1 OF 1

Fabrication / Assembly Notes

1. Material: Rigid FR-4, RoHS compliant: material should meet or exceed requirements of IPC 4101/126. ITEQ IT-180A Pre-approved.
2. Number of electrical layers: 6
3. Trace / Space minimum: 5mil (all layers)
4. Thickness: 0.782mm (31mils) +/- 0.1mm finished
5. Finish: ENIG plating on exposed copper
6. Soldermask: per IPC-SM-840, color matte black, registration within +/- 76um of circuit layer
7. Silkscreen: do printed silkscreen on top and bottom layers, color white. Clip on pads.
8. Board must be lead free process compatible and able to withstand minimum of 5 cycles at 250 degrees celsius
9. All Test/QA/QC markings to be made on back side of PCB
10. x mousebites shall be no larger than 0.05 mm
11. All Dimensions are after plating/finishing
12. All components must be placed within +/- 0.10mm
13. This board has controlled impedences between Layers 5 and 6.
    0.45mm traces on Bottom layer (layer 6) are 50 ohm +/-5 Ohm controlled impedence traces referenced to layer 5.
    Fab vendor to adjust trace width as needed but no smaller than .125mm without approval.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Paste				
2	Top Overlay				
3	Top Solder	Solder Resist	0.010mm	3.5	
4	Top Layer	Copper	0.025mm		
5	Dielectric1	FR-4	0.102mm	4.2	
6	Signal Layer 1	Copper	0.025mm		
7	Dielectric 5		0.152mm	4.2	
8	Signal Layer 2	Copper	0.025mm		
9	Dielectric 4		0.102mm	4.2	
10	GND	Copper	0.025mm		
11	Dielectric2		0.152mm	4.2	
12	PWR	Copper	0.025mm		
13	Dielectric3		0.102mm	4.2	
14	Bottom Layer	Copper	0.025mm		
15	Bottom Solder	Solder Resist	0.010mm	3.5	
16	Bottom Overlay				
17	Bottom Paste				



= mousebite locations

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
⊠	1	0.700mm (27.56mil)	NPTH	Round
▼	1	0.900mm (35.43mil)	NPTH	Round
✪	2	1.800mm (70.87mil)	NPTH	Round
○	2	2.200mm (86.61mil)	NPTH	Round
✡	33	0.300mm (11.81mil)	PTH	Round
⊠	122	0.305mm (12.01mil)	PTH	Round
□	317	0.200mm (7.87mil)	PTH	Round
	478 Total			

METRIC

DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:

0 > - < 2	0.10
2 > - < 10	0.10
10 > - < 50	0.10
50 > - < 100	0.15
100 > - < 200	0.20
200 > -	0.20
ANGLES	1.00

DRAFTER | DATE

DESIGNER: rsb/dfusi | DATE: 01/12/15

hello

TITLE: Morpheus Middle Board

SIZE: B | DWG. NO.: 201-00004-A | REV:

SCALE: 1:1 | WEIGHT: | SHEET 1 OF 1