

ESP32 - MESH KIT - SENSE

battery connector

wake-up button

power switch

led indicator

micro usb port

ambient light sensor

i2c connector

temperature & humidity sensor

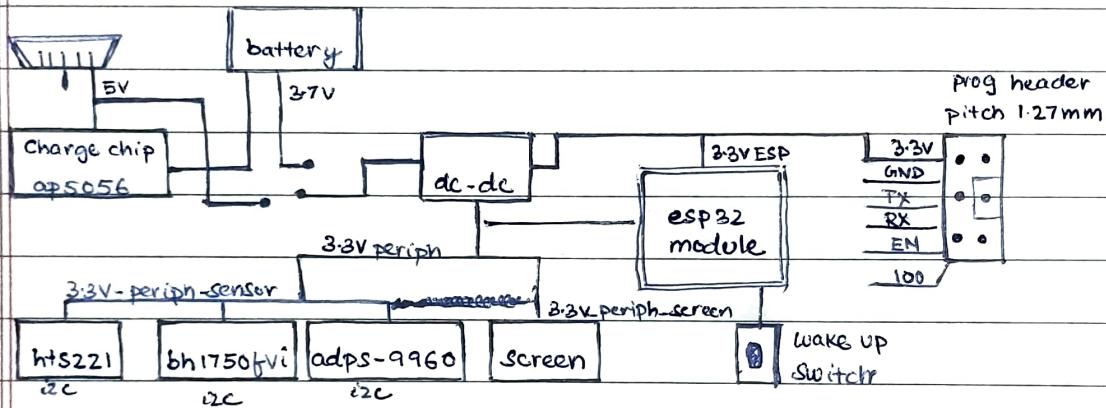
esp32-wroom2d module

charge management ic

dc/dc converter

lcd screen connector

esp-prog connector



INDICATORS

charge

PARTS

downloader

ESPRESSIF NETWORK

sensor

e-ink screen

CONFIGURATION APP

screen

lithium-ion battery

esp touch

wifi

COMPILE ENVIRONMENT

network

esp-idf

(server)

esp-idf ulp

device wakeup from deep sleep mode.

- gpio
- timer
- ulp

combine deep sleep with other functions

ESP32-D0WDQ6

UFL antenna

winband 250232TV1Q

4000T F8100

winband 25N01GNZE1G

AAV71634

08DHMYJW

G3P

REFERENCE

ESP32 → WiFi 2.4GHz BT 4.2 2 cores + ULP peripherals
40nm

CODE UPLOAD

<https://github.com/espressif/esp-idf>

① Hold BOOT

② Press EN
reset

make menuconfig

make flash

sudo usermod

make monitor exit → Ctrl+]

-a -G dialog

(+)

→ make flash monitor

\$USER

\$ESPPORT

\$ESPBAUD → flash

\$MONITORBAUD → monitor

BLUETOOTH

bluetooth controller & VHCI

PERIPHERALS

ADC

bluetooth common

CAN

bluetooth LE

DAC

bluetooth classic

GPIO + RTC lowpower 10

I2C

NETWORKING

I2S

Wi-Fi

LED control

SPI master

ethernet

MCPWM

SPI slave

IP network layer

pulse counter

timer

application layer

remote control

touch sensor

SDMMC host

UART

SD SPI host

SPIO slave

signal-delta modulation

PROTOCOLS

mDNS

ESP-TLS

HTTP client

HTTP server

HTTPS server

ASIO

ESP-MQTT

modbus

IP network layer

STORAGE

SPI flash and partition

SD/SDIO/MMC driver

non-volatile storage

NVS partition generation

virtual filesystem

FAT filesystem

weak leveling

SPIFFS filesystem

mass manufacturing

CONFIGURATION OPTIONS

introduction

using `sdKconfig.defaults`

Kconfig formatting rules

backward compatibility ↑

config. options reference

customization

SYSTEM

freeRTOS

freeRTOS additions

heap memory allocation

heap memory debugging

himem (ent. SPI RAM)

interrupt allocation

watchdogs

efuse manager

inter-process call

high resolution timer

logging

event loop library

application level tracing

power management

sleep modes

over-the-air updates

ESP HTTPS OTA

ESP pthread

Error codes, helper funcs

misc. system APIs

ERROR CODES REFERENCE

API GUIDES

general notes

build system

build system (cmake)

error handling

fatal errors

event handling

deep sleep wake ups

esp32 core dump

flash encryption

freertos SMP changes

thread local storage

high level interrupts

JTAG debugging

bootloader

partition tables

secure boot

ULP coprocessor

ULP coprocessor (cmake)

unit testing (& cmake)

app level tracing

console component

ROM debug console

RF calibration

WiFi driver

ESP-MESH

BlueFi

external SPI-RAM

linker script generation

ESP32 DEVKIT v4

- D0, D1, D2, D3, GND, CLK
 - used internally for SPI flash
 - C15 may cause reset issue or GPIO0 signal issue.

DATASHEET

TECHNICAL REFERENCE MANUAL

DATASHEETESP32 DOWD Q6
TSMC

DOWD ↑ package size

D2WD

SDWD

#processor ↑ flash

fine grained clock gating

multiple power modes

dynamic power scaling

adjustable power amplifier

LOW POWER
APPLICATIONS

antenna switch

RF balun

power amplifier

low-noise receive amplifier

filters

power management modules

COMPLETE
SYSTEM

WIFI

802.11 b/g/n

802.11n (2.4GHz), upto 150Mbps

WMM

TX/RX A-MPDU, RX A-MSDU

defragmentation

automatic beacon monitoring (hardware TSF)

9x virtual WiFi interfaces

simultaneous support for infrastructure station, soft AP, promiscuous mode

antenna diversity

BT

compliant with Bluetooth v4.2 BR/EDR and BLE specs.

class - 1, 2, 3 transmitter without ext. power amplifier

enhanced power control

+12dBm transmitting power

NZIF receiver with -97dBm BLE sensitivity

adaptive frequency hopping (AFH)

standard HCI based on SDIO / SPI / UART

high speed UART HCI, upto 4 Mbps

Bluetooth v4.2 BR/EDR BLE dual mode controller

synchronous connection-oriented / extended (Sco/escō)

CVSD and SBC for audio codec

Bluetooth piconet and scatternet

multi-connections in classic BT and BLE

simultaneous advertising and scanning

CPU AND MEMORY

intensa single/dual-core 32bit LX6 microprocessors, upto

600 MIPS (200 MIPS for ESP32-S0WD, 400 MIPS for ESP32-D2WD)

448 KB ROM

520 KB SRAM

16 KB SRAM in RTC

QSPI supports multiple flash / SRAM chips

CLOCKS AND TIMERS

internal 8MHz oscillator with calibration

internal RC oscillator with calibration

external 2~60MHz crystal oscillator

(40MHz only for WiFi / BT)

external 32 kHz crystal oscillator for RTC with calibration

2 timer groups, inc. 2x 64 bit timers, 1x main watchdog for each group

1 RTC timer

RTC watchdog

ADVANCED PERIPHERAL INTERFACES

34x programmable GPIOs

12bit SAR ADC upto 18 channels

2x 8-bit DAC

10x touch sensors

4x SPI

2x I²S

2x I²C

3x UART

1 host (SD / eMMC / SDIO)

1 slave (SDIO / SPI)

ethernet MAC interface with dedicated DMA

and IEEE 1588 support

CAN 2.0

IR (Tx/Rx)

motor PWM

LED PWM upto 16 channels

hall sensor

SECURITY

secure boot

flash encryption

1024-bit OTP, upto 768 bit for customers

cryptographic hardware acceleration

- AES • hash (SHA-2) • RSA • ECC

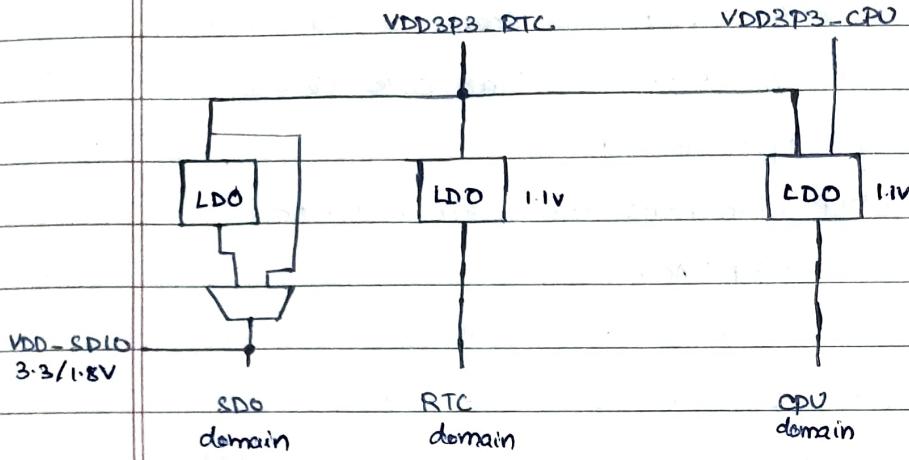
PIN DESCRIPTION

↓

1	VDDA	p	analog PS	2.3 - 3.6V
2	LNA-IN	o	RF IO	
3	VDD3P3	p	analog PS	
4	VDD3P3	p	analog PS	
5	SENSOR-VP	i	adc1-ch0	rtc-gpio00 gpio36
6	SENSOR-CAPP	i	adc1-ch1	rtc-gpio01 gpio37
7	SENSOR-CAPN	i	adc1-ch2	rtc-gpio02 gpio38
8	SENSOR-VN	i	adc1-ch3	rtc-gpio03 gpio39
9	CHIP_PU	i	chip power up / enable	
10	VDET-1	i	adc1-ch6	rtc-gpio04 gpio34
11	VDET-2	i	adc1-ch7	rtc-gpio05 gpio35
12	32K-XP	io	32KHz input toucha	adc1-ch4 rtc-gpio09 gpio32
13	32K-XN	io	32KHz output touch8	adc1-ch5 rtc-gpio08 gpio33
14	GPIO25	io	emac-rxd0	dac-1 adc2-ch8 rtc-gpio06 en
15	GPIO26	io	emac-rxd1	dac-2 adc2-ch9 rtc-gpio07
16	GPIO27	io	emac-rxdv	touch7 adc2-ch7 rtc-gpio17
17	MTMS	io	adc2-ch6	rtc-gpio16 gpio14
18	MTDI	io	adc2-ch5	rtc-gpio15 gpio12
19	VDD3P3_RTC	p	RTC IO PS	2.3 - 3.6V
20	MTCK	io	adc2-ch4	rtc-gpio14 gpio13

S 21	M TDO	io	adc2-ch3	rtc-gpio3	gpio15
22	GPIO2	io	adc2-ch02	rtc-gpio12	gpio2
23	GPIO0	io	adc2-ch21	rtc-gpio11	gpio0
↑ 24	GPIO4	io	adc2-ch0	rtc-gpio10	gpio4
↓ 25	GPIO16	io	U2RXD	gpio16	
26	VDD-SPI0	p	U2TXD	OUTPUT PS 1.8V / VDD3P3-RTC	
27	GPIO17	io	U2TXD	gpio17	
28	SD-DATA-2	io	U1TXD	gpio9	
29	SD-DATA-3	io	U1TXD	gpio10	
30	SD-CMD	io	U1CTS	gpio11	
E 31	SD-CLK	io	U1CTS	gpio6	
32	SD-DATA-0	io	U2RTS	gpio7	
33	SD-DATA-1	io	U2RTS	gpio8	
34	GPIO5	io		gpio5	
35	GPIO18	io		gpio18	
36	GPIO23	io		gpio23	
37	VDD3P3-CPU	p	CPU IO PS		
↑ 38	GPIO19	io	U0CTS	gpio19	
↓ 39	GPIO22	io	U0RTS	gpio22	
40	U0RXD	p	U0RXD	gpio2	
41	U0TXD	io	U0TXD	gpio1	
42	GPIO21	io			
N 43	VDDA	p	analog PS	2.3-3.6V	
44	Xtal-P	o	external	crystal output	
45	Xtal-N	i	external	crystal input	
46	VDDA	p	analog power supply		
47	CAP2	i	3nF cap and 20kΩ R in II		
↑ 48	CAP1	i	10nF series cap to ground		
.. B ← 49	GND	p	ground		

POWER SCHEME



STRAPPING PINS

MTDI, GPIO01, GPIO2, *MTDO, GPIO5 } GPIO-STRAPPING
register

- reset → power-on reset during chip's reset release, RTC watchdog reset the latches of the strapping pins
- brownout reset sample the voltage as strapping bits, and hold these bits until after reset release, the the device is powered down or strapping pins function as shorted down.
- normal function pins.

CPU

2 low power Xtensa 32-bit LX6 microprocessors

- 7 stage pipeline to support clock frequency upto 240 MHz.
- 16/24 bit instruction set provides high code density.
- support for floating point unit
- support for DSP instructions, eg. 32-bit multiplier, 32-bit divider, 60-bit MAC.
- support for 32 interrupt vectors from about 70 sources.
- RAM/ROM interface for instructions & data.
- local memory interface for fast peripheral register access.
- external and internal interrupt sources.
- JTAG for debugging

INTERNAL MEMORY

- 448 KB ROM for booting and core functions
- 520 KB on-chip SRAM for data and instructions
- 8 KB of SRAM in RTC (aka RTC FAST memory)
can be accessed by main CPU during RTC boot
(from deep-sleep mode.)
- 8 KB of CRAM in RTC (aka RTC SLOW memory)
can be accessed by co-processor during deep-sleep mode)
- 1 kbit of eFuse, 256 bits used by system (MAC address and chip configuration), remaining 768 bits reserved for customer applications, including flash encryption and chip ID.
- embedded flash (ESP32-D2WD)

EXTERNAL FLASH AND SRAM

multiple QSPI flash and SRAM chips supported. hardware encryption/decryption based on AES also supported.

8, 16, 32 bit R/W to SRAM supported (Crypto 8MB).

external QSPI flash, SRAM accessed through high speed caches.

upto 16MB external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.

11MB + 248 KB — 3MB + 248 KB — instruction space.

4MB at a time to read-only memory space.

MEMORY MAP

~~0000 0000 X~~

• ~~BF⁴⁰ 0000~~ cache — external memory

~~3F80 0000~~ cache — external memory

~~3FC0 0000 X~~

~~3FF0 0000~~ peripheral

~~3FF8 0000~~ embedded memory

~~4000 0000~~ embedded memory

~~400C 0000~~ cache — external memory

~~40C0 0000 X~~

~~5000 0000~~ embedded memory

~~5000 2000~~ ~~FFFF FFFF~~ X

FFFF FFFF

64BIT TIMERS

4 general purpose timers - 16bit prescalers

64bit auto reloadable up/down counters

• 16 bit prescaler, from 2 to 65536

• 64 bit timer

- configurable up/down counter
- halt/resume of time based counter
- auto-reload at alarming
- software-controlled instant reload
- level and edge interrupt generation

WATCHDOG TIMERS

3x 2x Main WDT 1x RTC WDT

intended to recover from unforeseen fault.

9 stages - 3/4 actions upon expiry of time period,

- interrupt
 - CPU reset
 - core reset
 - system reset
- a timeout value can be set for WDT only

• * each stage individually

during flash boot, RWDT and MWDT start automatically.

(to detect and recover from booting problems).

SPI flash boot protection ↑

CPU CLOCK

external + PLL / internal 8MHz oscillator

RTC CLOCK

external 32KHz crystal clock, 14

external internal RC oscillator ~ 150KHz

internal 8MHz oscillator, 1/256

AUDIO PLL CLOCK

generated by ultra-low noise fractional N-PLL.

RADIO

2.4 GHz transmitter → receiver, bias, regulators,
balun, Tx-Rx switch.

ACCELERATOR

hardware accelerator of general algorithms

- AES (FIPS PUB 197)
 - SHA (FIPS PUB 180-4)
 - RSA
 - ECC
- big integer multiply (modular)
max. operation length = 4,096 bits
also support code encryption and
dynamic decryption

SPI

SPI, HSPI, VSPI (3) upto 80 MHz (upto 64 byte) FIFO

in slave/master modes 1-line full duplex

4 1/2/4-line half duplex

4 modes of SPI transfer format

based on polarity (CPOL) and phase (CPHA)

all SPIs can be connected to external flash / SRAM / LCD.

each SPI can be served by DMA controllers.

LED PWM

16 channels with configurable periods and dutycycles,

with 25 MHz APB clock, 8 can use 8MHz clock.

each channel 20-bit timer, 16-bit duty.

PWUM

timers, operator, and dedicated capture sub-module.

PULSE COUNTER

Captures pulses and counts pulse edges through 7 modes.

8 channels, 4 at a time. 2 pulse, 2 control signals.

When counter reaches threshold, interrupt is generated.

IR CONTROLLER

8 channels share 512x32 bit memory block to store the transmitting or receiving waveform.

I₂S INTERFACE

I₂C INTERFACE

2x master/slave

- Standard mode (100 kbit/s)
- fast mode (400 kbit/s)
- upto 5MHz
- 7/10-bit addressing mode
- dual addressing mode,

UART

3x RS232, RS485, IrDA upto 5Mbps

hardware mgmt of CTS, RTS and software flow control (XON/XOFF).

(Can be accessed by DMA controller, or directly by CPU)

SDIO / SPI SLAVE CONTROLLER

SD / SDIO / MMC HOST CONTROLLER

ETHERNET MAC INTERFACE

ULTRA LOW-POWER CO-PROCESSOR

TOUCH SENSOR

DAC

HALL SENSOR

ADC

GPIO

RTC AND LOW POWER MANAGEMENT

- active mode
- light-sleep mode
- modern-sleep mode
- deep-sleep mode
- hibernation mode

BLUETOOTH LINK CONTROLLER

BLUETOOTH STACK

BLUETOOTH INTERFACE

BLUETOOTH RADIO AND BASEBAND

WIFI MAC

WIFI RADIO AND BASEBAND

CLOCK GENERATOR

2.4GHZ TRANSMITTER

2.4GHZ RECEIVER