2. Technical data

This instrument has been built and tested according to IEC publication 348 for Class I instruments and has been supplied in a safe condition. The present Instruction manual contains instructions and warnings which should be followed by the purchaser to ensure safe operation and to keep the instrument in a safe condition.

Properties expressed in numerical values with standard tolerances are factory guaranteed. Those without tolerances are typical values.

A. System

TV-system	:	PAL, 625 lines, 50 Hz field frequency.

B. Video inputs

Signal types	:	- Video signal, with or without sync (only when PM 5570 is synchronized to the external source). - Continuous wave signal. Blanking is mixed to the CW signal by pressing the CW push-button. A pedestal can be added by the CW set-up switch.
Input impedance (front)	:	75Ω
(rear)	:	High ohmic, looped through.
Input amplitude	:	0 to 1Vpp.
Return loss	:	>34 dB up to 7 MHz.

C. Synchronization input

Signal types	:	- Composite video - Black burst - Composite sync (subcarrier free running).
Input impedance	:	High ohmic, looped through.
Input amplitude	:	0.5 to 4Vpp.
Permissible hum	:	100%
Return loss	:	>34 dB to 7 MHz

D. Ext superimposition in

Input impedance	:	High ohmic (DC coupled)
Input amplitude	:	Max. 4.5Vpp
Maximum gain	:	0.33

E. Composite video output

Number of outputs	:	3
Output impedance	:	75Ω ± 1%
Return loss	:	>34 dB up to 7 MHz
Isolation	:	>40 dB up to 1 MHz >30 dB at subcarrier frequency
Composite signal	:	1Vpp ± 1% (with all amplitude controls in nominal position, and all output's terminated with 75 ohms).
Random RF noise	:	<-70 dBrms weighted
Low frequency noise	:	<-56 dBpp.

NB Noise figures are measured with amplitude controls in nominal position and superimposed signals are off.

F. Composite sync output

Output impedance	:	75Ω
Output amplitude	:	2Vpp

G. Subcarrier output

Output impedance	:	75Ω
Output amplitude	:	1Vpp ± 0.1Vpp.
Harmonic contents	:	<-34 dB

H. Trigger output

Signal type	:	Added composite sync and field pulses.
Output impedance	:	1 KΩ
Output amplitude	:	4Vpp

I. Sweep start output

Signal type	:	Pulse, indicating edges of CW set-up jump.
Output impedance	:	Collector with 100Ω series resistor.
Output amplitude	:	15V

J. Composite sync characteristics

A complete colour sync generator is incorporated in the instrument having the correct relationship between colour subcarrier frequency and line frequency as well as interlacing. The field information may be switched off.

Composite sync

Line sync frequency	:	15625 Hz locked to subcarrier.
Line sync duration	:	4,7 µs ±0,2 µs
5 serrations: duration	:	4,7 µs ±0,2 µs
5 pre- and 5 post equalizing pulses: duration	:	2,35 µs ±0,1 µs

Composite blanking

Line blanking: duration	:	11,8 to 12.3 µs
Start of line blanking	:	1,3 to 1,8 µs before line sync leading edge
Vertical blanking duration	:	25 H + 12 µs

Subcarrier

Generated by means of a TCXO (temperature controlled crystal oscillator).

Frequency	:	4433618,75 Hz ±5 Hz

Burst

Duration	:	2,03 to 2,48 µs
Position	:	5,5 µs ±0,2 µs after leading edge of line sync
Burst suppression	:	9 lines
Burst phase	:	135° and 225° alternating or 180°

Genlock

The generator may be synchronized to an external composite video signal or to a composite sync. The line and field frequencies will phase lock to the external sourse and if a burst is present, the subcarrier will lock to it.

Sync lock

Horizontal frequency range	:	15625 Hz ±1 Hz
Lock-in time	:	<7 sec
Jitter with respect to input sync	:	<10 nsec for noise free signal of nom. amplitude
Time offset of sync in video output	:	<100 nsec

Subcarrier lock

Subcarrier frequency range	:	4433618,75 Hz ±25 Hz
Lock-in time	:	<1 sec
Jitter with respect to incoming burst phase	:	<1°

K. Video test signals

a. Square wave signals

Frequencies	:	0.25 Hz 50 Hz, locked to field frequency 15.625 kHz, locked to line frequency 250 kHz, locked to line frequency
Rise time switchable	:	50ns +10 to -0ns 100ns +10 to -0ns 200ns +20 to -0ns
Overshoot	:	<1%
Tilt	:	<1%

b. Pulse & bar signals

Repetition rate	:	Line frequency
Signal types	:	- T pulse and T bar. - 2T pulse and 2T bar. - T pulse, 20T (10T) pulse composite and T bar. - 2T pulse, 20T (10T) pulse composite and 2T bar. - 20T(10T) pulse composite and 20T(10T) bar composite.
Sine squared pulse	:	T : 100ns +10 to -0ns 2T : 200ns +20 to -0ns 10T (system I) : 1µs ±0.03µs 20T (system G) : 2µs ±0.06µs

Can be gated with field frequency square wave giving a window signal.

K-factor	:	<0.5% for T- and 2T pulse
20T (10T) bar width	:	25µs ±0.5µs
Bar rise time	:	T bar : 100ns +10 to -0ns 2T bar : 200ns +20 to -0ns 10T bar composite (system I) : 1µs ±0.05µs 20T bar composite (system G) : 2µs ±0.1µs
Bar overshoot	:	<1%
Bar tilt	:	<1%
20T (10T) chrominance/luminance gain inequality	:	<1%
Delay inequality	:	<10ns
Subcarrier	:	4433618.75 Hz ±5 Hz (TCXO)

c. Sawtooth signals

Repetition rate	:	Line frequency - with superimposed sine wave frequencies - with superimposed subcarrier frequency A duty signal can be added giving alternating three lines duty signal and one line sawtooth.

d. Staircase signals

Repetition rate	:	Line frequency - with superimposed sine wave frequencies - with superimposed subcarrier frequency A duty signal can be added giving alternating three lines duty signal and one line staircase.
Number of steps	:	10 or 5 (switchable)
Non-linearity of staircase	:	<0.5%
Rise time	:	228ns ±20ns

e. Chrominance signals

Signal types	:	- (system I) 10T pulse and 10T bar, chroma only. - (system G) 20T pulse and 20T bar, chroma only. - Chroma staircase (fixed 50% pedestal) The chroma staircase can be jumped on/off.

Jump frequency	:	0.25 Hz	
Rise time	:	Chroma bar (system I)	: 1µs
		Chroma bar (system G)	: 2µs
		Pedestal	: 200ns +20 to -0ns
Chroma staircase	:	Number of rises	: 5
		Rise time	: approx. 1µs
		CLIM	: <0.5% of pedestal amplitude.
		Nominal amplitude	: 875mV ±2% (peak to peak).

f. Composite signal

Signal type	:	White reference bar, 2T pulse, 20T (10T) pulse composite, and staircase.	
Bar width	:	10µs	
2T pulse	:	See technical data, section b.	
20T(10T) pulse	:		
Staircase	:	Number of steps	: 5
		Non-linearity of staircase	:< 0.5%
		Rise time	: 228ns ±20ns

g. ITS

The composite signal can be inserted in the lines 17 and 330 as an ITS signal.

Signal level	:	700mV ±0.5% (independent of gain control settings).

h. Sweep signal

Frequency range	:	0.1 MHz to 10 MHz
Repetition rate	:	50 Hz, locked to field
Amplitude accuracy	:	<±2% 0,1 to 5 MHz <±4% 5 to 10 MHz
Reference	:	4 µs white bar and 4µs black bar at the start of each active line (switchable).
Pedestal	:	Level : 50% of white level Rise time : 200ns +20 to -0ns
Markers	:	1, 2, 3, 4, 5, 6, 7, 8, 9, and 10 MHz (crystal derived, switchable).
Marker width	:	approx. 200µs.

i. Fixed sine wave signals

Frequency range	:	0.1, 1, 2, 3, 4, 5, 6, 7, 8, 9, and 10 MHz.
Frequency accuracy	:	±3% or 15 kHz
Harmonic contents	:	<3%
Reference	:	4µs white bar and 4µs black bar at the start of each active line (switchable).
Pedestal	:	Level : 50% of white level Rise time : 200ns +20 to -0ns

j. Multiburst signal

Frequencies	:	1, 2, 3, 4, 5, and 6 MHz
Frequency accuracy	:	±3%
Reference	:	4µs white bar and 4µs black bar at the start of each active line.
Pedestal	:	Level : 50% of white level Rise time : 200ns +20 to -0ns

k. Duty signal

This signal can only be used in combination with the staircase signals and the sawtooth signals to form duty cycled signals.

Signal levels	:	- 100% white level - black level
Jump function	:	Alternating between white and black level.
Jump frequency	:	0.25 Hz

l. CW set-up (Blanking mixer)

Any externally applied continuous wave signal can be converted into a complete TV signal (incl. set-up, sync, and burst).

Pedestal	:	- 50% white, 350mV ±1% - PRE 1, 100mV (adjustable) - PRE 2, 600mV (adjustable) - continuously variable between 0 and 0.9V
Jump function	:	Alternating between PRE 1 and PRE 2.
Jump frequency	:	0.25 Hz

L. Composite video output signals

The signal parts of the composite video signal can be controlled in amplitude by means of the front plate controls. Rotary switches give easy adjustments to preset levels, while potentiometers ensure flexibility of continuous level control.

a. Video signal

Amplitude range	:	0 to 1Vpp
Nominal level	:	700mVpp ±1%
Preset level	:	200mVpp (adjustable 0 to 1Vpp).

Video signal off is indicated by a blinking light in the test signal push-button.

b. Set-up signal

Amplitude range	:	0 to 0.9Vpp
Amplitude range negative	:	0 to -0.3Vpp
Preset level	:	50mV ±10mV (adjustable 0 to 0.9Vpp).

c. Sync signal

Amplitude range	:	0 to 0.6Vpp
Nominal level	:	300mV ±1%

The sync signal can be switched off

d. Burst signal

Amplitude range	:	0 to 0.6Vpp
Nominal level	:	300mVpp ±2%
The burst signal can be switched between three modes	:	- Alternating phase 135° and 225° - Non-alternating phase 180° - Off

e. Composite video signal

Amplitude range	:	0 to 1.5Vpp
Nominal amplitude	:	1Vpp ±1%
- 3 dB amplitude	:	708mV ±1%
+ 3 dB amplitude	:	1413mV ±1%
Preset amplitude	:	0.5V ±2% (adjustable 0 to 1.5Vpp)

M. Superimposition levels

The superimposition levels are independent of the setting of the composite level control.

a. Subcarrier/sine wave signals

Amplitude range	:	0 to 300mVpp
100mV amplitude	:	100mVpp ±3%
140mV amplitude	:	140mVpp ±3%
280mV amplitude	:	280mVpp ±3%

The superimposition of subcarrier or sine is determined by push-buttons controlling the test signals.

b. Noise signal

Noise spectrum	:	Flat from 10 kHz to 5 MHz within ±3 dB.
Fixed positions	:	- 20 dBrms ±2 dBrms
		- 30 dBrms ±2 dBrms
		- 40 dBrms ±2 dBrms
		- 50 dBrms ±2 dBrms
Variable control	:	0 to -10 dB attenuation of selected position

The superimposed noise can be switched off.

c. Hum signal

1. Internally generated

Frequency	:	50 Hz, mains derived
Amplitude	:	0 to 1,5Vpp
Preset amplitude	:	0,5Vpp ±3%

2. External superimposition

Amplitude range	:	0 to ±0,75V
Gain	:	Continuously variable

The superimposed hum can be switched off

N. Response of video path

Transmission performance with signal level controls in nominal positions and video input level of 0.7 Vpp without sync.

Gain	:	Unity gain ±1%
Amplitude response 10 Hz to 10 MHz	:	10 Hz - 5 MHz : within ±2%
		5 MHz - 10 MHz : within ±4%
50 Hz square wave tilt	:	<0.5%
15 kHz line tilt	:	<1%
Line time non-linearity	:	<0.5%
Differential gain	:	<0.3%
Differential phase	:	<0.5°

O. Remote control (optional)

The selection of test signals can be remotely controlled. The selected test signal will be indicated by the light push-button on the instrument and it may also be remotely indicated.

P. Power supply

Voltage	:	230/115V ±20%
Frequency	:	48 - 65 Hz
Comsumption	:	70 W at 220V

R. Temperature

The instrument works within specification limits at the temperature range of 0 - 45°C ambient when adjusted to nominal values at 20 - 25°C.

Storage	:	- 30°C to + 70°C.

S. Mechanical data

Width	:	6/6 module in PHILIPS universal 19" system.
Height	:	132 mm (3 units)
Depth	:	435 mm
Weight	:	13.5 kg.

3. Accessories

1 Instruction manual
1 Mains cord
1 Extension board, enabling measurements in the instrument when it is in operation.
1 Hexagonal key
2 Brackets

4. Description of the simplified block diagram

Functionally the PM 5570 can be divided into three sections, which are briefly described in this chapter. (For a more detailed description please see chapter 7 in this manual). The three sections are as listed below:

A. TEST SIGNAL GENERATORS
B. SIGNAL PROCESSING
C. CONTROL SECTION

A. Test signal generators

All necessary signal elements are derived from the generators in this section. The generators also contain some mixer networks in order to obtain the different combinations of signal elements.
Finally all generator outputs are combined in the "Adder" circuit and led to the "Signal processing" circuit as a complete test signal

B. Signal processing

In this section, sync, burst and set-up as well as superimposition signals are added to the complete test signal. In addition, all levels are controlled by means of the switches SK43-SK51 and the potentiometers P1-P9.

C. Control section

The "Control section" contains both the control logic for the entire instrument and the timing pulses for all signal generators. It also contains the interface circuitry for remote control of the main function switches SK2-SK20, used for the signal selection.
The timing pulses are synchronized to the signals from the built-in sync pulse generator with genlock facility.
A subcarrier generator is also incorporated in this section, which means that all necessary control pulses, such as sync, burst key, and subcarrier for the signal processing and for external use, are available.

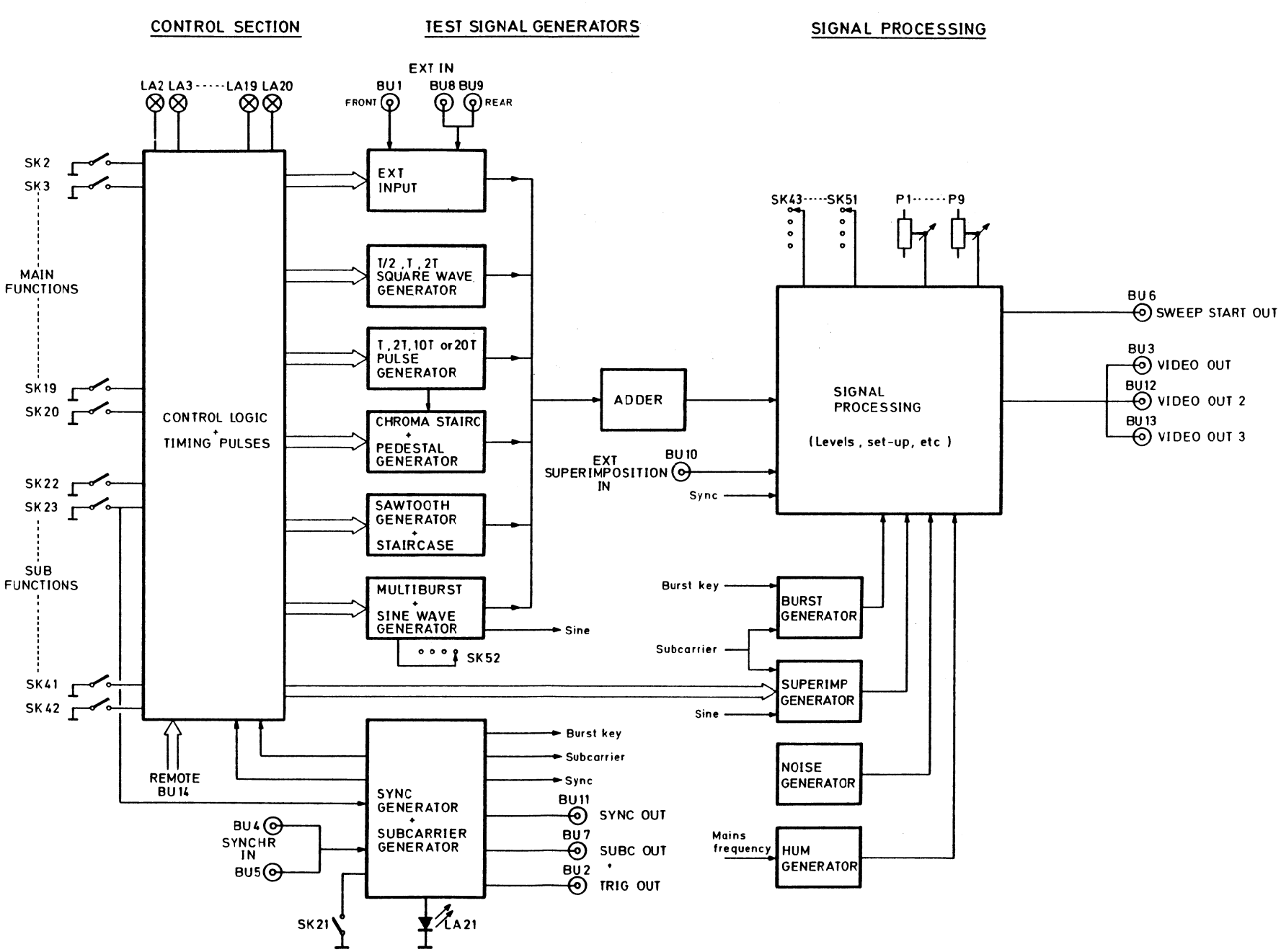

Fig. 4-1 Simplified block diagram

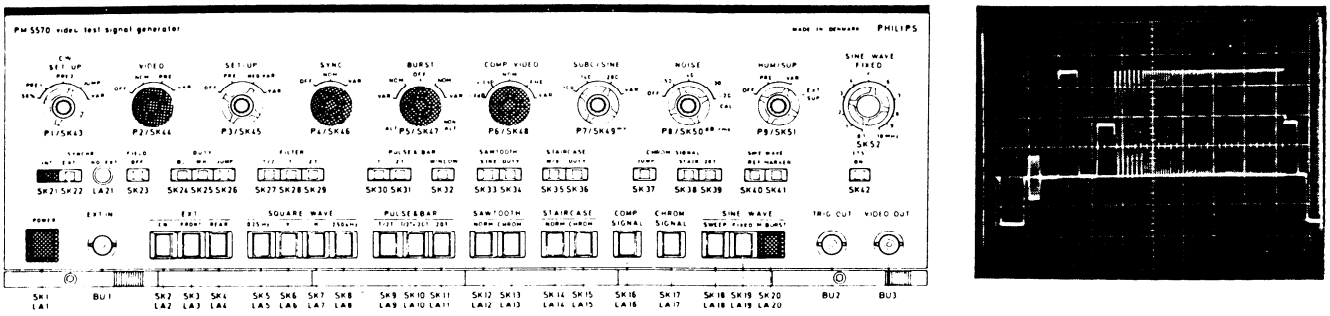

Fig. 6-26 Multiburst signal.

C. Applications

The combination of the PM 5570 and a suitable wideband oscilloscope or waveform monitor constitutes an outstanding video measuring system. The range of applications is broad. The instrument is suitable for routine measurements and alignment of TV studios, switching centres, transmitter stations and link stations. Acceptance testing of video equipment is easily done with the PM 5570 because of the possibilities incorporated for signal processing i.e. amplitude controls and superimposition of hum and noise.

Another large area where the instrument finds its use is in development and service labs, where it is indispensable for the designing and repair of video equipment.

In general the PM 5570 can be used to check the performance of all television equipment and systems since it enables the measurement of all important characteristics such as INSERTION GAIN, NON-LINEAR DISTORTION, and LINEAR DISTORTION.

In the following sections a more detailed description of the measurements is given.
All figure numbers mentioned below can be found in section B. OPERATING THE INSTRUMENT.

INSERTION GAIN

Insertion gain is defined as the ratio, (expressed in decibels) of the peak-to-peak amplitude of a specified test signal at the receiving end to the nominal amplitude of that signal at the sending end.
The peak-to-peak amplitude being defined as the difference between the amplitudes measured at defined points in the signal used.

The square wave signal fig. 6-4 is suitable for measuring the insertion gain because of its "white reference pulse".

NON-LINEAR DISTORTION

In a television circuit the transmission characteristic may not be completely linear. The extent of the non-linear distortion produced primarily depends on:

- the average picture level
- the instantaneous voltage of the luminance signal voltage
- the amplitude of the chrominance signal

There would, in general, be little purpose in describing completely the non-linear characteristics of a transmission circuit. When the C.C.I.R. recommended classification system of non-linear distortions is used, the relevant test signal for a certain distortion can be listed as shown below (all the figure numbers given in the system are related to the test signals which are shown in section B. OPERATING THE INSTRUMENT.):

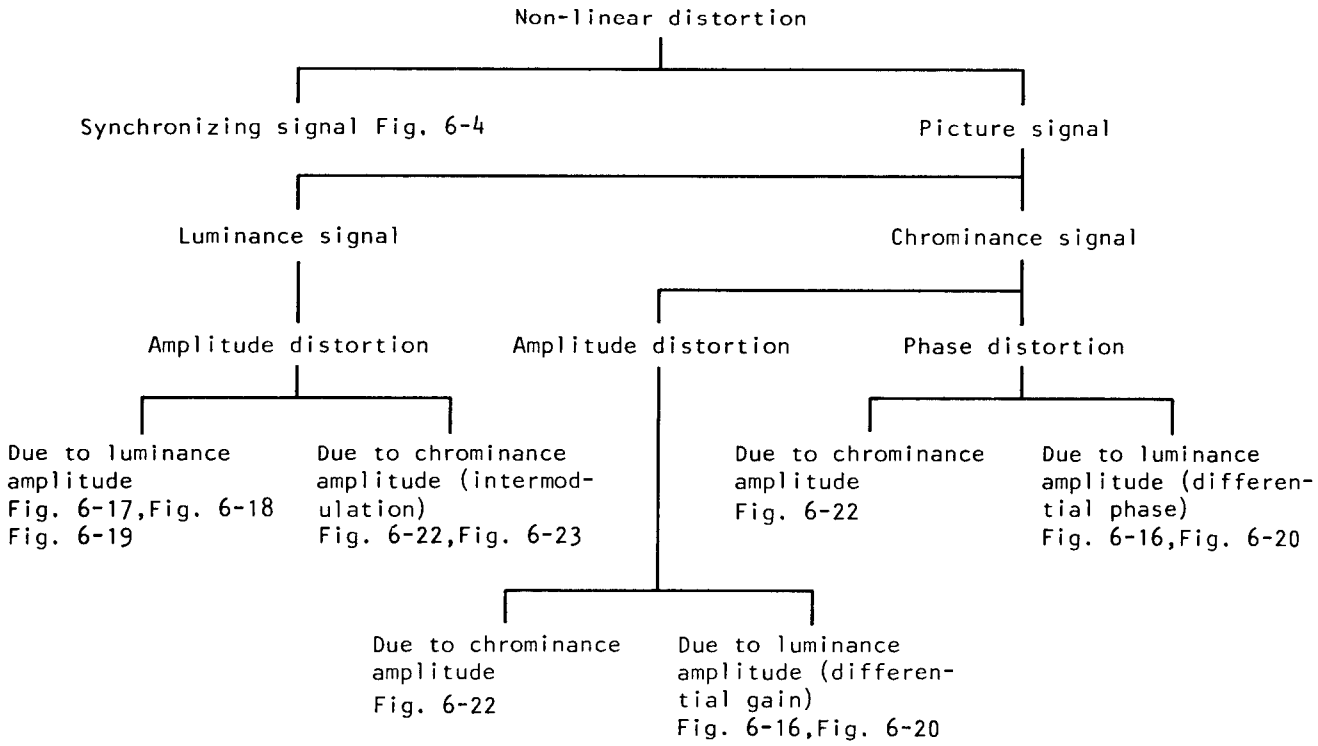

Fig. 6-27 Classification system of non-linear distortions.

LINEAR DISTORTION

Linear distortions are those which can be caused by linear networks. Such distortions do not depend on the average picture level or the amplitude and position of the test signals.

In this case, too, C.C.I.R. has recommended a system of classification of linear distortions. All the figure numbers given in the system are related to the test signals which are shown in section B. OPERATING THE INSTRUMENT.

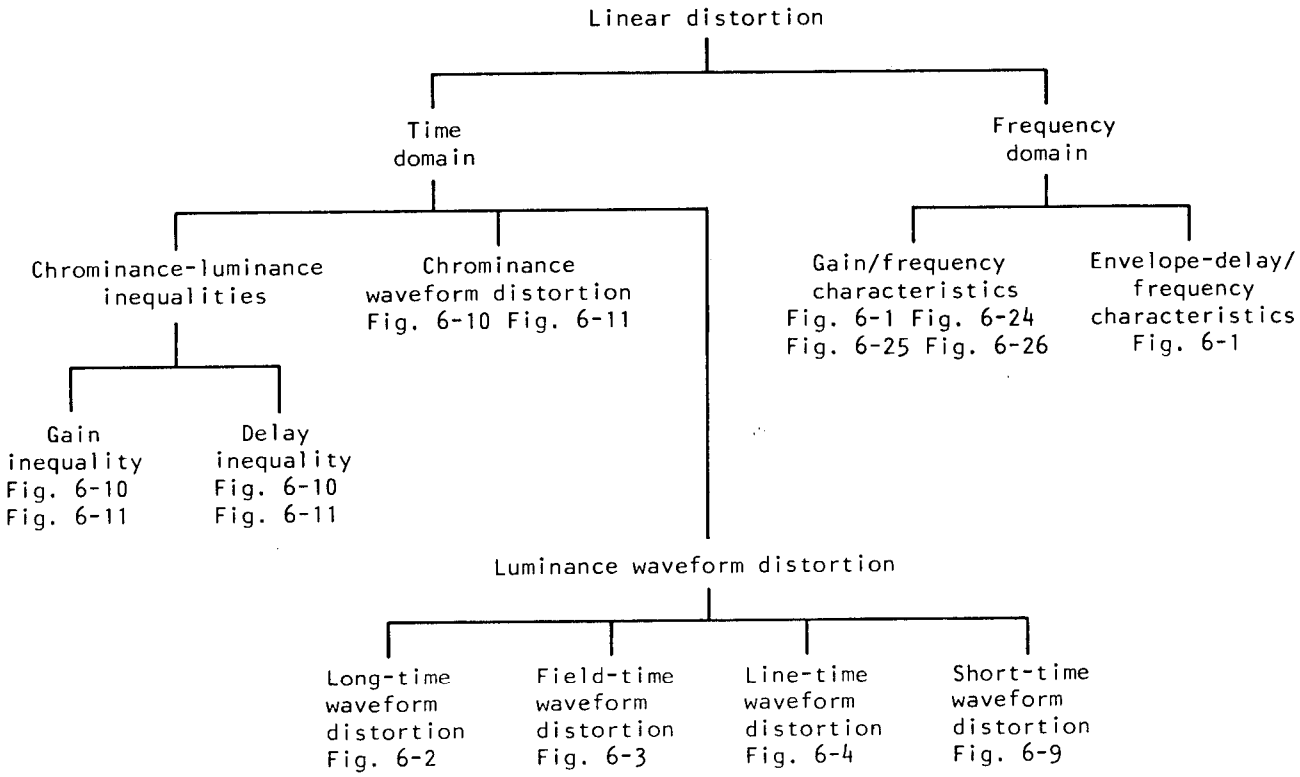

Fig. 6-28 Classification system of linear distortions.

7. Description of the detailed block diagrams

As mentioned in the brief decription of the simplified block diagram, the PM 5570 can be divided into three sections which will be described in this chapter:

A. Test signal generators

Besides an external input circuit with control switches for front- and rear input, all necessary signal elements for a complete test signal are generated in this section.

The "T/2, T, 2T square wave generator" consists of three similarly arranged trapezoid generators followed by a buffer and a filter. The generators are controlled by timing pulses derived in the control section unit 21. The three outputs are then added in the matrix and applied to the output stage "Square wave current", which is a voltage to current converter.

The "T, 2T, 20T pulse generator" also consists of three similarly arranged trapeziod generators followed by a buffer and a filter. But in this case the trapezoid generators are controlled by three different one-shot generators to obtain the right pulse duration for the T, the 2T, and the 20T pulse. Via output amplifiers the T pulse signal and the 2T pulse signal are fed to the matrix circuit. The 20T pulse circuit operates a little differently:
The pulse-and-bar signal requires a correct 20T pulse/bar ratio wich is determined by the pulse/bar switch and an amplitude control circuit (20T pulse/bar ratio). The filter output is then via a chroma switch led to the output amplifier. In the following buffer stage a 20T delay is introduced in order to obtain coincidence between the 20T pulse and the chroma part which is derived from the "Chroma staircase + pedestal generator.
In the matrix the delayed 20T pulse is added to the T pulse and the 2T pulse.
Finally, the matrix output is led to the output stage "Pulse current", which also is a voltage to current converter.

The "Chroma staircase + pedestal generator" contains first the trapezoid generator followed by buffer, filter, output amplifier, and controlled by timing pulses produced in the control section unit 21. This part of the generator is the pedestal generator.
The other part of the generator is the chroma staircase generator. This circuit consists of a staircase generator and a modulator. The staircase generator is controlled by an address circuit. The staircase is applied to the modulator via a filter. A subcarrier signal and the 20T modulation signal from the "T, 2T, 20T pulse generator" are also fed to the modulator.
The modulated signal (chroma + staircase) is then via a filter applied to the matrix, where it is added to the pedestal signal.

The matrix output is led to the output stage "Chroma current", where it is converted from a voltage to a current output.

The "Sawtooth + staircase generator" consists of two signal element generators. The sawtooth generator contains an integrator and a sawtooth control circuit. The "Sawtooth control" determines the amplitude of four different sawtooths, all used as test signals. A reset curcuit for the integrator and the sawtooth control is controlled by timing pulses from unit 21. The integrator output is via an amplifier led to the matrix.
The other part of the generator, the staircase part, comprises the "Staircase generator" with an address circuit controlled by timing pulses. The staircase signal is then applied (via the output amplifier) to the matrix.
The combined signal from the matrix is (via a filter) passed over to the "Sawtooth/ staircase current" stage, which converts the voltage signal to a current out signal.

The "Multiburst + sine generator" consists in principle of a triangle generator followed by a sine shaper and a marker pulse generator.
The function of the triangle generator is as follows: The integrator is charged by the "Oscillator control current" and current switch. When the integrator amplitude has reached a pre-set level the "Triangle amplitude control" initiates the "Flip-flop", which is a tunnel diode. The flip-flop opens for current switch 2 which means that the "Oscillator control current" sinks both the "Integrator" amplitude and the charge current, until a pre-set lower level is reached. At that moment the "Flip-flop" is triggered again, and a new charging of the "Integrator" takes place.
The generator frequency is determined in one of three ways; first, one out of eleven fixed frequencies can be chosen by the "Fixed sine control" SK52.
Secondly, the "Multiburst frequency control", which is a staircase generator with five risers, gives six different frequencies one by one.
Finally, the oscillator frequency can be controlled by the "Sweep control" circuit, (frequency range 0.1 MHz - 10 MHz). The triangle signal is shaped to a sine signal by the "Shaper" circuit. This sine signal passes through a buffer and a switch before enterring the output stage.
In the sweep mode some switchable marker pulses are present from 1-10 MHz in 1 MHz steps. These marker pulses are derived in the "Mixer" circuit, where the applied 1 MHz signal is differentiated and mixed with part of the sine shaped signal. The difference frequency between the sine signal and the harmonics of the needle-pulses is then taken off from the "Mixer" and fed to the "Detector" via a 60 kHz "Low-pass filter". The detector output initiates the "Marker pulse generator", which generates a 200 µs pulse. This pulse is amplified and led to the "Buffer", where it is added to the sine signal.

The current output from the various generators are then applied to the "Adder", which consists of a "Video amplifier" with a feed-back network. The amplifier is a current-to voltage-converter, where the dc-level is kept constant by means of the "Sample and hold" circuit followed by a filter.

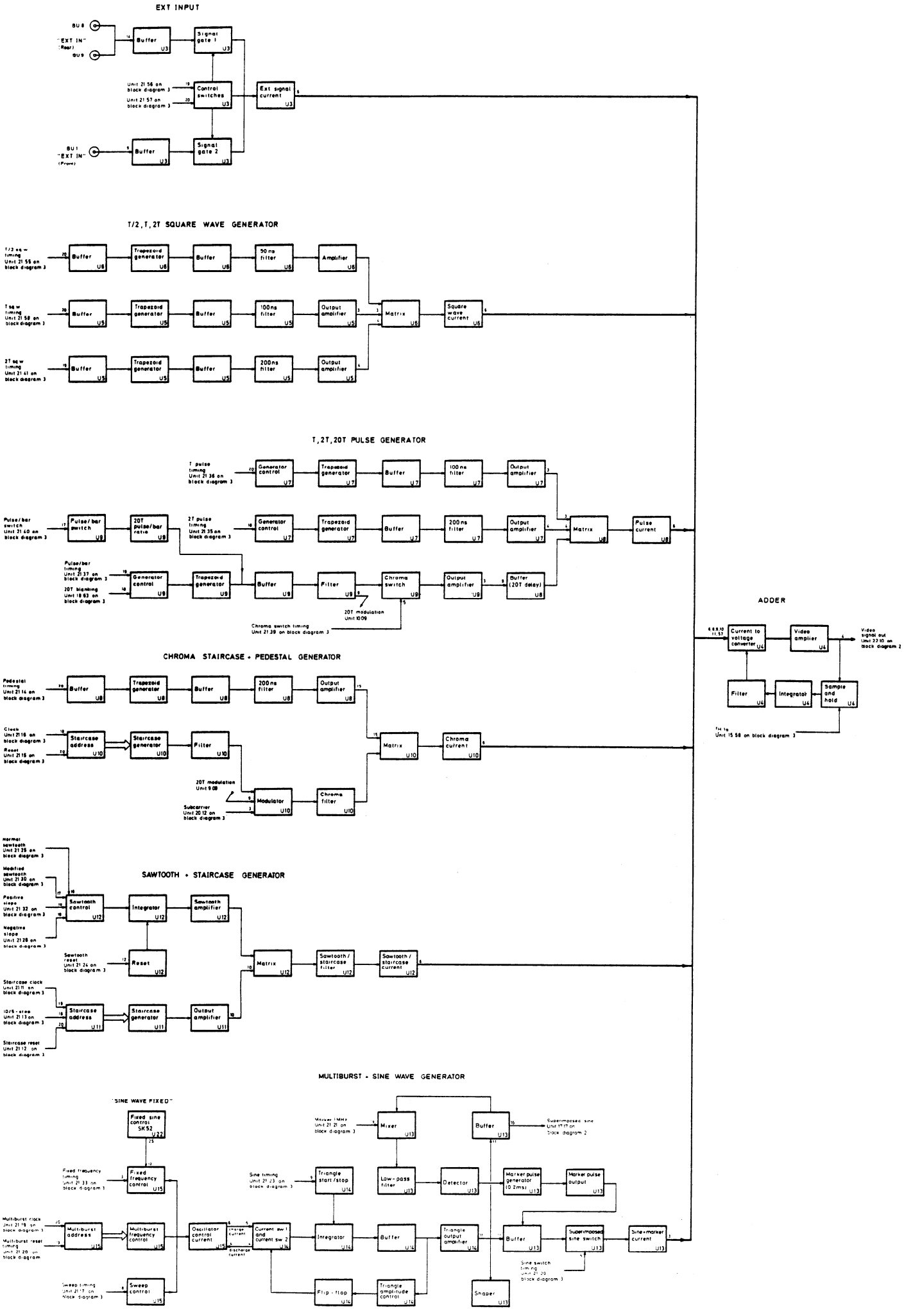

Fig. 7-2 Detailed block diagram I

B. Signal processing

The video test signal is applied via a buffer to the video level control P2/SK44. By means of this control the video amplitude can be set to some fixed levels or switched off by SK44. P2 allows a continuously variable adjustment of the amplitude.
From P2/SK44 the video signal is led to a "Matrix", where sync, set-up, and burst are added.
The applied sync signal (from block diagram 3) is fed to the sync amplitude control P4/SK46. The output from this control is then converted to a current which is added to the outputs from the set-up generators and the CW set-up current generators.
The set-up control P3/SK45 makes it possible to choose between a preset set-up level, a negative variable level and a positive variable level, of which the last two are continuously variable by means of P3.
A CW set-up pedestal can be added to an externally applied signal when the "CW" switch is pressed. The CW set-up is controlled by P1/SK43, where SK43 has positions for a 50% white level and a jump facility between two preset levels. The two preset levels can also be chosen as steady levels. Finally, the CW set-up level can be set by means of the potentiometer P1.
The CW set-up jump control funtion is also used as a "Sweep start out" signal (terminal BU6).
The current outputs from the sync, the set-up, and the CW set-up generators are then added and applied to the "Matrix" via a 230ns filter.
The last signal to the "Matrix" is the burst signal. This signal is derived as follows:
The subcarrier is led to the "Modulator" via two 45° phase shift circuits and a "Switch". The "Switch" funtion is controlled by PAL identification pulses. The subcarrier from the "Switch" is led to the "Modulator", which again is controlled by burst key pulses. The burst output from the "Modulator" is via a filter and two amplifier stages applied to the burst level control P5/SK47. This control can either switch off the signal, or introduce a nominal burst level, or a continuously variable level, (by means of P5). It is also possible to choose between an alternating burst and a non-alternating burst (by SK47).
The burst signal is then fed to the "Matrix" via a buffer.
The matrix output is a composite video signal which via a buffer is applied to a level control "COMP VIDEO" P6/SK48. By means of this control it is possible to choose between four fixed levels and a continuously variable composite video level. The "COMP VIDEO" control is followed by some amplifier stages with a clamp circuit in between to ensure the right dc level of the composite video signal.
This signal is then led to a buffer stage where also the ITS signal is applied. The ITS signal is led separately from the input terminal to the buffer stage via two ITS amplifier stages with an ITS clamp circuit and an ITS switch. This means that the ITS signal is completely unaffected by the controls mentioned above.
Before entering the output amplifier with its three output terminals, the signal passes another matrix and a filter. In this matrix the composite video signal and the ITS signal can be superimposed with some well specified signals.

The superimposition part consists in principle of three signal generators, where all outputs are completely unaffected by the composite video level control.

The hum signal derives from the mains and is applied to the "HUM/SUP" level control P9/SK51. An external superimposition signal is also fed to P9/SK51 via an input amplifier. This level control makes it possible to chose between hum (fixed level or continuously variable) and an externally applied superimposition signal. When an external signal is used, the amplitude of this signal is also adjustable by P9 before entering the matrix.

The noise generator comprises a noise source and two amplifier stages followed by a "NOISE" attenuator P8/SK50. The switch SK50 has five positions, one of which is used to switch off the noise, and the other four to attenuate the noise in 10 dB steps. In addition, these noise levels are adjustable from 0 to - 10 dB of the selected level by means of P8.
The noise signal from P8 is then passed over to the matrix via an amplifier.

The subcarrier/sine wave signal is obtained quite differently. The subcarrier is fed to the "Modulator", which is controlled by timing pulses from the control unit. Via a filter the signal is then led to the "Matrix", where it is added to the sine wave signal.
The sine wave signal derives from the "Sine wave generator" (see block diagram I) and has access to the matrix via the "Sine switch". The switch is also controlled by timing pulses from the control unit.
The subcarrier/sine wave output from the matrix is applied to the "SUBC/SINE" control P7/SK49 via two amplifiers. SK49 has three positions with fixed levels and one position where the level is continuously adjustable by means of P7.
In the following matrix all superimposition signals are added together and led to the last matrix, where the superimposition takes place.
The composite video signal as well as the superimposed signals are then applied to the three output terminals.

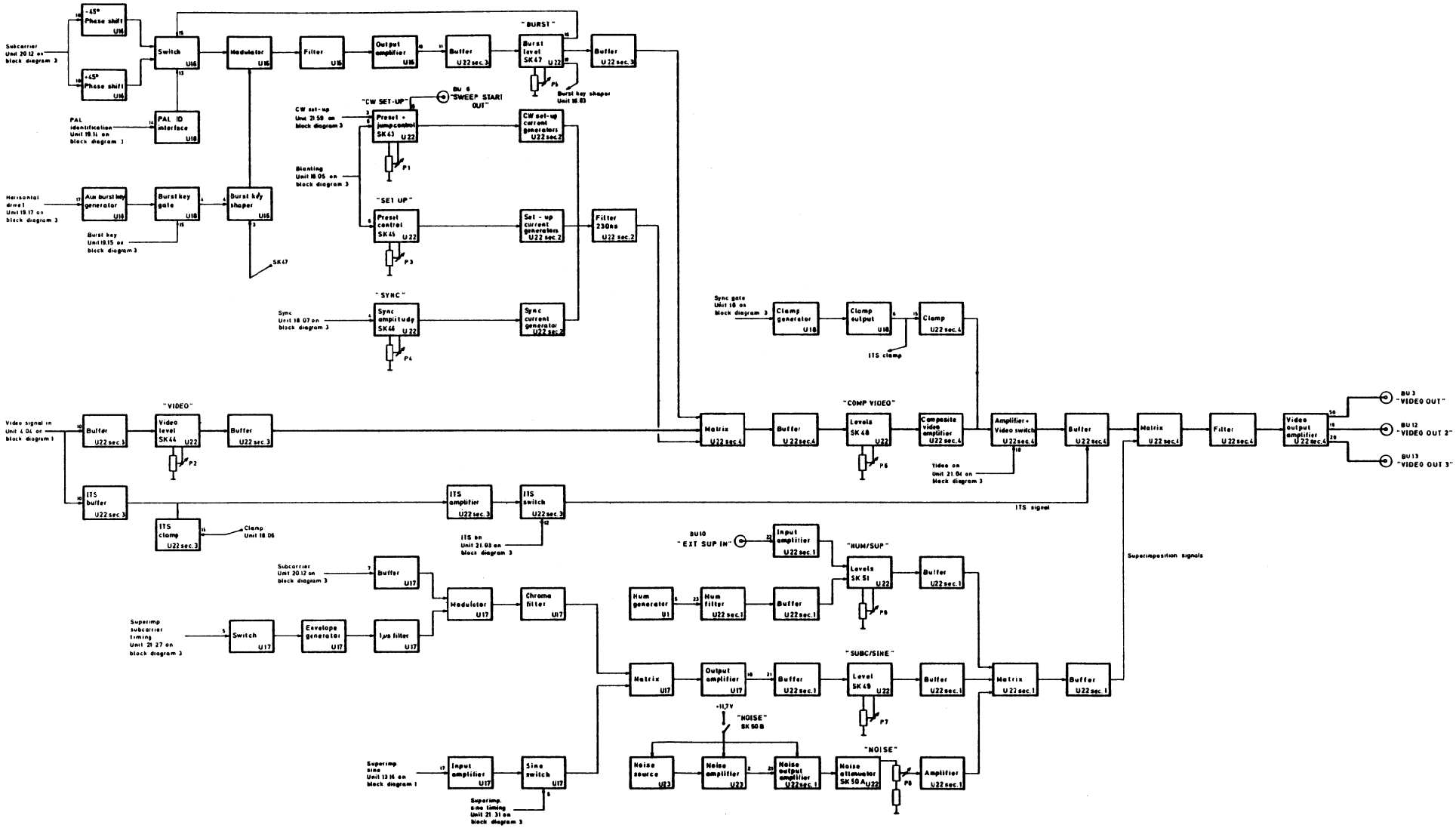

Fig. 7-3 Detailed block diagram II

C. Control section

All necessary control and timing pulses as well as sync and subcarrier signals are generated in this section.

The main function switches SK2 to SK20 are used to select the desired video test signal as follows:
When for instance SK18 ("SINE WAVE" sweep) is pressed, this event will be detected and converted into binary information by the encoder (diode matrix). The binary information is applied to the "Main function memory", where it is stored. Similarly, remotely applied binary information can also be used. (Optional).
The memory output is then converted back to decimal form and led to the lamp drivers. (lamp LA18 lights). The same information is also fed to the "Generator control". Here the control and timing pulses for the sine wave generator (block diagram 1) are generated and applied to the generator circuitry.
The timing information derives from a "horizontal divider" driven by a 1 MHz colck pulse. The counter divides the lines into 64 intervals (1 µs each), and the following "Time decoding" and "Timing latches" circuits contain information about the position of every single element.
Moreover, the "Generator control" gets information about some sub-functions from the switches SK31, 33, 35, 39, 40, and SK41; in the chosen example (that of the sine wave sweep), it is possible to add a marker information to the sweep signal by pressing the push-button SK41.
In addition a jump generator is introduced. This generator is also controlled by information from the "Main function memory" and the sub-function switches. The purpose of this generator is to enable the "Generator control" to activate or stop some of the test signal generators in a fixed sequence. This is used when for instance a white or black level signal and a sawtooth or staircase signal form the duty signals (alternating 3 lines steady level and 1 line sawtooth or staircase).
The square wave timing pulses are derived from the "Square wave + window generator", which is controlled by the "Main function memory". The sub-function switches SK27, SK28, and SK29 make it possible to choose between three different rise times for the square wave signals.

Finally the "PULSE & BAR" sub-function switches are located here. By means of SK30 and SK31 a choice between a T-pulse and a 2T-pulse can be made. When SK32 is pressed, the chosen bar of the pulse-and-bar-signal is gated together with an f_V square wave pulse. The result is that the bar signal is visible in part of the field period only.

The PM 5570 has its own standard sync pulse generator which can be genlocked to an external composite video- or black burst signal.

The sync generator consists in principle of two integrated circuits (the sync circuit and the genlock sircuit) with some interface circuitry.
When a composite video signal is applied to BU4 or BU5,it passes a buffer stage before entering the "Sync level detector". Superimposed hum is also removed and the dc level is clamped to zero. In the 50% clipper stage the sync signal is sliced at the 50% level and led to the "Genlock" circuit.
The "Genlock" output controls an oscillator, which gives two different frequencies -5 MHz and 2.5 MHz. The 5 MHz signal is led to the "Line-clock divider", where it is divided by five and used to derive the timing information. The ITS timing information is derived from the f_H and f_V pulses.
The 2.5 MHz signal is fed to the sync generator in which the standard sync signals are derived from three one-shot generators, (the aux burst key generator is located on block diagram 2). The signals from the gates are then applied to the "Input logic" circuit as well as to some amplifiers, from where the "SYNC OUT" and "TRIG OUT" is obtained.

The subcarrier generator consists of a TCXO, which may be synchronized externally, a "Limiter" and an "Output amplifier". The subcarrier is fed from the TCXO via the "Limiter" and the "Output amplifier 1" to BU7 "SUBC OUT". The "Limiter" also delivers a subcarrier to "Output amplifier 2", from where the output is applied to the "Genlock" circuitry to obtain correct relationship between subcarrier and sync frequencies (internal mode only).
The chroma content of a composite video signal applied to BU4 or BU5 "SYNCHR IN" is taken off from the "Buffer" stage and led to the "Burst gate" via an amplifier. This burst gate is controlled by burst key pulses from the sync generator. The presence of the burst keeps the "Int/ext switch" on (via the "Burst detector"), unless SK21 "SYNCHR INT" is activated.
The "Burst gate" output and the subcarrier signal from "Output amplifier 2" are then conbined in the "Demodulator". Via the "Sample and hold" circuit, also controlled by burst key pulses, the demodulated output is applied to the "Low-pass" circuit.
The signal from this circuit is passed to the oscillator via the "Int/ext switch".

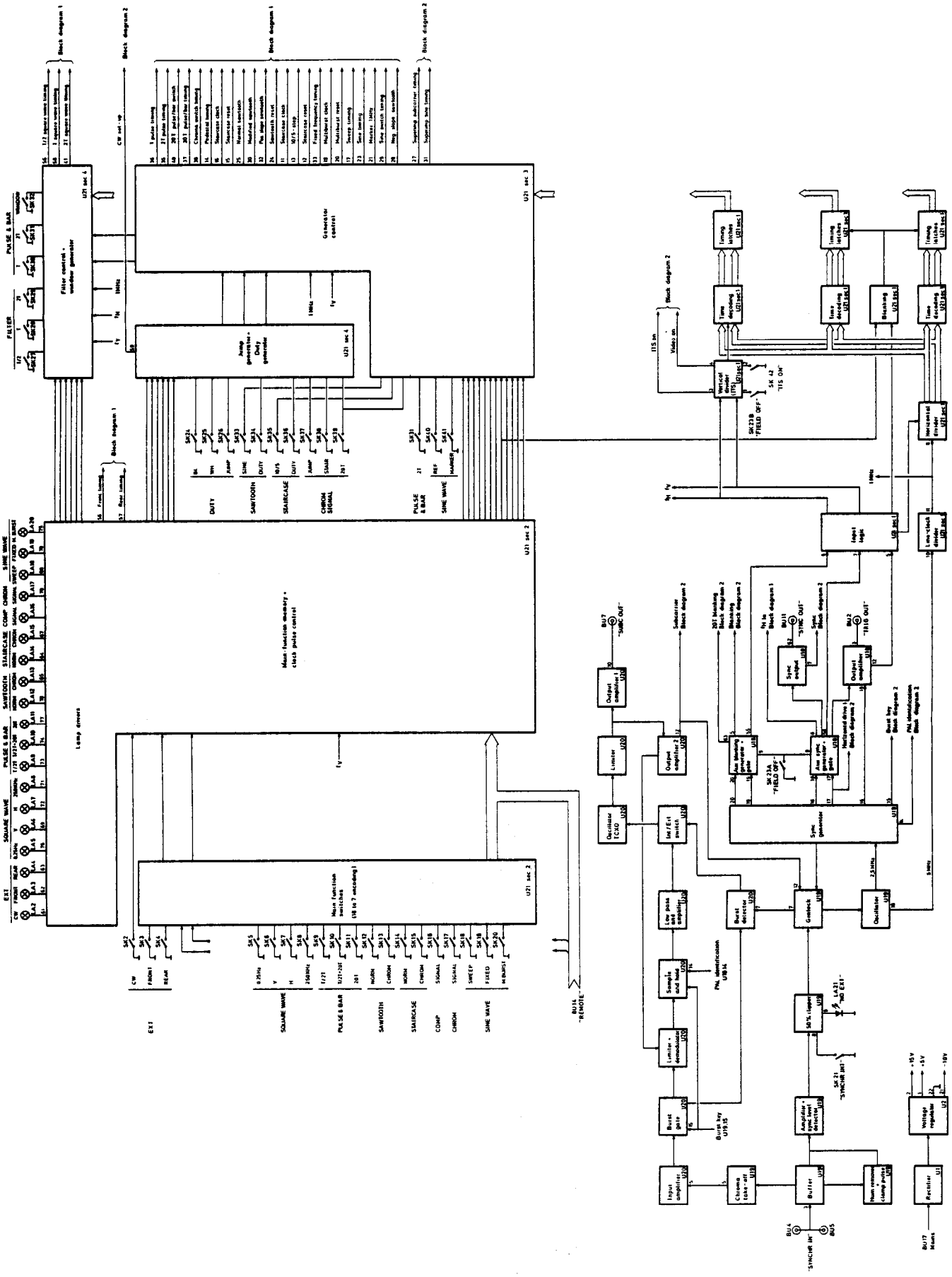

Fig. 7-4 Detailed block diagram III

10. Unit 3 External input

This unit consists of two similarly designed input amplifiers - with associated signal gates and switches - and a current output stage.

Circuit description

In the inactive mode both amplifiers are disabled by means of the transistors TS4 and TS13 respectively which are saturated, while the signal gates 1 and 2 (TS5, TS14) are cut-off. At the same time switch 3 (TS7, TS8) is ON, causing a quiescent current at about 4.5mA in the output transistor TS16.

Considering the case where a signal applied to "BU1" has access to the output amplifier, a logical "high" level is applied to terminal 19. After being inverted in IC1/4 this command signal activates switch 2, which again reverses TS13 to be cut off and TS14 to be saturated. The command signal from IC1/4 is via IC1/2 also used to set switch 3 in the cut-off state, which means that the quiescent current in the output transistor TS16 is now controlled by the buffer amplifier TS11, TS12.
The externally applied video signal at "BU1" is amplified in TS10 and led to the buffer amplifier TS11, TS12, thus causing a current sink in the output amplifier according to the applied video signal.

The output information (terminal 6) is then led to the "Signal adder" unit 4, where all signals from the various signal generators are combined.

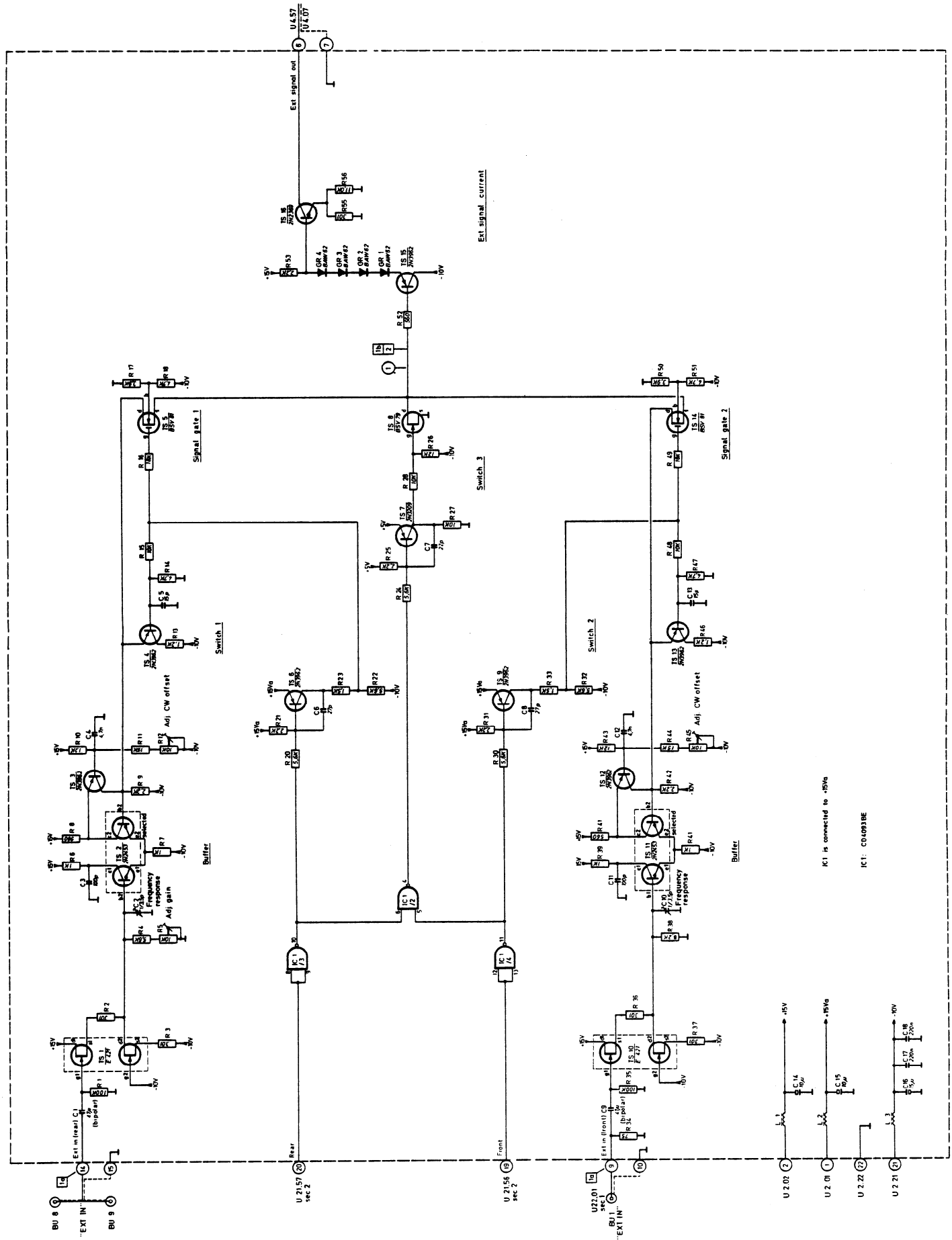

Fig. 10-6 Circuit diagram, external input, unit 3/02

11. Unit 4 Signal adder

The various test signal elements are added in this unit, which in series 01 consists of a combined current to voltage converter/video amplifier and a correction circuit.

In series 02, the unit has a separate current to voltage converter and a video amplifier as well as a correction circuit. In addition, the voltage +15Vc is replaced by a regulated +12V supply.

Circuit description

The various test signal elements are added in this circuit and applied to the first stage, which in the 01 series is a combined current to voltage converter/video amplifier TS1 - TS4, the dc output level of which is kept constant by the built-in correction circuit.

The current supply, required for the various signal generator output stages, is obtained partly by TS1, R2, R28 and partly by TS5, R12, where TS5 performs the output stage of the correction circuit, which also comprises a "Sample and hold" circuit, an "Integrator" and a "Filter".
The current flow in TS5 is determined by the dc level of the hold capacitor, which via the "Integrator" and the "Filter" controls the base current in TS5. The dc level of the hold capacitor is the dc output level of the video amplifier, which is sensed, transferred and stored by the "Sample and hold" circuit during the line sync period.
Assuming that the current sink at the input is decreased, the dc output level of the "Video amplifier" will be negative, and consequently the correction circuit responds with a decreased current in TS5 to correct the dc off-set of the "Video amplifier".
The video output signal is then, via terminal 4, passed over to unit 22 for the final processing.

As mentioned earlier the "Current to voltage converter" TS1 - TS4 and the "Video amplifier" TS5 - TS9 are separated in series 02, while the correction circuit TS10 - TS12 is similar to the correction circuit in series 01.
The function of the entire unit is as described above and needs no further explanation.

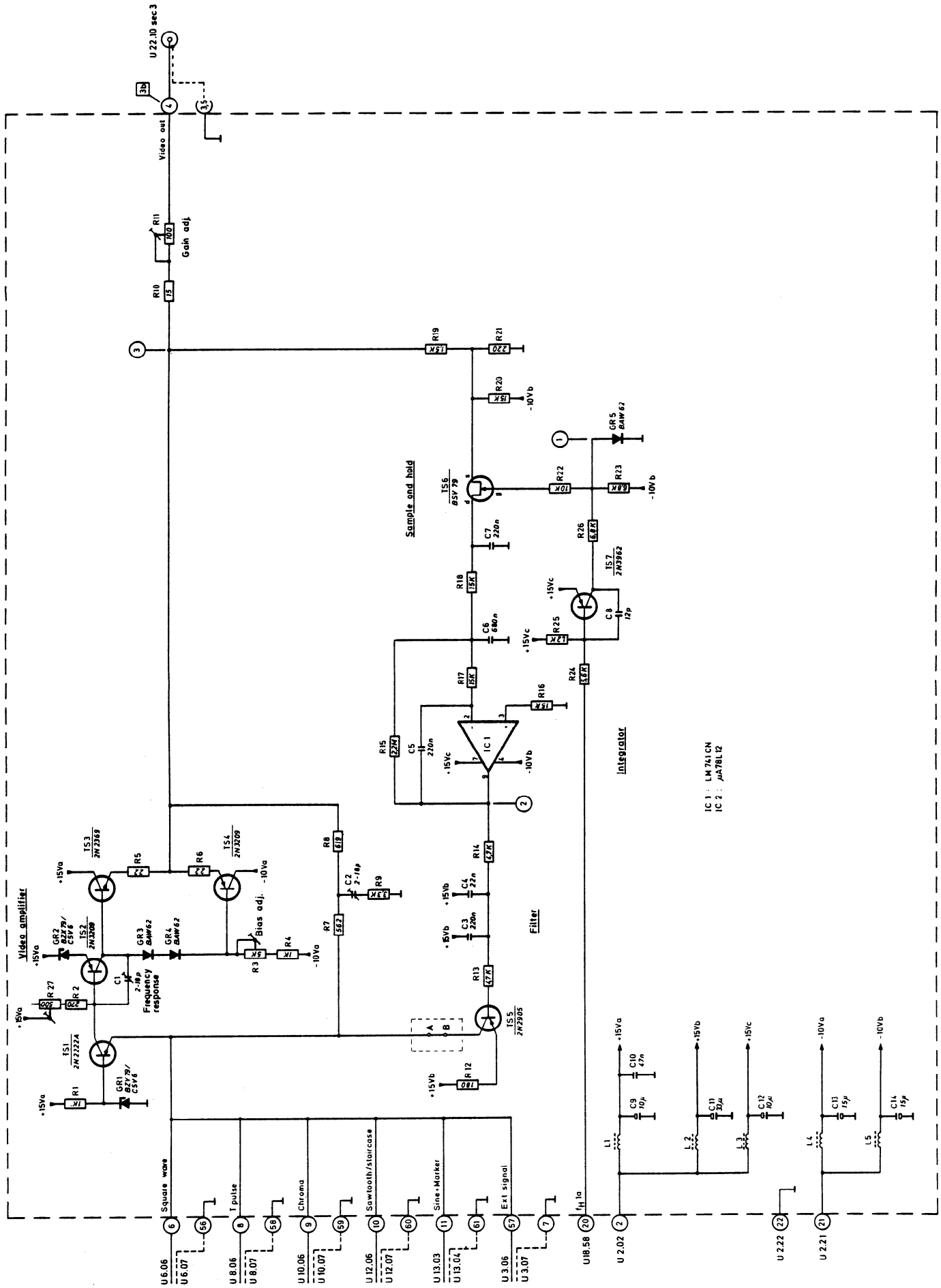

Fig. 11-3 Circuit diagram, signal adder, unit 4/KF6xx

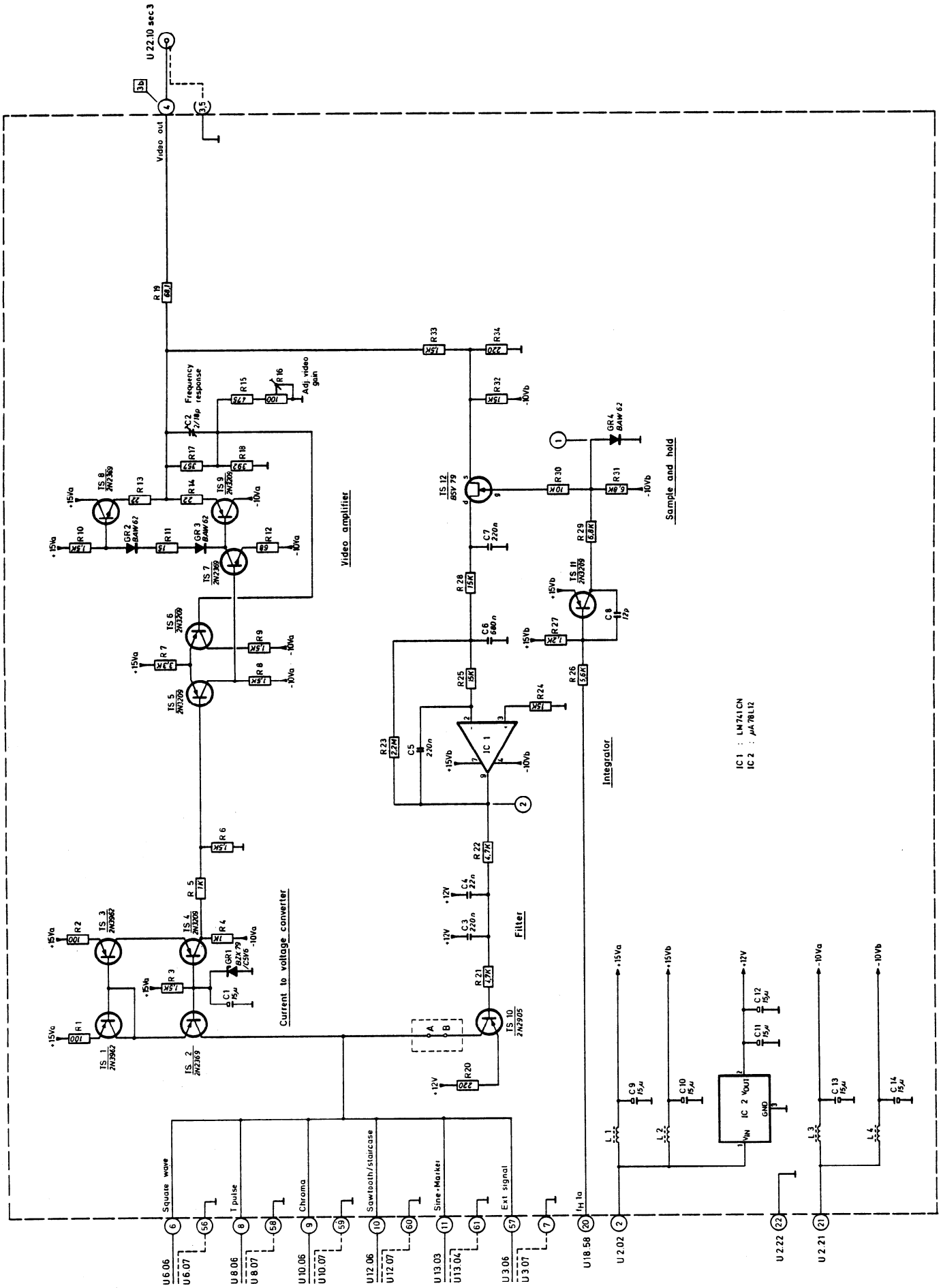

Fig. 11-7 Circuit diagram, signal adder, unit 4/02

12. Unit 5 T-2T Square wave

This unit produces two square wave signals with a rise/fall time corresponding to the T pulse and the 2T pulse respectively, and where the frequencies are determined by switches on the front panel.

Basically the unit contains two trapezoid generators, each of them are followed by a buffer, a filter, and an output amplifier. As the two generator circuits are almost identical, only one of them is described here.

Circuit description

The 2T square wave timing - applied to terminal 19 - controls the trapezoid generator, which consists of the constant current generator IC2, TS13, the capacitor C4 and the transistors TS11, TS12 and TS14, TS15. In the quiescent state TS11 and TS15 are cut off, while TS12 is saturated. This means that a constant current flows through TS12, TS13, and the capacitor C4 is kept discharged.
When the trapezoid generator is sequentially activated by the timing signal - via TS10 - the generator shifts in turn between two states; first by saturating the transistors TS11 and TS15, it causes C4 to be charged to about +6V (GR4 clamps to +5V), and secondly it discharges C4 via TS12 and TS13.
The resultant square wave signal from the trapezoid generator is then buffered by TS16, TS17 and shaped in the filter circuit L2, C5, C6.

Finally the square wave signal, which now has a well defined rise/fall time, is adjusted to a proper amplitude by R37 (TS18) before being passed along to the square wave pulse matrix on unit 6.

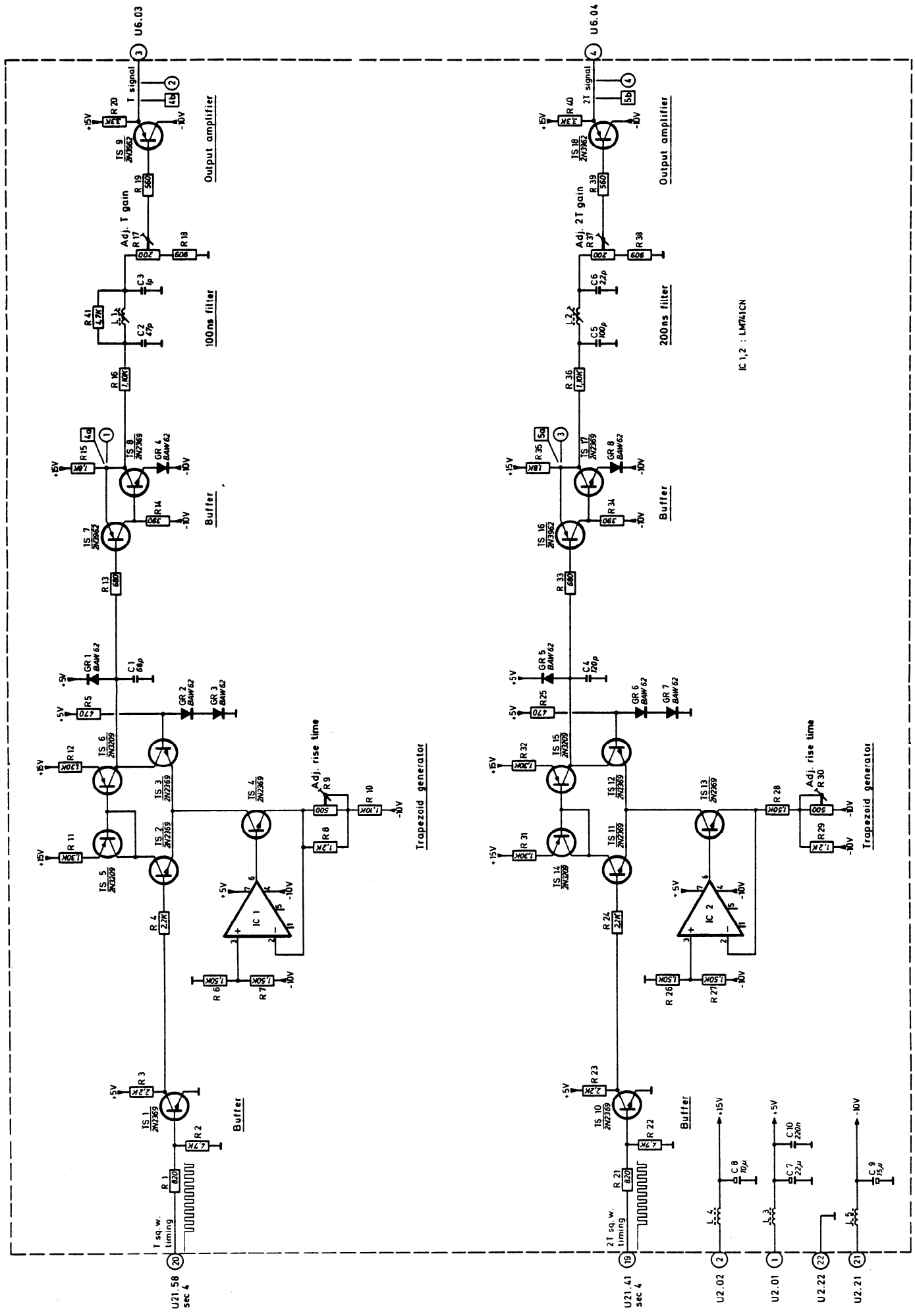

Fig. 12-4 Circuit diagram, T-2T square wave, unit 5

14. Unit 7 T-2T Pulse generator

Whenever either a T pulse or a 2T pulse is to be used, one of the two generators - located on this unit - will be activated.

Essentially the unit consists of two similarly arranged trapezoid generators with associated control circuits as well as two filters and two output amplifiers.

Circuit description

In the case when the 2T pulse is desired in a specific test signal, the generator control IC1-13 is triggered by a timing pulse applied from unit 21.
The generator control is a one-shot generator, where the one-shot time determines the pulse duration as shown in fig. 14-1.

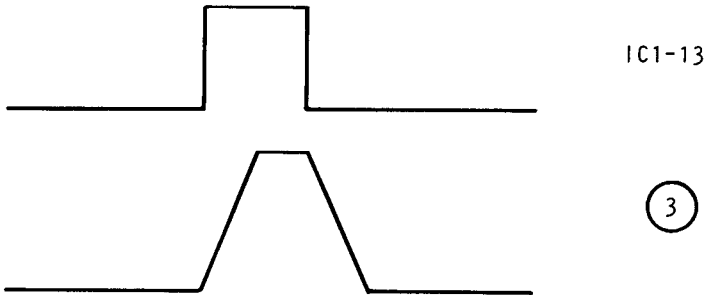

Fig. 14-1 2T pulse duration

In the quiescent state TS10 and TS15 are cut off, while TS11 is saturated. This means that a constant current flows through TS13, and the capacitor C7 is kept discharged. When triggered, the Q output from the generator control is "high", and this "high" level forces the transistors TS10 and TS15 to be saturated. Consequently, the capacitor C7 will be charged via R24 and TS15 to about +6V (GR5 clamps to +5V).
When the one-shot time expires, the Q output shifts to "low" again, and the capacitor C7 is now discharged via TS11, TS13, R27, R28. The trapezoid waveform is shown in fig. 14-2, where t_2 is about equal to two times t_1.

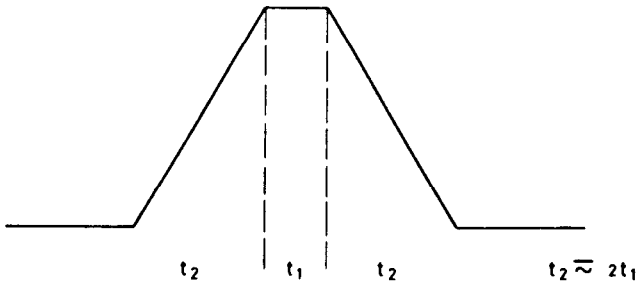

Fig. 14-2 Pulse diagram of the trapezoid waveform

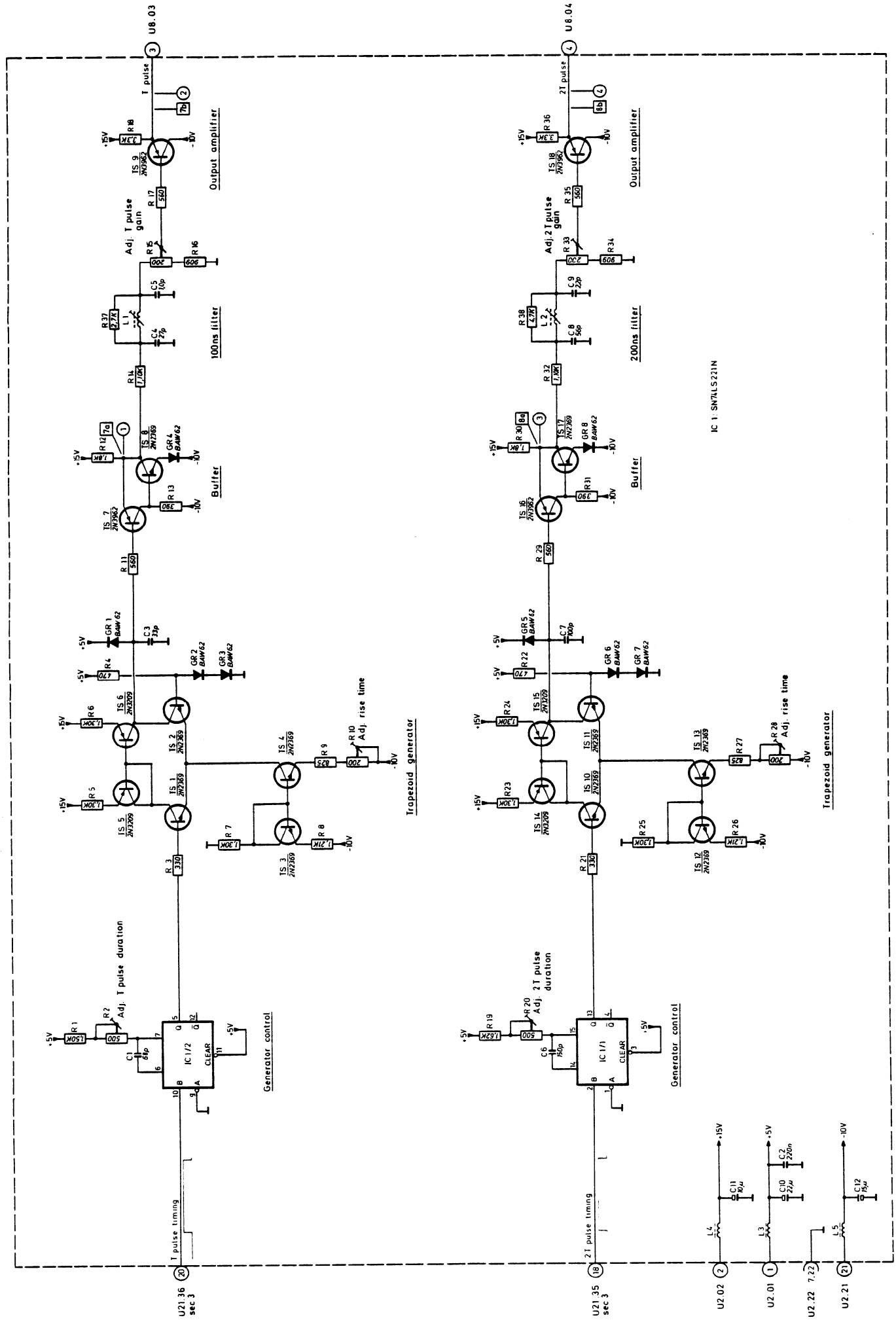

Fig. 14-8 Circuit diagram, T-2T pulse generator, unit 7

16. Unit 9 20T Pulse and bar

This unit produces the curvature of the 20T pulse as well as the 20T bar (see fig. 16-1). It consists of a trapezoid generator which is controlled by a generator control circuit. The generator is followed by a buffer stage and a filter circuit from where the pulses are passed over to the chroma modulator on unit 10, while the chroma swith allows only the 20T pulse part of the two signals to be passed along to the T pulse matrix on unit 8.

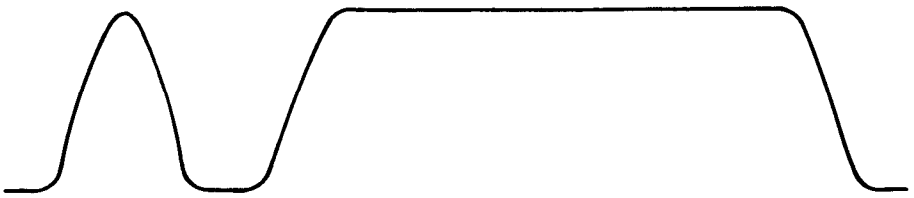

Fig. 16-1 20T pulse and 20T bar

Circuit description

When the 20T pulse form is desired in a specific test signal, the generator control circuit IC1, IC2 is triggered by a timing pulse applied by unit 21. The generator control consists of a one-shot generator and two NAND-gates, where the one-shot time determines the pulse duration as shown in fig. 16-2.

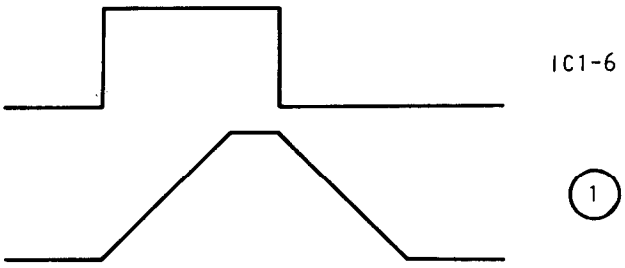

Fig. 16-2 20T pulse duration

In the quiescent state TS4 and TS5 are cut off, while TS6 is saturated, keeping C3 discharged via the constant current generator TS7, TS8. When the one-shot generator is triggered, the output from IC1-6 shifts to "high" and forces the transistors TS4 and TS5 to be saturated. Consequently, the capacitor C3 will be charged via R12 and TS4. When the one-shot time expires, the output from IC1-6 shifts to "low" again, and C3 is now discharged via TS6, TS8, R16, R17.
The trapezoid waveform is shown in fig. 16-3, in which t_2 is about equal to two times t_1.

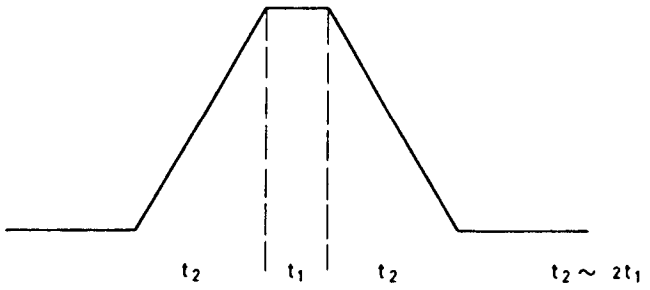

Fig. 16-3 Pulse diagram of the trapezoid wave form

In the case when both the pulse signal and the bar signal are required, the generator control works as shown in fig. 16-4.

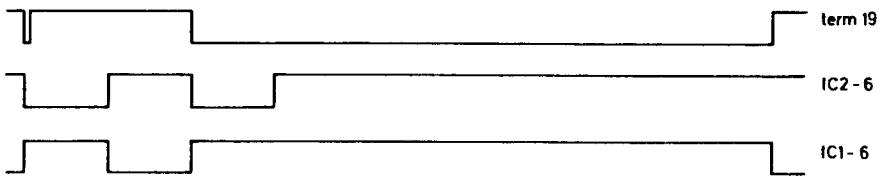

Fig. 16-4 20T pulse and bar control pulses

In addition a difference in the rise/fall time of the two signals are obtained by adding C4//C5 parallelly to C3 when the bar signal is to be produced. This is done by means of the pulse/bar switch TS1, which, controlled by unit 21 (via terminal 17), brings TS9 in the conducting state.
However, the pulse/bar switch also determines the clamp level for the 20T pulse in such a way that when not activated, the input level at IC3-3 is adjustable between +5V to +6V by P7, and consequently the voltage of C3 is somewhere around +6V and +7V. But when the pulse/bar switch is activated - in the bar mode - TS2 is saturated and the input level at IC3-3 is now +5V, which gives a maximum voltage on C3//C4//C5 at about +6V. The resultant pulses are then buffered by TS11A, TS12 and shaped in the filter circuit L1, C6, C7, before they are passed along to unit 10 (via terminal 9) where they activate the chrominance modulator.
The same information is also passed to the chroma switch IC4, via the 20T pulse gain potentiometer R25, and when this chroma switch is enabled (terminal 5 is "high" when the luminance part of the 20T pulse is required) the 20T pulse is applied to the T pulse matrix on unit 8.
In order to coincide with the chroma part of the 20T pulse, derived from the chrominance modulator on unit 10, the luminance part of the 20T pulse is delayed on unit 8, before it is applied to the T pulse matrix.

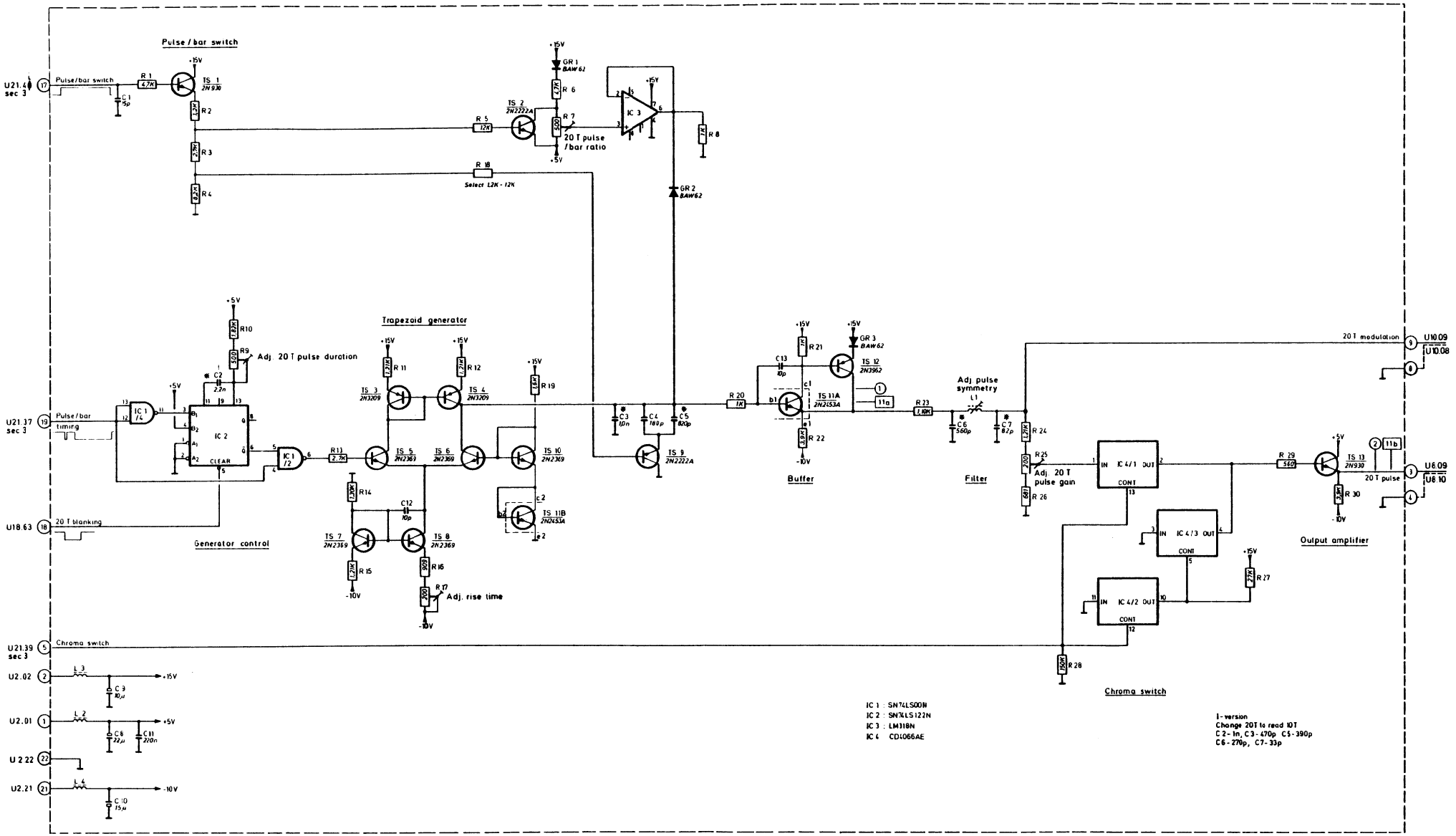

Fig. 16-10 Circuit diagram, 20T pulse and bar, unit 9

17. Unit 10 Chroma staircase

The chroma information required for some of the test signals as well as the 5 riser chroma staircase are produced here, while the 50% luminance pedestal for these chroma test signals is supplied by unit 8.

Circuit description

Basically the circuit consists of a modulator from which an applied subcarrier (term 3) under certain conditions, has access to the following filter, matrix and output stage. The modulator mentioned is a double balanced modulator, where the chroma output amplitude is proportional to the dc level of the two X-inputs.

In the case when the 20T modulation signal from unit 9 is applied to the modulator, a chroma signal similar to the 20T modulation signal is present at the modulator output, pin 6. The chroma signal is, via TS11 and the filter, passed along to the matrix circuit. When the 50% luminance pedestal is required together with the chroma signal, the pedestal signal, derived from unit 8, is also applied to the matrix. The matrix output is led to the chroma current stage TS8, TS9, TS10, which is a voltage to current converter.
The current output signal is then led to the "Signal adder" unit 4 to be combined with the signals generated by the various signal generators.

The chroma staircase generator consists of five current generators TS2 to TS6, a common resistor R23, and a generator control IC1/1, IC1/2.
Each of the current generators delivers a current flow in R23, and this enables a dc voltage to be built up across R23, where the dc level is proportional to the number of generators activated.
The current generators are all controlled by the generator control IC1/2, which consists of two static shift registers. These registers are clocked and reset by the control unit via the terminals 19 and 20.
When the generator control now activates current generator TS2, the resulting dc level across R23 controls a chroma signal from the modulator, pin 6 (first step of the staircase). The next clock pulse steps the generator control one step forwards, thus activating the current generator TS3 which also delivers a current through R23. The dc level across R23 is now the sum of the two currents multiplied by the resistor value. Consequently this new dc level means that the chroma signal from the modulator has a higher amplitude (second step of the staircase). The third, the fourth, and the fifth steps are similarly obtained by an addition of the current flow from one or more of the remaining generators to the already existing current flow in the common resistor R23.
A filter circuit is inserted between R23 and the modulator IC2 to obtain a right shape, and the entire dc level of the staircase is adjusted with R25.

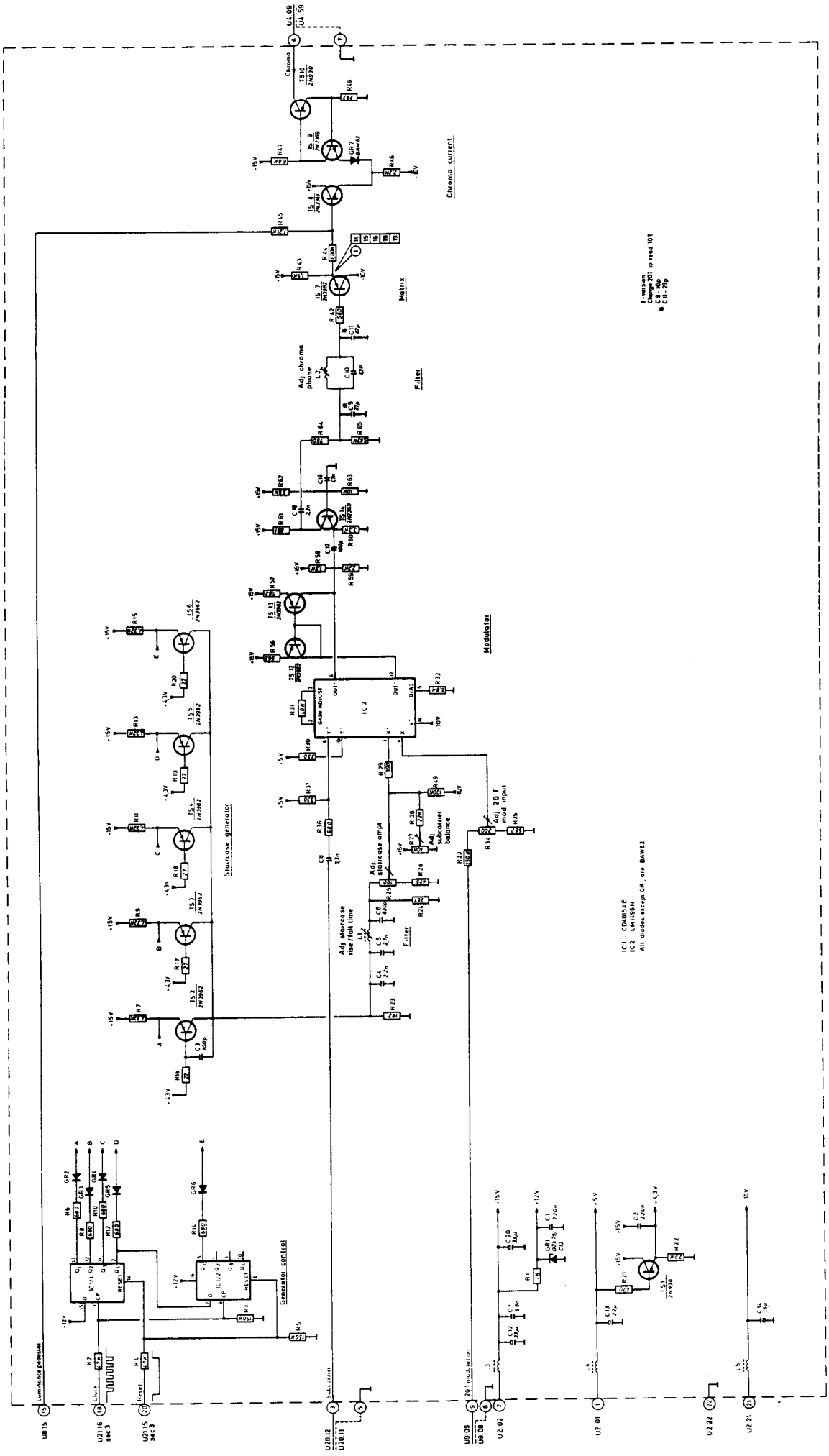

Fig. 17-9 Circuit diagram, chroma staircase, unit 10/02

18. Unit 11 Staircase generator

Two different staircase signals are produced by this unit, which mainly consists of a staircase generator and a staircase address circuit.

Circuit description

The staircase generator consists in principle of ten independent current generators TS1 to TS10 and a common resistor R42//R43 + R44 followed by an output amplifier TS11. Each current generator contributes with 10% of the maximum current flow in the common resistor.

Assuming a 10 step staircase signal to be provided, current generator TS1 is activated which produces a dc level across the common resistor network. This dc level indicates the first staircase level (10%), and it is via the output amplifier TS11 passed along to unit 12 where a further processing takes place. The second staircase level (20%) is obtained by activating TS2 as well as TS1, thus I(TS1) + I(TS2) x R42//R43 + R44 makes the dc level of the second step.
Each of the following steps are then made by adding one more current generator to the generators already employed.

The entire function of the staircase generator is controlled by the staircase address circuit, which consists of three shift registers IC1, IC2, IC3. The function of these registers is controlled by command pulses from unit 21. In the ten step staircase mode terminal 18 is "0", and the staircase address acts as a serial shift register which activates one more current generator for each staircase clock received from the control unit (terminal 19).

In the five step mode terminal 18 is "1", and the staircase address works as a parallel shift register. In this mode each staircase clock pulse causes the staircase address to employ two more current generators, which means that the first staircase level is 20% of the maximum dc level, the second level is 40%, and so on. At the same time, the staircase clock frequency from the control unit (terminal 19) is only half the frequency to extend the duration of the five step staircase signal to be similar to the ten step staircase signal.
When the five step staircase is to be used in the composite signal, the clock frequency is the same as in the ten step staircase signal.

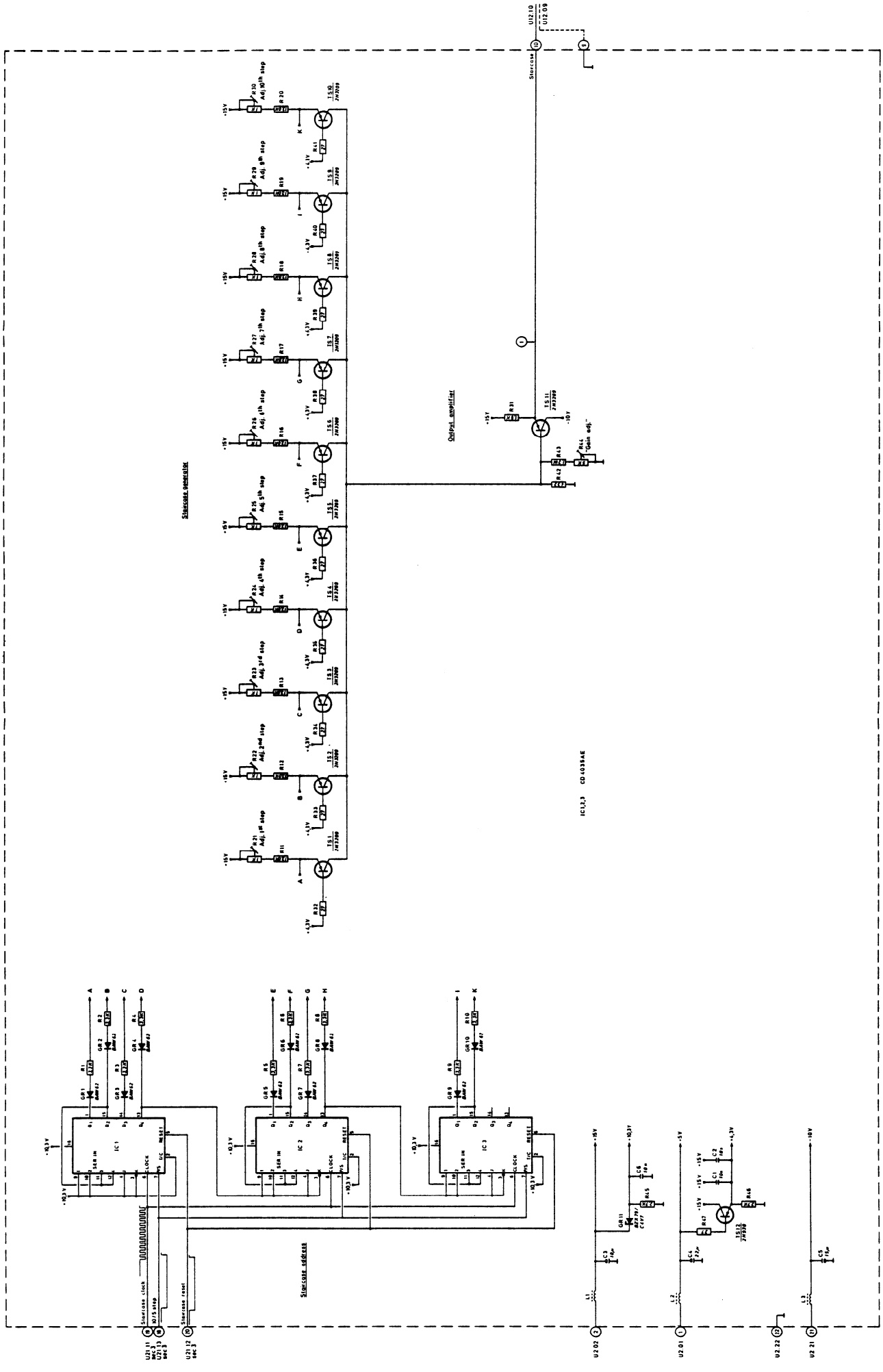

Fig. 18-3 Circuit diagram, staircase generator, unit 11

19. Unit 12 Sawtooth generator

Three different sawtooth signals are generated and processed in this unit.
The staircase signals from unit 11 are also processed here before they are applied to the "Signal adder" unit 4.

Circuit description

Basically the sawtooth generator consists of four current generators TS1 to TS4 and an integrator C1 with associated reset facility. When a normal sawtooth is required the integrator C1 is charged by the current generator TS1, which is held open by a command pulse from unit 21 (via terminal 16). The integrator resetting is cancelled simultaneously (also controlled by unit 21).
The resulting integrator level is amplified by the sawtooth amplifier TS9,TS10 and is passed along to the output stage via the matrix and the filter circuit. In this output stage TS12 to TS14, which has a quiescent current at about 4.5mA, the signal is converted from a voltage level to a current output signal, before it is led to the "Signal adder" unit 4.
The modified sawtooth generator TS2 is activated only when a sawtooth signal superimposed with sine wave is required, while TS3 as well as TS4 to TS6 are involved to make the sawtooth signal with superimposed chroma. The last mentioned sawtooth signal consists of a negative slope (the integrator is charged in negative direction via TS4 to TS6) and a positive slope, which is made by TS3.

The staircase information from unit 11 is applied to the matrix (via terminal 10) from where it is applied to the output stage, via the filter, to be converted to a current output signal and led to the "Signal adder" unit 4.

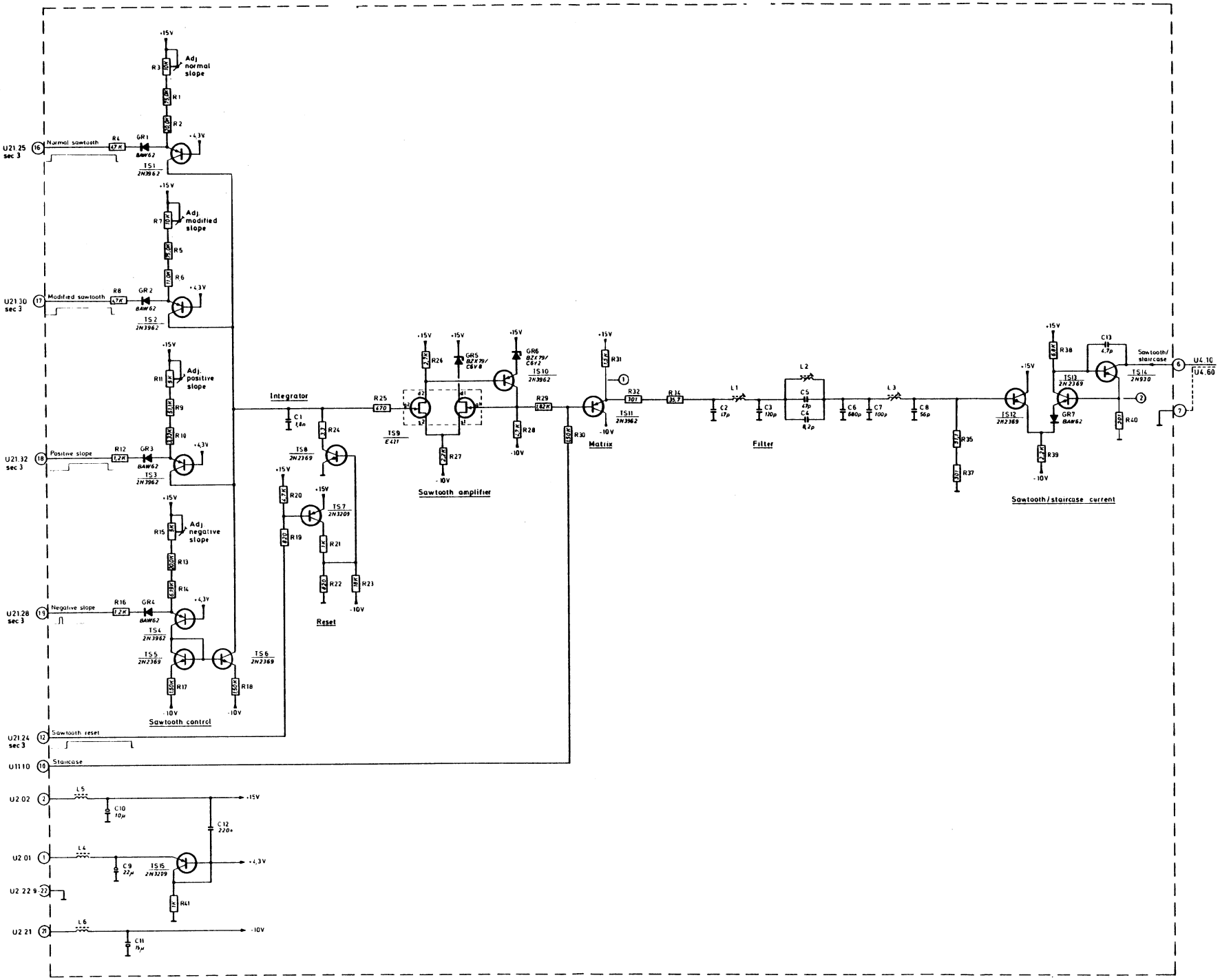

Fig. 19-6 Circuit diagram, sawtooth generator, unit 12

20. Unit 13 Sine shaper + marker

Unit 13 is part of the "MULTIBURST + SINE WAVE GENERATOR" which is accomplished by the units 13, 14, and 15.

The main functions of unit 13 are to convert a triangular wave signal into a sine wave signal, and to generate a marker signal which can be used in the "SINE WAVE SWEEP" mode.

Circuit description

The triangular wave signal, derived from unit 14 and unit 15, is via terminal 11 applied to the sine shaper circuit.
The sine shaper circuit is divided into a positive shaper and a negative shaper, where each shaper part consists of four transistors TS1 to TS4, and TS5 to TS8 respectively. The function of the sine shaper circuit is shown in fig. 20-1, where the influence of the transistors TS2 to TS7 are indicated. TS1 and TS8 act as bias generators for the two shaper parts, the shaping thresholds of which are adjustable by R1 and R12.

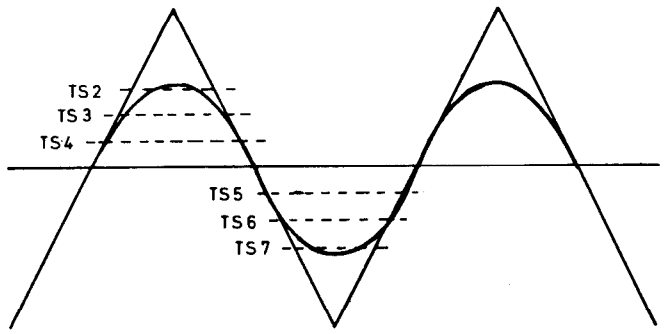

Fig. 20-1 The function of the shaper

The sine wave shaped signal 0.1MHz - 10MHz is then, via the buffer TS13 and the sine switch IC5, passed along to the output stage TS16, TS18, TS19, where it is converted to a current output.
The sine switch IC5 and the output stage TS16, TS18, TS19 are both controlled by the sine switch timing (terminal 5) which is derived from unit 21.

Part of the sine wave signal is via the buffer TS9 used as superimposition signal in unit 17 via terminal 16.

The same sine wave signal is also led to transistor TS10, the emitter of which is connected to the "Mixer" TS11 and TS12. A 1MHz is via terminal 19 applied to the "Mixer" where it is differentiated by C9. The resulting needle-pulses, with a large contents of harmonics, are then mixed with the sine wave signal (TS10, TS11).
The difference frequency between the sine wave signal and the harmonics of the needle pulses is then taken off from TS10, and because of the low-pass filter only a difference frequency lower than 60kHz will be detected by the detector, GR2, GR3, IC3. When a frequency, lower than 60kHz, is detected, the output of IC3 shifts to "high" and initiates the "Marker pulse generator" IC4.
The "Marker pulse generator" is a one-shot generator with a one-shot time at about 0.2ms. This 0.2ms marker pulse is then amplified by TS15 and led to the buffer TS13, where the combination of the sine wave signal and the marker pulse takes place.
The combined signal is, via the sine switch and the output stage, applied to the "Signal adder" circuit, unit 4.

Checking and adjusting

See chapter 31. Common adjustments

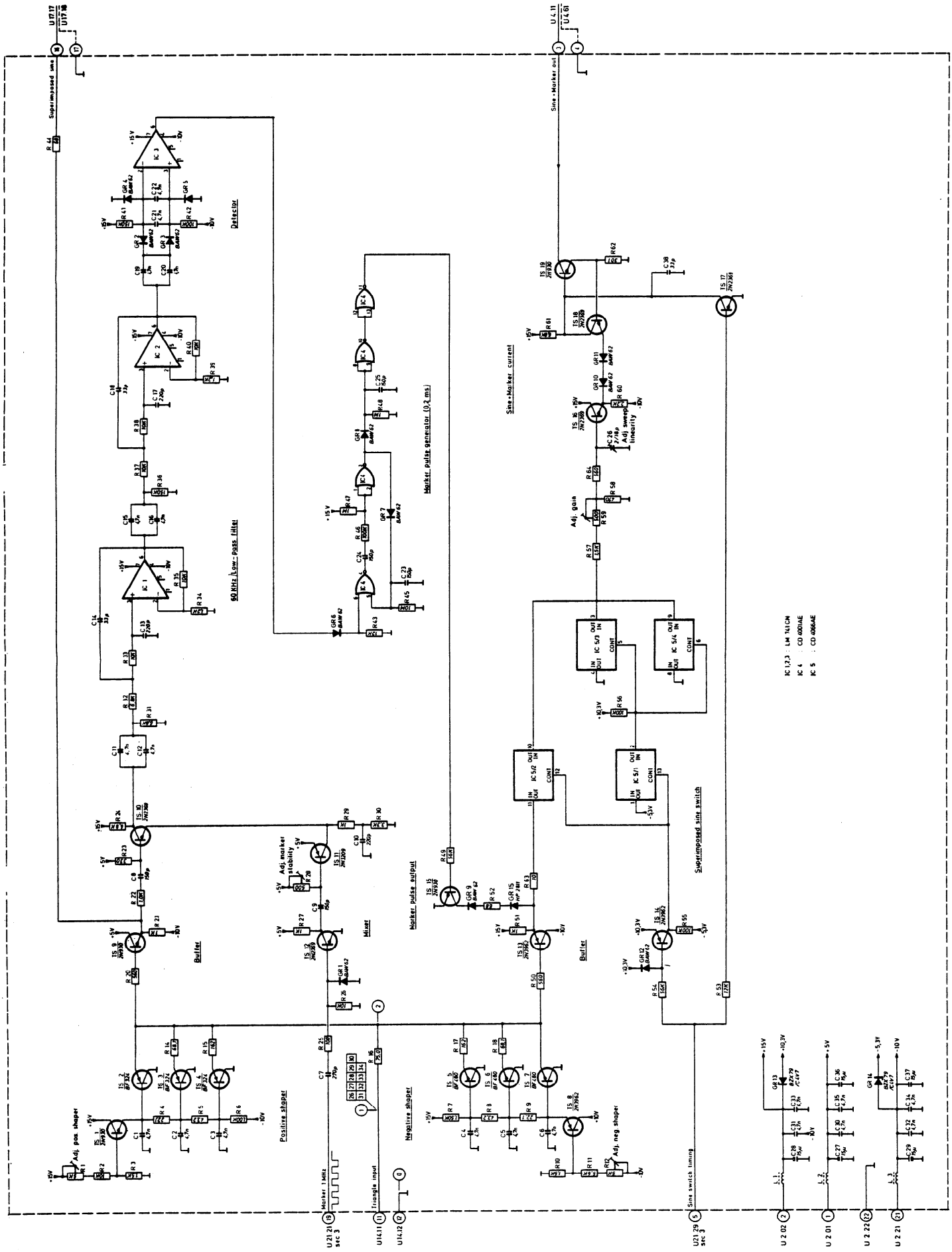

Fig. 20-5 Circuit diagram, sine shaper + marker, unit 13/02

21. Unit 14 Triangle gen. + stop

This unit is the generator part of the "MULTIBURST + SINE WAVE GENERATOR" which is accomplished by the units 13, 14, and 15.

The generator circuit consists mainly of an integrator with associated current switches and a triangle amplitude control, while the control of the generator frequency is carried out by means of unit 15.

Circuit description

In the quiescent state of the generator, capacitor C8 is, via TS4, kept at a steady dc level by IC1. This pre-selected dc level, which is adjustable with R11, determines the zero level of the triangle signal.
When a sine timing pulse appears at terminal 19, TS4 as well as TS7 are cut-off. At the same time the triangle start/stop circuit TS3, TS6, TS5 are shortly reset, which means that no current flows through the tunnel diode GR4, and consequently the current switch 2 is in position OFF.
The charge current which is supplied by unit 15 (via terminal 6) now has access to the integrator C8 via TS8, and C8 will be positively charged. This voltage is passed along to the triangle output amplifier TS18 to TS22 via the buffer TS11 to TS13.
In the buffer stage the voltage is sensed by the triangle amplitude control (TS14 to TS17) which forms two comparators, one of them (TS14, TS15) is preset to a desired positive triangle level, and the other (TS16, TS17) is preset to a negative level. When the preset positive level is reached, a 5mA current flows through R30, TS15, and GR4. The diode GR4 is a tunnel diode which has a characteristic as shown in fig. 21-1, where a 5mA current increase causes the diode to jump from point A to point B.

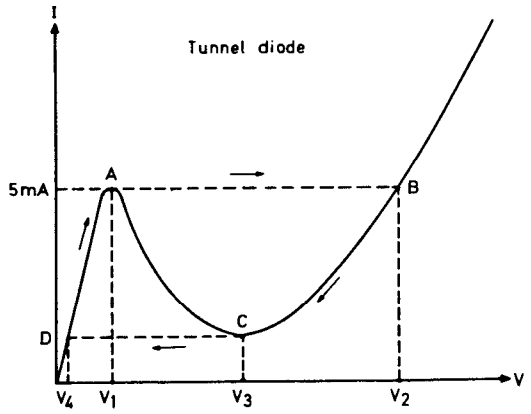

Fig. 21-1 Characteristic of a tunnel diode

This jump means that the voltage across GR4 shifts from V1 to V2, which saturates TS10.

Consequently, the charging current from TS8 as well as the current from the integrator C8 are removed via current switch 2. This state remains until the preset negative level - in the triangle amplitude control - is reached, which causes the current through the tunnel diode to be reduced by TS17.
With a reduced current through GR4, the diode jumps from point C to point D (see fig. 21-1) and current switch 2 is OFF again causing a renewed charging of the integrator C8. The triangle frequency is determined by the charge current and the discharge current, which are controlled by unit 15.

Checking and adjusting

See chapter 31. Common adjustments

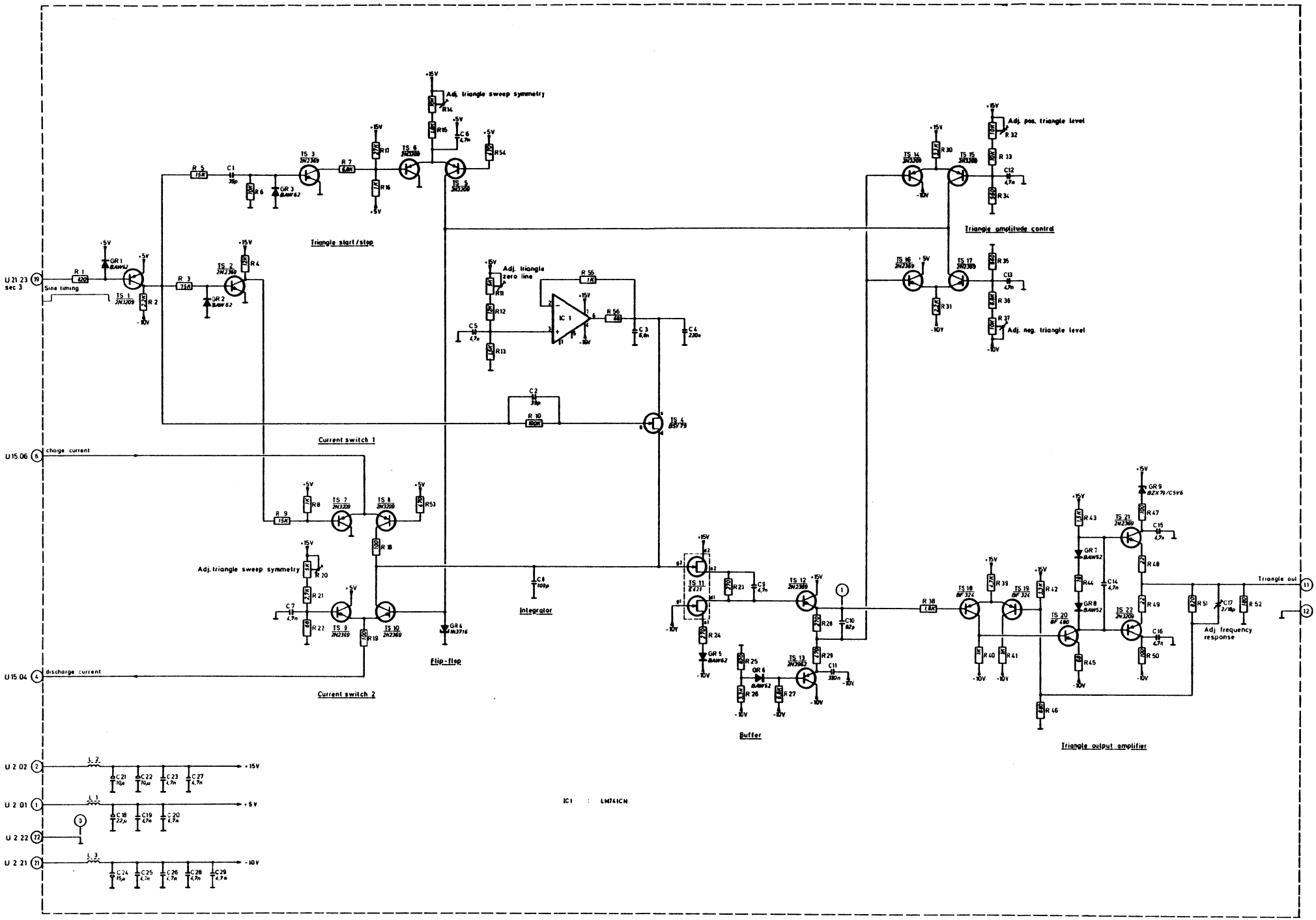

Fig. 21-3 Circuit diagram, triangle gen. + stop, unit 14

22. Unit 15 Frequency control

The frequency of the triangle generator, unit 14, is controlled by this unit, which contains the "Oscillator control current" stage as well as three mode circuits: The Fixed frequency control", the "Multiburst frequency control", and the "Sweep control".

Circuit description

In principle, the "Oscillator control current" stage is divided into two parts: An upper part, which consists of IC5, TS18, IC4, TS16, TS17, supplies the charge current to the integrator on unit 14, and a lower part, IC6, TS19, TS20, which is capable of sinking two times the current supplied to the triangle generator, unit 14. The charge current (terminal 6) and the discharge current (terminal 4) are both controlled by the dc voltage across the resistor R43. A less negative dc level means a high charge current at terminal 6, and a heavy current sink at terminal 4. Due to the high current, the integrator C8 on unit 14 will be charged and discharged fast and the resulting triangle frequency is high. A more negative dc level across R43 means a lower current, which results in a lower frequency.
The dc level across R43 is derived from a current flow generated with one out of the following three control circuits, depending of the mode chosen:

The "Fixed frequency control", which is connected to +15V by SK52 and a resistor network, consists of TS1, IC2, TS12, TS13. When this circuit is enabled by a fixed frequency timing pulse at terminal 13, TS12 is OFF, and a current flows through the fixed frequency resistor (SK52), TS1 and the resistor R43.
The resulting dc level across R43, which determines the triangle generator frequency, is now controlled by the setting of SK52 "SINE WAVE FIXED" at the front panel.

The "Multiburst frequency control" consists of six current generators, TS2 to TS7, and a multiburst address circuit IC1, which is a dual shift register.
When the "SINE WAVE MULTIBURST" mode is chosen, the reset of the multiburst address is cancelled and the multiburst clock at terminal 20 steps the shift register forwards. The first clock pulse, after the reset state is cancelled, activates the current generator TS2, and this current through R43 build up the dc level required to get the first multiburst frequency out of the oscillator, unit 14.
The next clock pulses activate the current generators, one by one, and all generators remain activated until the multiburst address is reset by the multiburst reset timing at terminal 19.
When activated each current generator contributes with a current flow through R43, and the resulting dc levels across this resistor determine the various multiburst frequencies.

The "Sweep control" consists of two current generators TS10, IC3 and TS11 controlled by the reset circuit TS14 and TS15.
In the "SINE WAVE SWEEP" mode a sweep timing command at terminal 18 sets TS14 and TS15 in the position OFF, and C12 will then be charged via TS11 and R32. The dc charging level is detected by IC3 and TS10, with converts the voltage slope of C12 to a variable current through R29, R30, TS10 and R43. Consequently the variable current through R43 makes the oscillator frequency (unit 14) sweep from 100kHz to more than 10 MHz.

Checking and adjusting

See chapter 31. Common adjustments

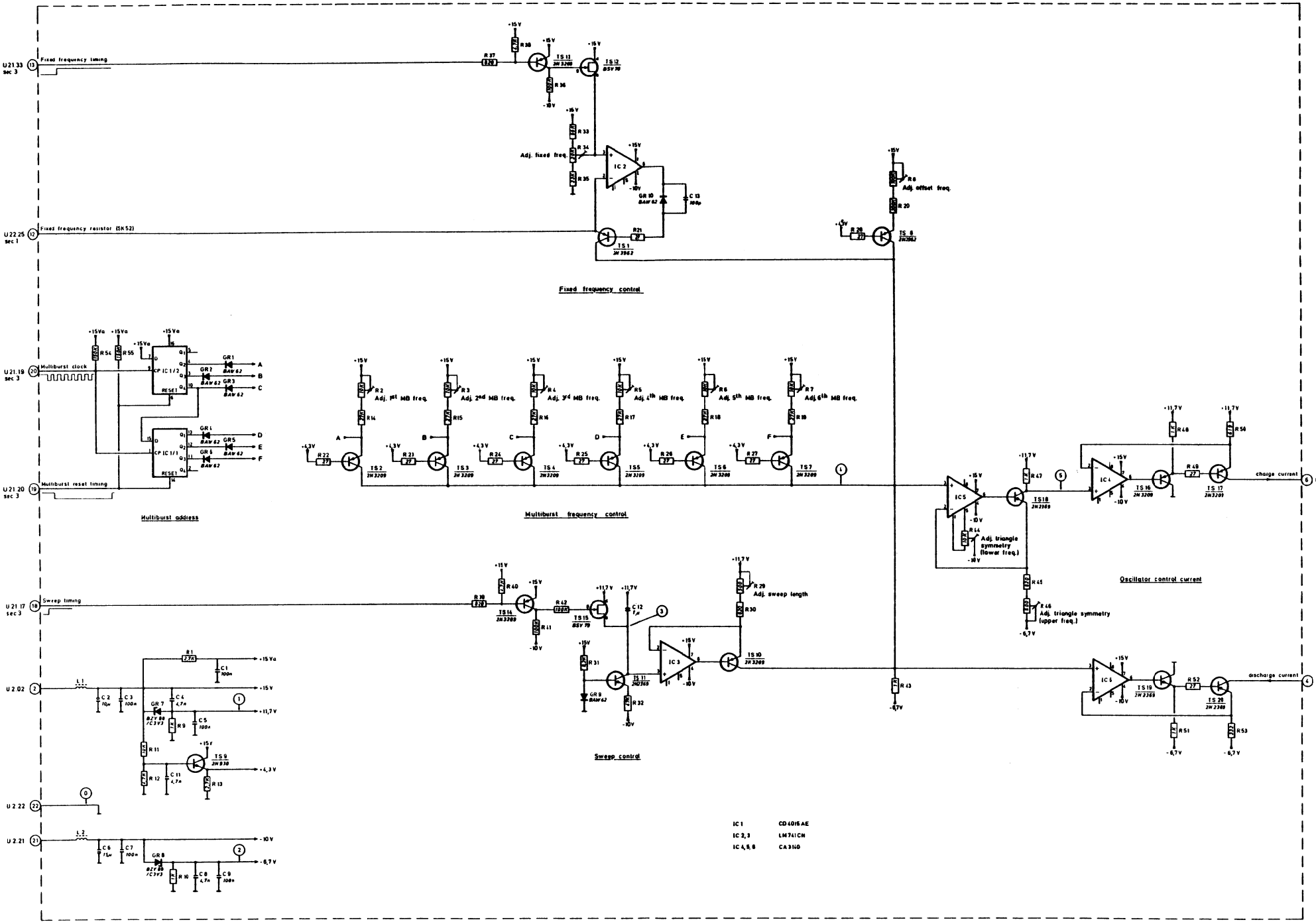

Fig. 22-2 Circuit diagram, frequency control, unit 15

23. Unit 16 Burst generator

This unit produces the burst signal, which is part of the complete TV-signal. Essentially, the circuit consists of a modulator, two phase shift circuits, and some control circuits.

Circuit description

The subcarrier signal from unit 20 is, via terminal 18, applied to the two 45^{o} phase shift circuits.
The -45^{o} phase shift is obtained by R13 and C4, which are located between the two buffer transistors TS2 and TS3.
The $+45^{o}$ phase shift is made with C6 and R19 + R20. These components are placed between TS4 and TS5.
The two phase shift outputs are then applied to the switch TS6, IC2, which allows passage of one signal at the time depending of the PAL identification pulse at terminal 13, provided,however, that the level at terminal 15 is "low".
The phase shift signal out of TS6 is then led to the "Y+" input of the modulator IC3, which is a double balanced modulator. Another signal is applied to the "X+" input, and this signal, which is derived from the burst key pulse (via terminal 4) and shaped to a burst envelope by the "Burst key shaper", controls the appearance as well as the amplitude of the modulator output.
Via the transformer TR1, the filter C9, L2//C10, C11, and the output stage TS7 the burst signal is passed along to the processing unit to be combined with the various signal elements.

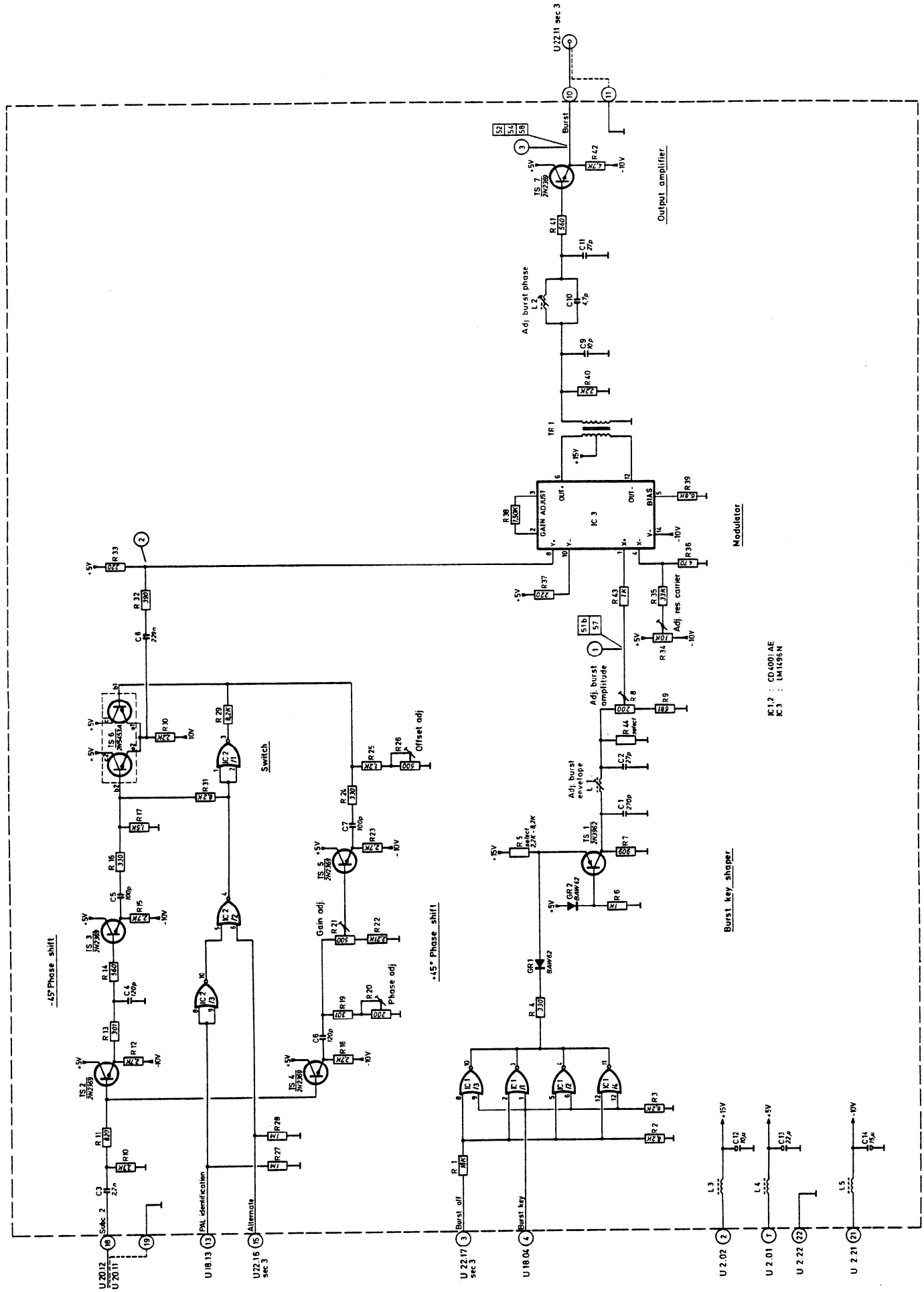

Fig. 23-10 Circuit diagram, burst generator, unit 16

24. Unit 17 Superimposition

The purpose of this unit is to allow either the subcarrier or the sine wave signal to superimpose the test signal in progress.
Generally, the unit consists of two signal inputs, two signal switches, a matrix, and an output stage.

Circuit description

The superimposition subcarrier part consists mainly of the double balanced "Modulator" IC1, which has a subcarrier signal applied to its "Y+" input, via terminal 7 and the "Buffer" TS3. When a superimposed subcarrier timing pulse is present at terminal 5, "Switch" TS1 enables the "Envelope generator" TS2, and the resulting pulse at the "X+" input controls the appearance and the amplitude of the modulator output signal.
Via the transformer TR1, the "Filter" C7, L2//C8, C9, and transistor TS4, the signal is applied to the "Matrix" R22, R23.

The superimposition sine wave part comprises an "Input amplifier" TS5, TS6, a "Sine switch" TS7 to TS11, IC2, and a buffer stage TS12. The superimposition sine wave signal from unit 13 is, via terminal 17 and the "Input amplifier" TS5, TS6, applied to the transistor TS8, which acts as the main gate of the "Sine switch". The two delay circuits, TS9 and TS10, are incorporated to compensate for transition time differences in the "Sine switch" components.
When a superimposed sine timing pulse at terminal 19 initiates the "Sine switch", TS8 is ON while TS7 and TS11 are OFF, and the superimposition sine wave signal has now access to the "Matrix" R22, R23, via TS12.

The "Matrix" output signal is then amplified in the "Output amplifier" TS13 to TS16 and passed over to the processing unit for further processing.

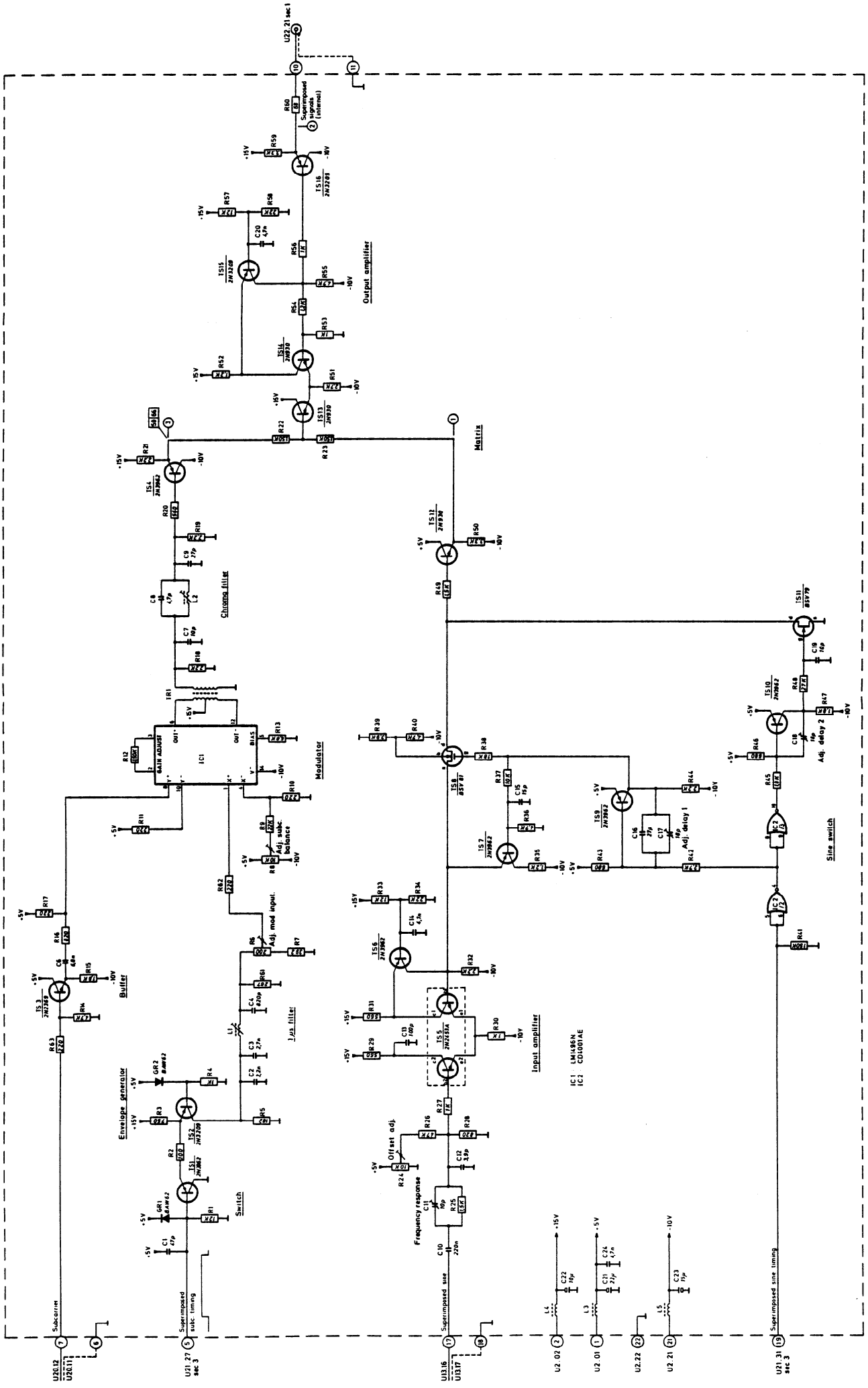

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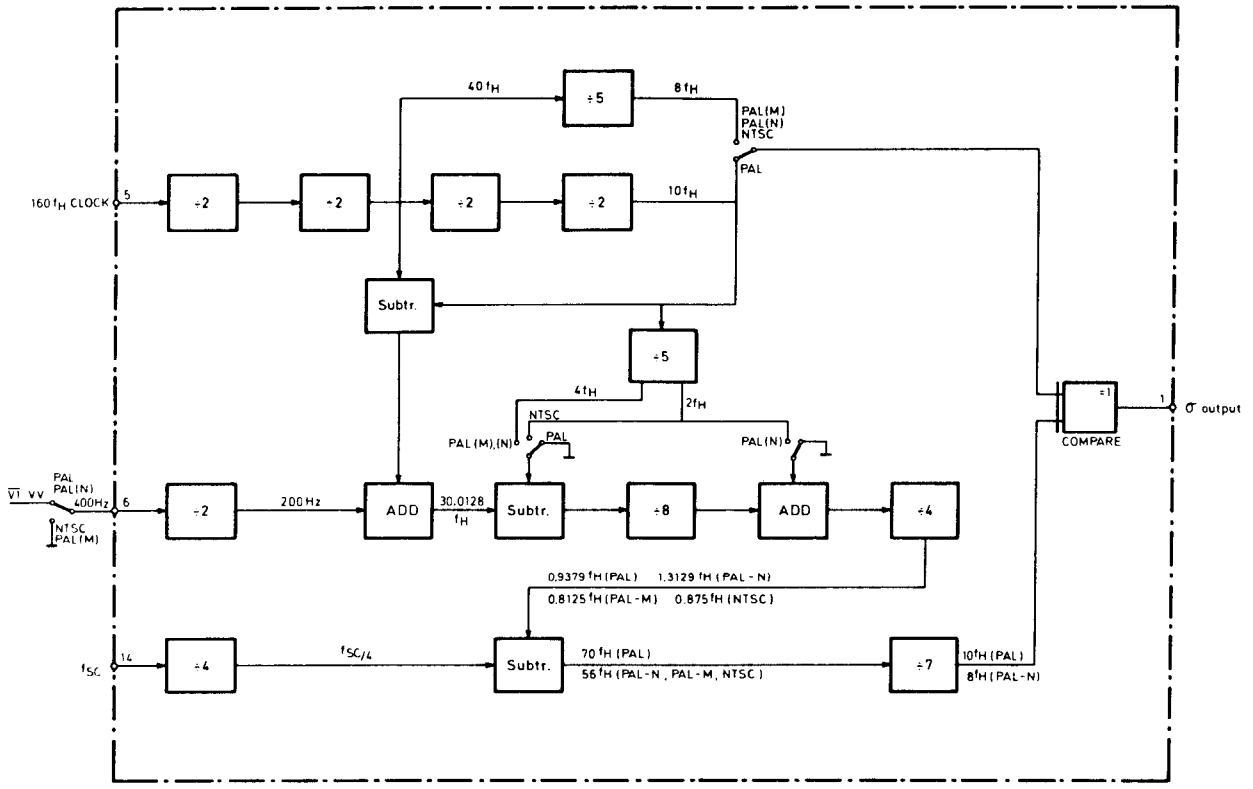
Fig. 24-11 Circuit diagram, superimposition, unit 17

Subcarrier/Line Frequency Relationship

A block diagram showing the method of establishing this relationship is given in Figure 26-4.



f_{SC}CCIR/PAL	:	4433618,75 Hz	f_HCCIR/PAL	:	15625 Hz
f_{SC}PAL (M)	:	3575611,49 Hz	f_HPAL (M)	:	15734,265 Hz
f_{SC}EIA/NTSC	:	3579545,0 Hz	f_HEIA/NTSC	:	15734,265 Hz
f_{SC}PAL (N)	:	3582056,25 Hz	f_HPAL (N)	:	15625 Hz

Fig. 26-4 Subcarrier/Line frequency relationship.

Basically the circuit is input with subcarrier frequency from the subcarrier oscillator and 160 f_H from the clocking oscillator. These two outputs are offered to an Exclusive-OR gate which acts as a comparator so that, if the two outputs are in phase, the output level of the signal will be logical zero. The Phase Lock Loop principle is illustrated in figure 26-5.

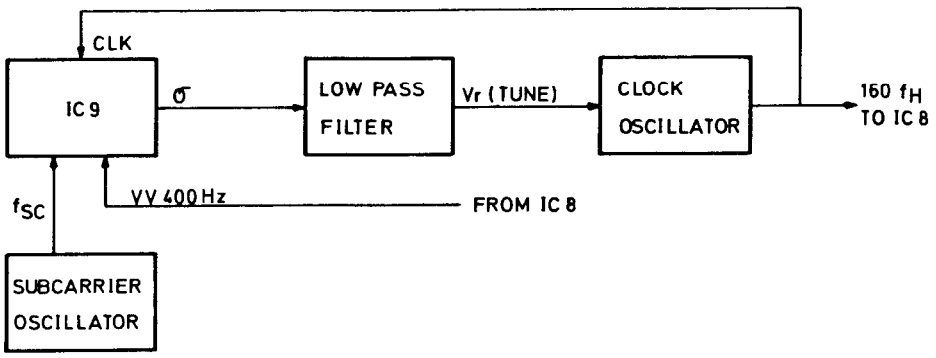


Fig. 26-5 Phase lock loop principle.

ECS Processing and Line Phase Comparison

The 160 f_H input to IC9 is first divided by eight, to provide a 20 f_H clock signal for the line counter. This counter divides by 20 and is reset by the leading edge of the External Composite Sync signal. The pulse period of the clock is 3.2 μs so that the counter period is 64 μs between ECS resets. Thus, provided the systems are locked, phase equality of the ECS signal and the line counter output will always be within 3.2 μs.

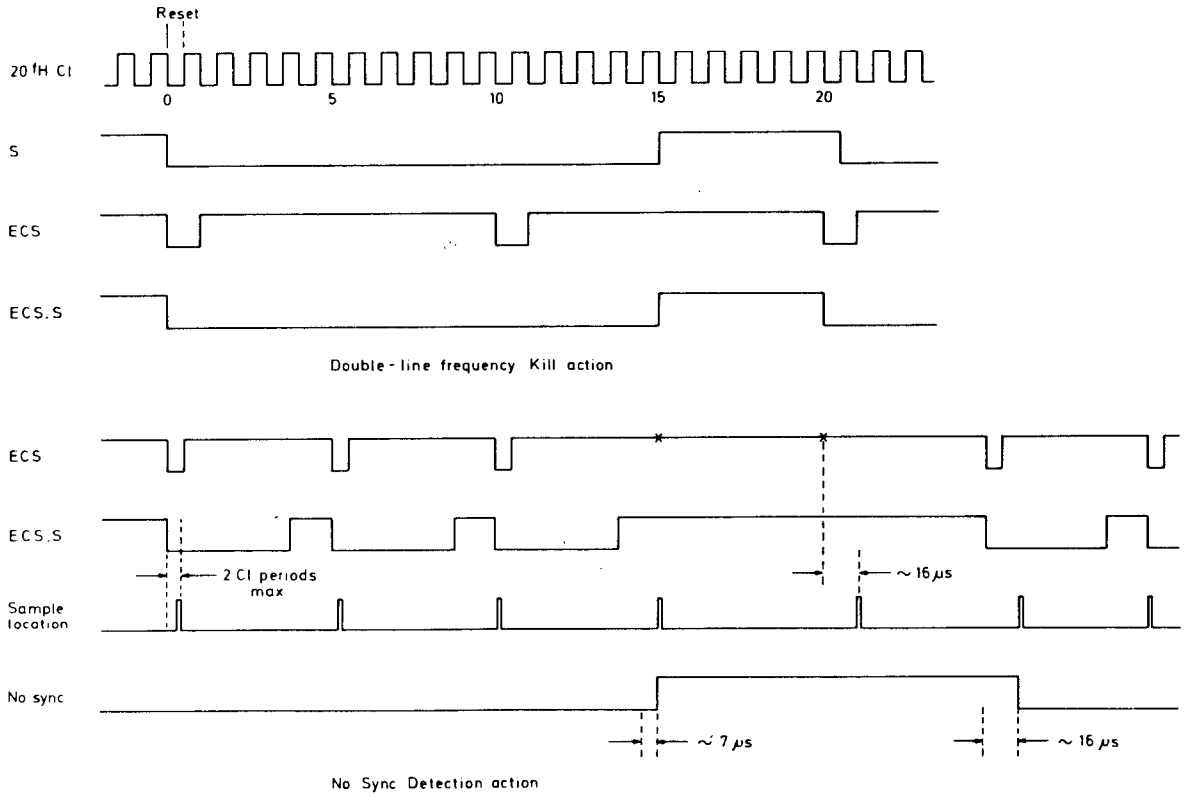


Fig. 26-6 Sync pulse processing in IC9.

After 15 clock pulse periods, the line counter outputs a signal to set a "dead-end" flip-flop output to logical one. This flip-flop 'S' will return to output a logical zero only if a reset occurs due to an ECS signal (i.e. it will remain high during ECS drop-out periods). The signal from the flip-flop is offered to the line phase comparator (the product eliminates the delay introduced by the flip-flop switching back to logical zero).

The NO SYNC detector in IC9 detects the absence of an ECS line pulse after a maximum of two clock pulse periods (i.e. approximately 7 μs) . By sampling the two-clock pulse periods in the ECS.S signal following every start of the line counter (i.e. not following a reset from the ECS signal), drop-outs can be detected quickly. When the NO SYNC (NS) signal becomes logical one, sampling of the 'S' information takes place 16 μs after the start of the line counter. This delay is necessary as the phase comparator in C9 must deliver the correct phasing information following possible drift of the oscillator during drop-out periods. Idealised waveforms showing the switching of the ECS Processing are given in figure 26-6.

Line Phase Comparison is achieved by an Early-Late detector. The product signal ECS.S is input to the comparator and forms the reference information to which the local signal H-Drive 1 from pulse generator IC8 is locked.

The principle of the Early-Late Detector is illustrated by the first waveform diagram of Fig. 26-7. The leading edge of the ECS.S. (reference) waveform drives the Y1 output and the leading edge of the local H1 signal drives the Y2 output
When both Y1 and Y2 signals are at logical zero, both lines are switched back to logical one. Thus the trailing edges of the Y1 and Y2 pulses are always coincident and the difference in pulse widths (duty cycles) provides a measure of the phase error between the reference and the local signals.

The outputs of the Y1 and Y2 channels are fed to lowpass filters R70/C28 and R69/R74/C27 where they are integrated to provide d.c. levels at the inputs of op. amplifier IC10. With a phase error present, as shown in the diagram, the op. amplifier inputs will be unbalanced so that this will produce a control output voltage to tune the 160 f_H oscillator until the error is cancelled and equilibrium is established at the inputs. Thus Y1 and Y2 pulses will have the same duty cycle and the leading edge of the H1 signal will coincide precisely with that of the ECS.S. reference signal. Due to the high open-loop gain of op. amplifier IC10, very small phase differences will produce the full control voltage range, thus ensuring very fast response with an accuracy of ±100 nanoseconds.

When drop-outs occur in the ECS.S. reference signal this is detected so that the NO SYNC detector produces an output to the switches TS11, TS12. Thus, during these periods, the control voltage for the 160 f_H oscillator is derived from the Sub-carrier/Line Frequency Relationship from pin 1.

The second waveform diagram of Fig. 26-7 demonstrates the method of detecting the External Vertical Sync Pulse for use in IC8. The level of the ECS signal is detected twice per half-line. The first detection occurs 6,5 µs after the start of the line counter and the second a further 6,5 µs later. From detectors 1 and 2 pulses the signal EV1 and EV2 are derived and, thence, the product signal $\overline{EV1}$. $\overline{EV2}$ provides a suitable EV output to IC8. Double detection of the ECS signal is required for applications involving VCR-locking.

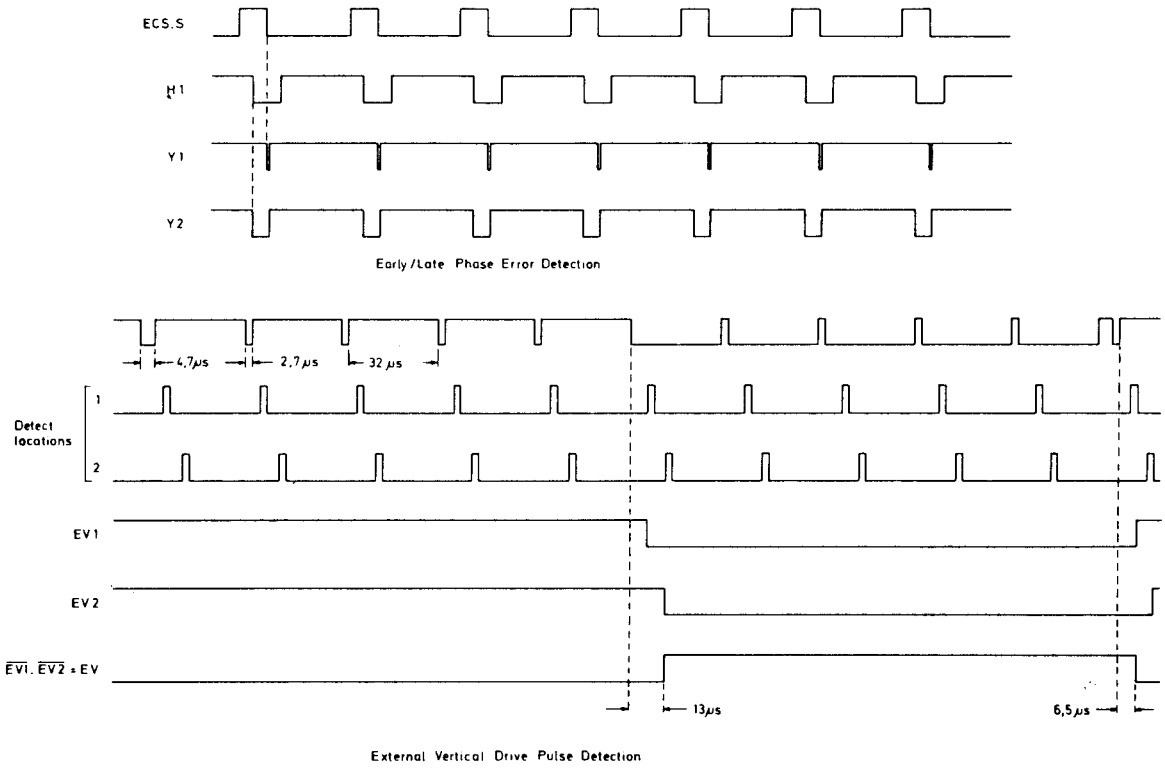


Fig. 26-7 External vertical drive pulse detection.

Circuit description

As mentioned in the functional description of OQ5501 and OQ5502, the entire sync and phase-locking are carried out by these IC's, which have two basic requirements: A clock oscillator and a colour subcarrier.

The "10MHz oscillator" on this unit is an X-tal oscillator, which is controlled by the dc output level of IC10.
The 10MHz signal is then divided by two in IC7/2, and the so derived 5MHz signal is passed on to unit 18, via terminal 10, as well as to another divide by two system IC7/1. The resulting 2.5MHz - equal to $160f_H$ - is applied to IC8 and IC9 to drive the entire sync generator.

The colour subcarrier, derived from unit 20, is via terminal 12 passed on to the "Genlock" circuit IC9, pin 14, in which it is used to established the relationship between subcarrier and line frequencies.

When a composite sync signal or a black burst signal is applied to the looped-through "SYNCHR IN" input, this signal has access to the "Buffer" stage TS1 via terminal 3.
The output from TS1 is now processed by four circuits. First the chroma contents of the signal is removed by the "Chroma take-out" circuit L3, C9 and is passed along to the "Subcarrier generator" unit 20. Then the TS1 output is also used to initiate the "Clamp pulse generator" IC3, IC2/1, IC4/2, provided that no field sync information is present. The clamp pulse is positioned at the back porch on each line outside the field sync period.
The TS1 output is via TS4 applied to IC5, where the black level of the signal is clamped to zero by the clamp pulse (via TS5). The signal is then amplified by IC5 and passed on to IC6 as well as to TS6, TS7, which is a negative sync peak detector.
The "Sync level detector" output is, reduced to 50% by R29, R30, fed to IC6.
The resulting output of IC6 is a sync signal sliced at 50% of the sync peak level and this signal is led to the "Genlock" circuit IC9.

In order to remove hum from the incoming sync signal (via TS1), the dc level of C10 is compared to zero by IC1 in the "Hum remover". The output of IC1 is followed by a one-shot generator IC2/2 where, depending on the hum polarity, C10 + R10 is connected either to +5V (through TS2) or to - 10V via R11, thus compensating the hum.

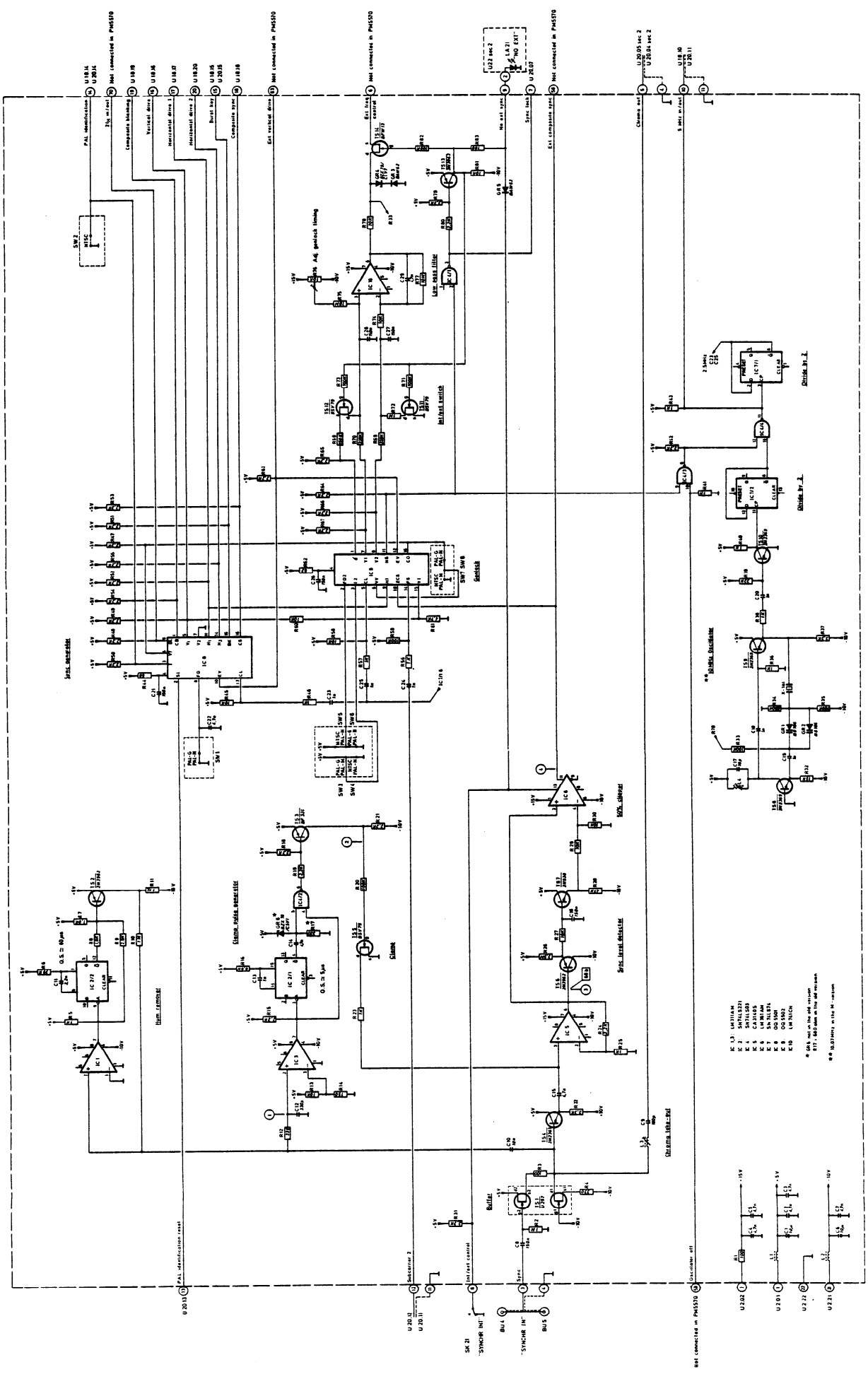


Fig. 26-12 Circuit diagram, sync generator, unit 19/01/02

27. Unit 20 Subcarrier generator

This unit produces the colour subcarrier by means of a Temperature Compensated X-tal Oscillator, which is corrected by some control circuits.

Circuit description

The "Oscillator" consists of an 8,86 MHz TCXO, the output of which is buffered by TS13 and is shaped by TS14. Then the 8.86 MHz signal is divided by two in IC6/2 and is passed over to the "Limiter" stage TS15 to TS17, where the sinusoidal shaping of the signal is carried out.
The "Limiter" stage is followed by two amplifiers, "Output amplifier 1" and "Output amplifier 2", where "Output amplifier 1" provides the 4.43 MHz subcarrier signal to the "SUBC OUT" connector BU7 at the rear, while "Output amplifier 2" provides the 4.43 MHz subcarrier to be used inside the PM 5570.

In order to lock the "Oscillator" to an external chroma signal a "Demodulator" and some burst control circuits are present.
In the case when a composite sync signal is connected to PM 5570 and the sync mode selector SK22 is pressed, a "high" level at terminal 7, Sync lock, indicates the presence of the sync, while the chorma signal at terminal 5 is taken out from the applied sync signal.
In the burst key periods, this chroma signal has access to the "Limiter" and the "Burst detector" via the "Input amplifier" and the "Burst gate".
The "Limiter" output is then applied to the "X+" input at the "Demodulator" IC2, which continuously has part of the subcarrier signal connected to its "Y+" input. These two signals are now compared by means of IC2, and the phase difference is amplified by IC3, the output of which , via TS8, has access to the hold capacitor C15 every second line. TS8 performs the gate part of the "Sample and hold" circuit TS7, TS8, C15, in which the sampling intervals are controlled by the PAL identification pulses at terminal 14. The voltage of C15 is, via the "Low-pass and amplifier" IC4 and the switch TS12, passed over to the "TCXO" to correct the subcarrier frequency.
The switch TS12 is "ON", only when a chroma signal is detected by the "Burst detector" and at the same time the sync lock level at terminal 7 is "high".
The PAL identification phase of the chroma signal is sensed at the "Demodulator", pin 6, and this phase information is via IC7 applied to the "PAL identification phase detector", where it is compared to the vertical drive pulse coming from the sync generator unit. In case of improper phasing a positive PAL identification reset pulse is applied to the sync generator unit, via terminal 13, and this pulse causes the PAL identification pulse to be "high" as long as the PAL identification reset pulse remains "high".

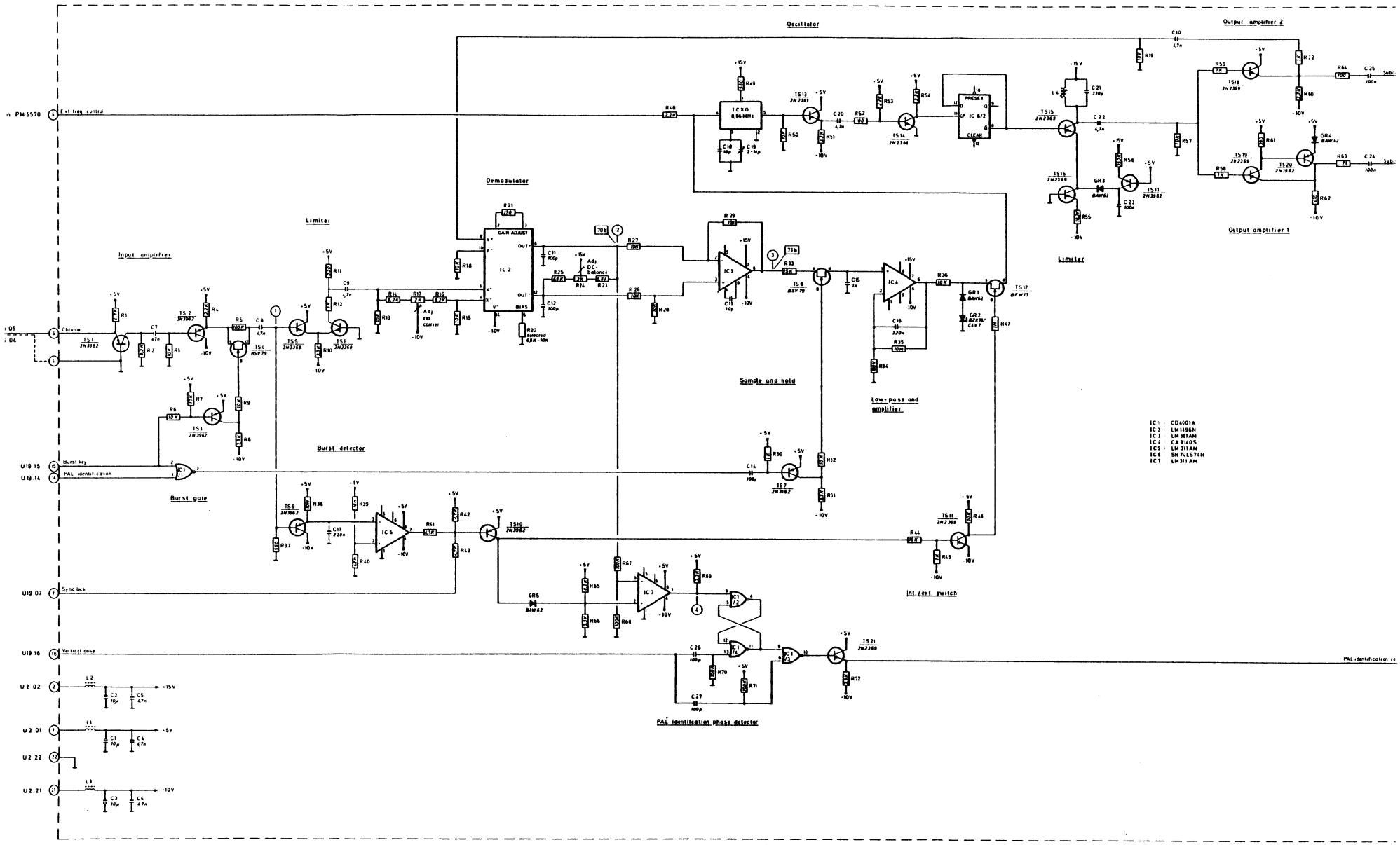


Fig. 27-5 Circuit diagram, subcarrier gene

Section 4. Video signal out

In this section the composite video signal is formed by the various signal elements. The composite video signal in progress is then combined with the ITS information. Finally the entire video signal is superimposed with some well specified signals.

Circuit description

The various signal elements are via the terminals 40, 37, 44 respectively combined in the "Matrix" which is followed by the "Buffer" stage TS401, TS402. The buffered composite video signal is then applied to an attenuator P6/SK48 "COMP VIDEO", where SK48 has five positions: A nominal level "NOM", a preset level "PRE", and a continuously variable position "VAR" in which the level is determined by the potentiometer P6. A fixed +3dB position as well as a fixed -3dB position are also provided. The attenuator output signal is amplified by means of the "Composite video amplifier" TS403 to TS407 and clamped to a proper dc level by TS408, which is controlled by the "Clamp generator" in unit 18.
The clamped composite video signal is now amplified in one more amplifier TS409, TS419, TS410 and passed over to the "Video switch" TS411, which is controlled by a command pulse from unit 21 via terminal 18.
When the "Video switch" is ON ("high" level at terminal 18) the composite video signal is passed on to the "Matrix" R440, R441 via the "Buffer" TS412.

In the "Matrix" the entire composite video signal including the ITS information can now be superimposed with hum, noise, subcarrier/sine wave information, or with a signal from an external source.

The "Matrix" output is then filtered and led to the "Video output amplifier" TS414 to TS418, which after a final processing provides the video output signal to the three output connectors BU12, BU13, and BU3.

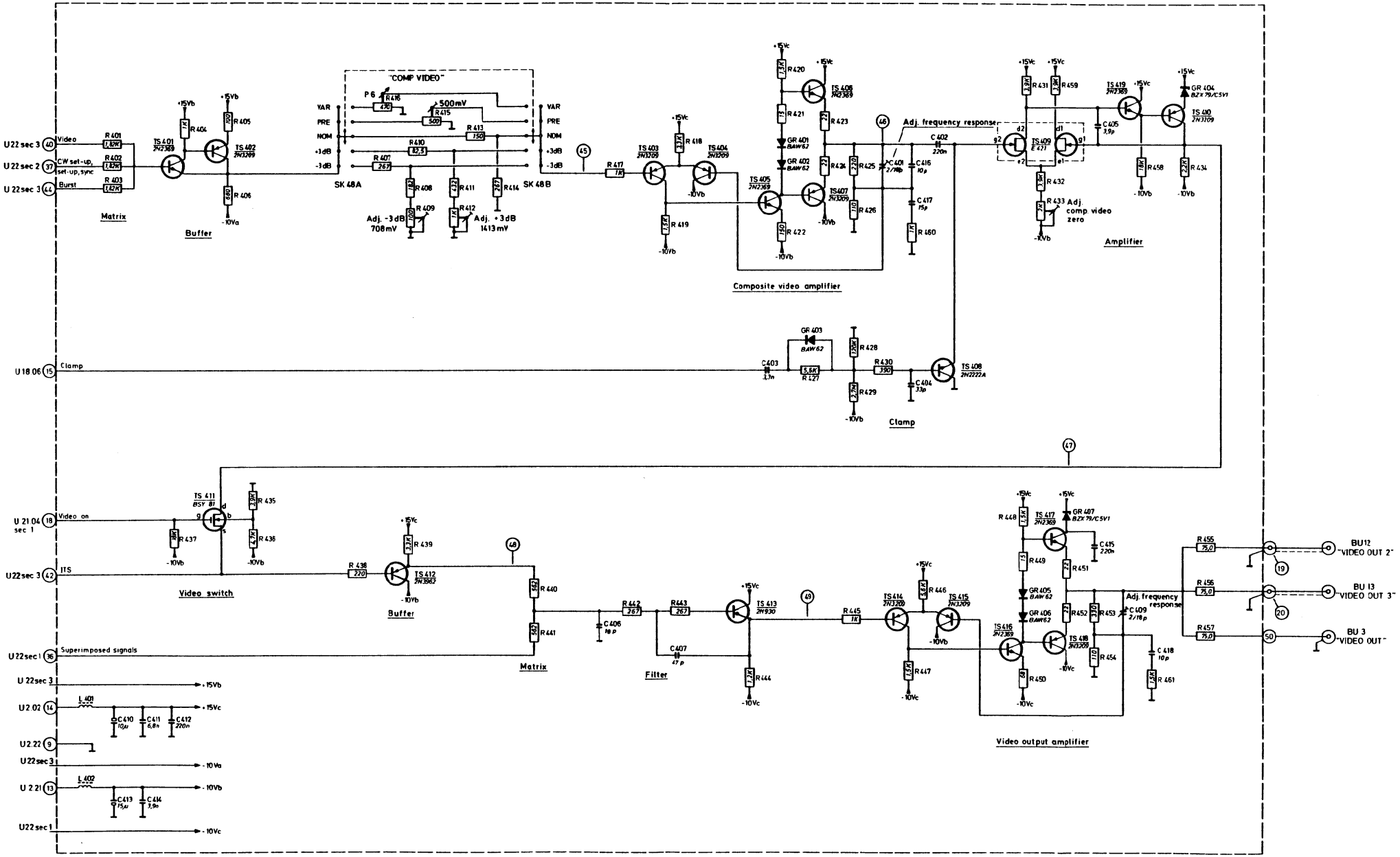


Fig. 29-10 Circuit diagram, processing unit, unit 22 sec. 4

30. Unit 23 Noise generator

This unit produces a random white noise signal intended to be used as one of the superimposition signals.
The generator consists of a "Noise source" TS1 to TS4 and a "Noise amplifier" TS5 to TS8.

Circuit description

Basically, the noise signal is generated in the "Noise source" circuit TS1 to TS4 by the combination of R5//R6 and TS2 followed by the transistors TS3 and TS4.
The level of the noise signal out of TS4 is about 1mVpp, and this signal is via C5 passed on to the "Noise amplifier" TS5 to TS8 to be amplified to a noise output level at about 35mVpp.
The noise output signal is then applied to another noise amplifier on unit 22, section 1.

Note When the switch SK50 "NOISE" at the front is in position "OFF", the +11.3V supply is switched off.

Checking and adjusting

None.

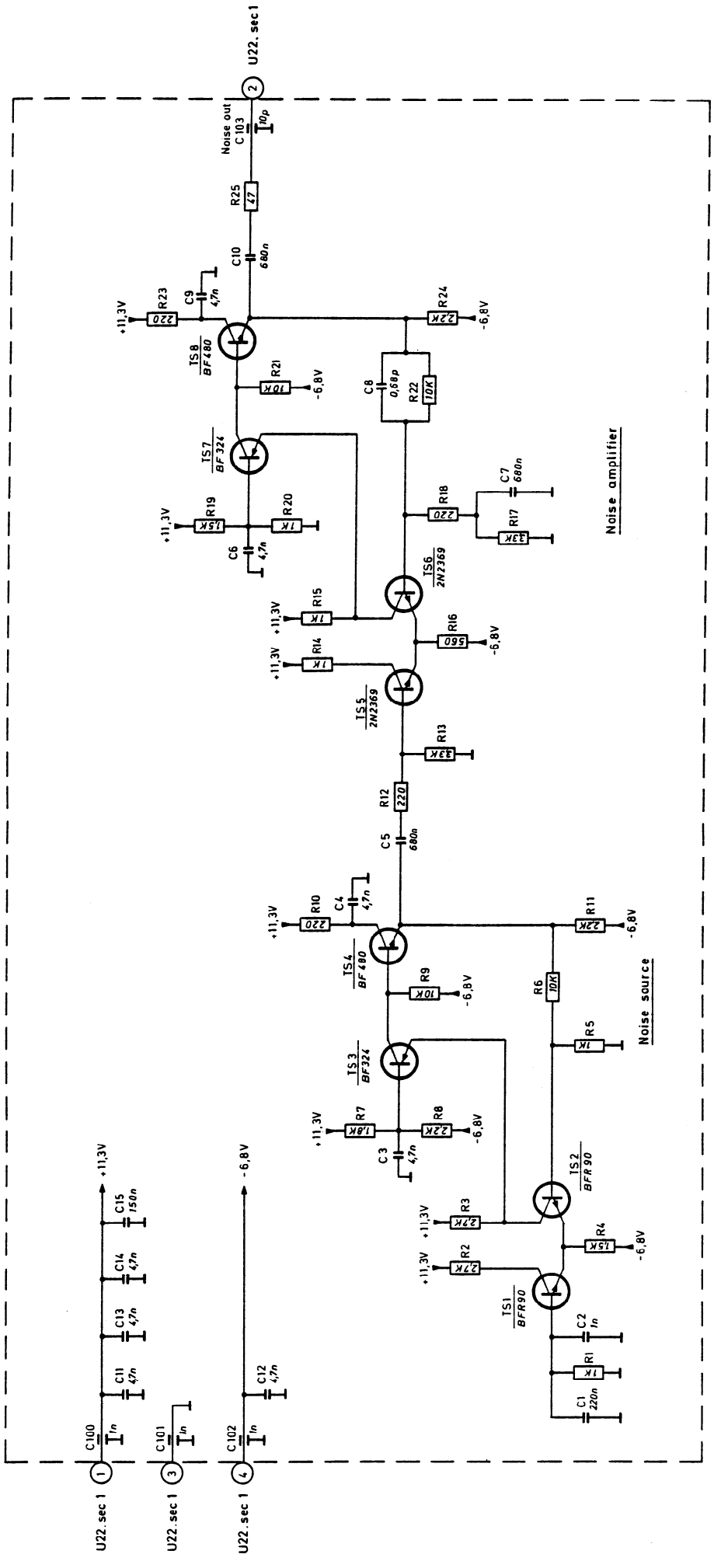


Fig. 30-2 Circuit diagram, noise generator, unit 23