XIV. Unit 2 Circle memory

This unit consists of the circle register with the 15 MHz clock oscillator, the memory, the address counter and the center line gate.

The circle register consists of two rows of binary counters IC2, IC4, IC6 and IC7 generate the left part, and IC10, IC11, IC12 and IC13 generate the right part of the circle.

The counters are set, respectively reset, by the bits 1 to 8 from the memory.

The 15 MHz clock oscillator TS1 and TS2 is an emitter coupled multivibrator, which is controlled by a start/stop circuit (IC1, IC2 and IC17) via TS3.
The start/stop circuit consists of two bistable multivibrators IC15/1, IC15/3 and IC1/3, IC1/4.

The functioning of the circle register is as follows: (see Fig. XIV-1).

1. At the time t_1 a $\overline{f_H}$ pulse, amplified by IC14, is applied to the register.
The pulse to the register for the left circle part is applied to the clear input and will set all outputs to "0".
The pulse to the register for the right circle part is applied to the pre-set input and will accordingly set all outputs to "1".

2. At the time t_2 the memory will be read-out and via the IC21 and IC22 the bits are applied to the pre-set inputs of one register, and to the clear inputs of the other register.
The gates IC3 and IC5 are incorporated in the upper counter row to disable unwanted triggering during the pre-setting period.
At the time t_2 a read-out pulse $\overline{H5\text{-}7}$ will disable any information from the circle register to flip-flop IC9. The same pulse, inverted in IC23/2, is used as an enable pulse for the gates IC21, IC22. The content of the memory for the time being will then be transferred and stored in the register until the counting down is started.
The selection of the different words is controlled by the address counter.

   The address counter consists of two up/down counters IC17, IC19 in cascade. The count-direction is determined by the "h" pulse (field control pulse) from unit 4.
The "h" pulse is "0" in the first field and "1" in the second field. It means that the address counter counts up in the 1st field and down in the 2nd field. The line pulses $\overline{f_H}$ are used as clock-pulses for the address counter, and the outputs are used to address the memory.
In order to obtain a fixed start position for the address counter, the V3-5 pulse generates a load pulse, which pre-sets the counter to a certain value according to the pre-set table (see Fig. XIV-1).

   The center line gate supplies a raster of horizontal white lines V_I which are placed between the raster V_L (unit 4).
The information for the gate is derived in such a way, that the field sequence of these lines is opposite to the one of the other white horizontal lines.
This is done in order to obtain the special interlacing center line V_I' (see unit 5).
These gates will only be open for the pulses, when the upper row of the register is in action.

3. At the time t_3 output 11 of flip-flop IC1 will shift to "1" by the "start 1" pulse (from unit 4), which will open the gates for the left circle register.
At the same moment output 12 of flip-flop IC15 will shift to "0", which starts the 15 MHz oscillator. The register will then start counting down to zero. When the register has reached the zero position, output 6 of IC7 supplies a pulse, which via IC8/2 and 8/1, shifts the flip-flop IC9. This shift determines the left side of the circle.
Output 3 of IC8/1 will also shift flip-flop IC15 and stops the 15 MHz oscillator.

4. At the time t_4 the same process will be repeated for the right side circle register. Then the register and the oscillator will be started by the "start II" pulse.
When the register has reached zero by counting down from the start position, flip-flop IC9 will be shifted back again and determine the right side of the circle.

The circle pulse "ϕ" passes through the gate IC15/2 to the video mixers (unit 11 and 13).
The "ϕ" pulse can only pass through the gate when switch SK2 ("GRID ONLY") is off and the enable pulse V4-28 is present.

The memory, which contains the circle information, is a 2048-bit Read-Only Memory organized as 256 words of eight bits each. 252 words are sufficient to describe the entire circle (204 words in M-version).

NB. For modifying this unit from G-version to M-version or vice versa one jumper has to be positioned in accordance with the diagram. The memory IC20 has to be replaced with a memory containing the relevant program.

Checking and adjusting

See unit 4.

PRE-SETTING OF THE ADDRESS COUNTER						
	COUNTER	MEMORY	G-VERSION		M-VERSION	
	OUTPUT	INPUT	FIELD I	FIELD II	FIELD I	FIELD II
IC 17	A	A1	1	0	1	0
	B	A2	1	0	0	1
	C	A3	1	0	0	1
	D	A4	0	1	0	1
IC 19	A	A5	1	0	1	0
	B	A6	1	0	0	1
	C	A7	1	0	0	1
	D	A8	1	0	0	1
VALUE			247	8	17	238

MA8574

Fig. XIV-1. Pre-setting of the address counter

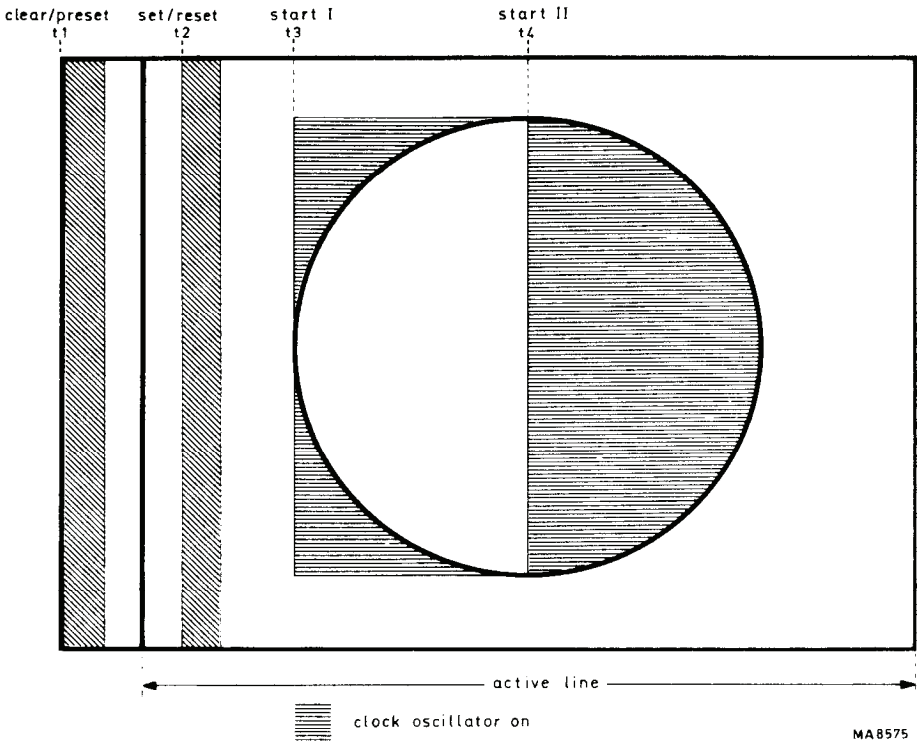
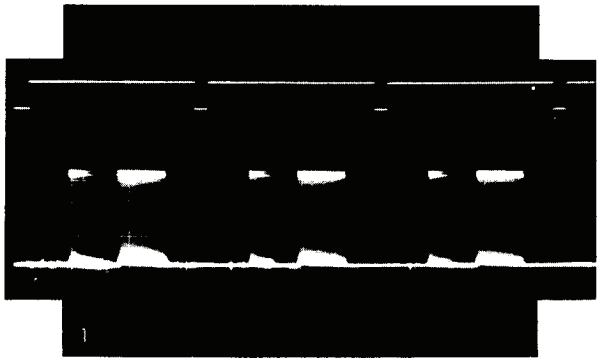


Fig. XIV-2. Circle memory



2 V/div. 20 µs/div.
Ref.: $\overline{f_H}$. pulse

Fig. XIV-3. Oscillogram, unit 2

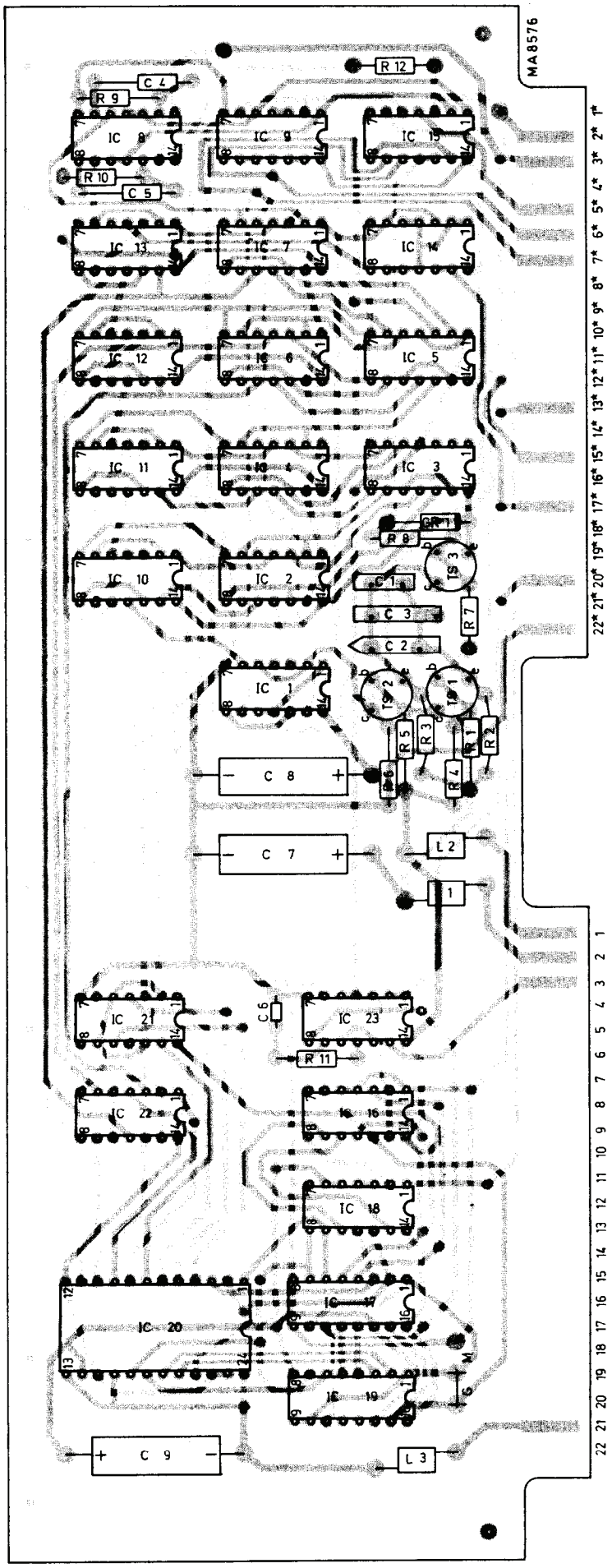
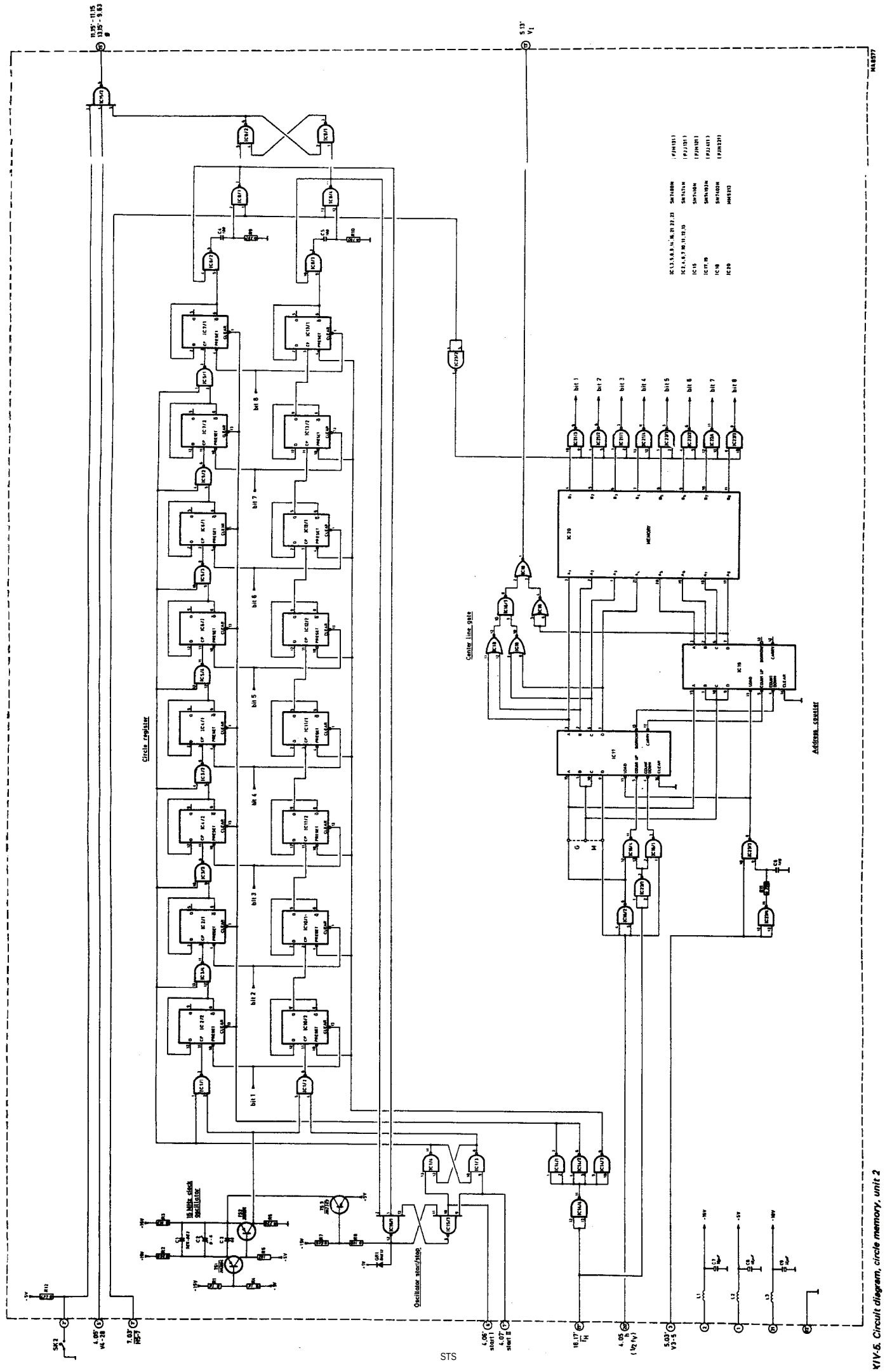


Fig. XIV-4. Printed wiring board, circle memory, unit 2



KIV-6. Circuit diagram, circle memory, unit 2