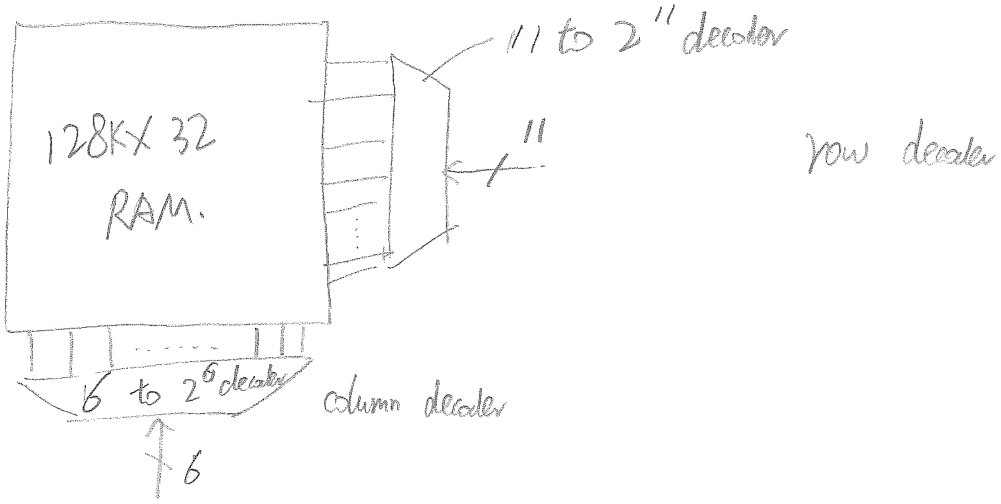
Homework 7 – Solution

1. [Memory]
   a) 8K X 32 = 2^{13}*32
      Address wires: 13
      Data wires: 32
      Bytes = 8K * (32/8) = 32K
   b) 256K X 64 = 2^{18}*64
      Address wires: 18
      Data wires: 64
      Bytes = 256K * (64/8) = 2M
   c) 32M X 32 = 2^{25}*32
      Address wires: 25
      Data wires: 32
      Bytes = 32M * (32/8) = 128M

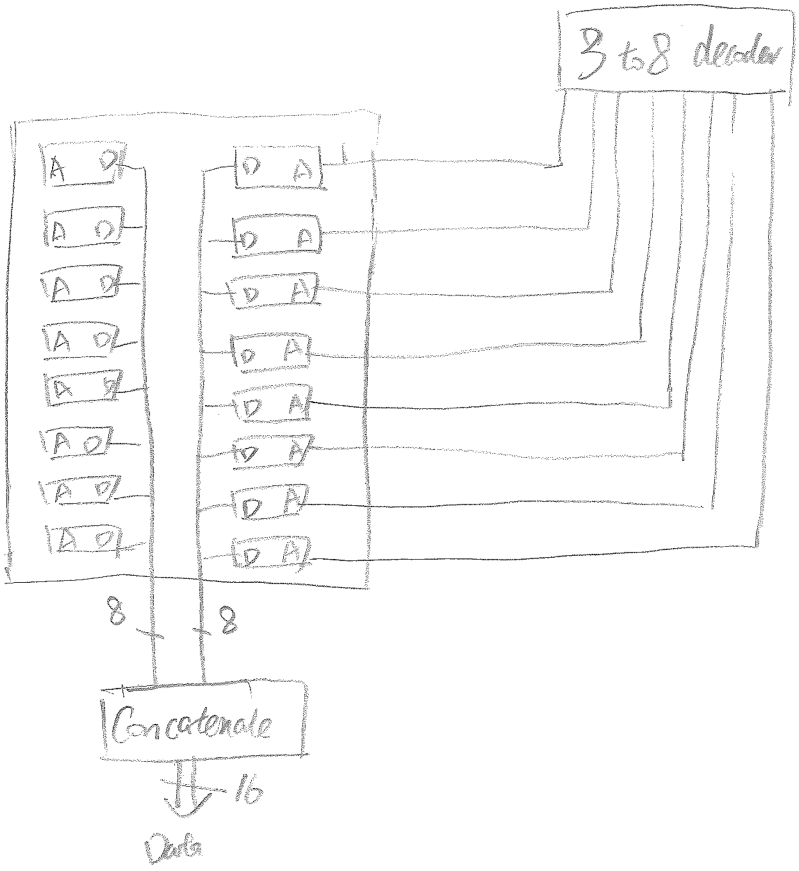
2. [Memory]
   a) 128K X 32 = 2^{17} * 2^5 = 2^{22} = 2^{11} * 2^{11}
      2^{11} columns (bits) = 2^6 32-bit words per row
      2^{11} rows



   b) 0x39ABCD = 11 1001 1010 1|011 110|0 1101
      -row address-- -col addr- -offset-

   c) Square structure means faster access time, since row and column widths are minimal.

3. [Memory]
   Two chips in the same row have the same address input:



4. [Cache]
   a) Major memory technologies: SRAM, DRAM, disk
   b) SRAM: fastest, larger area compared to DRAM
      DRAM: slower but smaller area compared to SRAM
      Disk: cheap, large capacity, slow
   c) There are multiple memory technologies since they meet different requirements on area, power and speed.

5. [Cache]
   a) DRAM chip: 60ns
   b) SRAM chip: 5-25ns
   c) FLASH chip: 75ns

6. [Cache]

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for (i=0; i<100; i++)
    for (j=0; j<=1000; j++)
            A[i,0] = A[i,j] + B[j,i]
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   a) A great deal of temporal locality of data: A[i,0] in above code
   b) A great deal of spatial locality of data: A[i,j] in above code
   c) A great deal of temporal locality of instructions: the inner for loop in above code

d) A great deal of spatial locality of instruction: a sequence of instructions without any branches or jumps.