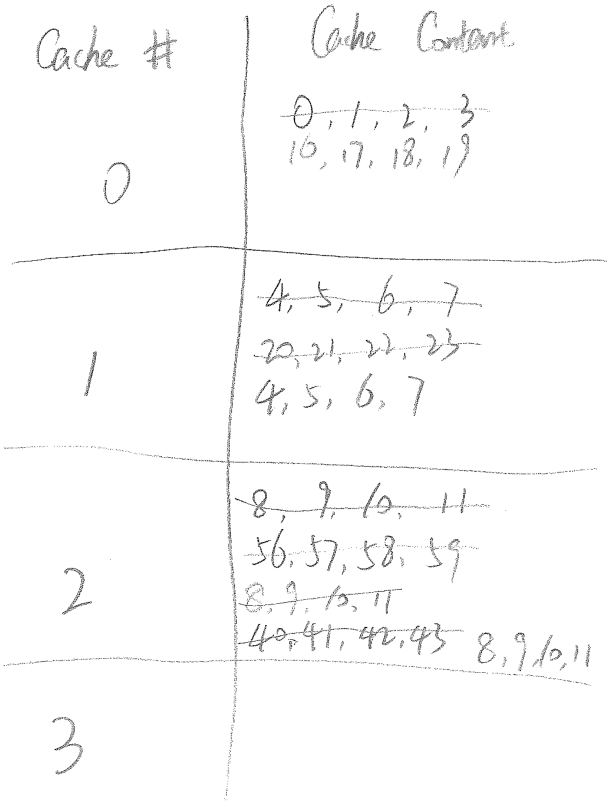
Homework 8 – Solution

1. [Cache]
   2.4GHz clock → 0.4ns clock cycle
   Miss time is 40 ns → 100 more cycles on a miss
   a) CPI = 0.7 + (30% x 5% x 100) + (2% x 100) = 4.2
   ---data miss----- --instr miss-
   instr/sec = 2.4G/6.2 = 387,096,774
   b) CPI=0.7
   instr/sec = 2.4G/0.7 = 3,428,571,429

2. [Cache]
   - Direct mapped with 16 1-word blocks

Cache #	Cache Content
0	
1	17
2	
3	19
4	4
5	5
6	6
7	
8	56
9	9
10	
11	43
12	
13	
14	
15	

- Direct mapped with 4 4-word blocks



3. [Cache]

5.1.1 4

5.1.2 I, J

5.1.3 A[I][J]

5.1.5 I, J

5.1.6 A(J, I)

4. [Cache]

5.2.1

Word Address	Binary Address	Tag	Index	Hit/Miss
3	0000 0011	0	3	M
180	1011 0100	11	4	M
43	0010 1011	2	11	M
2	0000 0010	0	2	M
191	1011 1111	11	15	M
88	0101 1000	5	8	M
190	1011 1110	11	14	M
14	0000 1110	0	14	M
181	1011 0101	11	5	M
44	0010 1100	2	12	M
186	1011 1010	11	10	M
253	1111 1101	15	13	M

5.2.2

Word Address	Binary Address	Tag	Index	Hit/Miss
3	0000 0011	0	1	M
180	1011 0100	11	2	M
43	0010 1011	2	5	M
2	0000 0010	0	1	H
191	1011 1111	11	7	M
88	0101 1000	5	4	M
190	1011 1110	11	7	H
14	0000 1110	0	7	M
181	1011 0101	11	2	H
44	0010 1100	2	6	M
186	1011 1010	11	5	M
253	1111 1101	15	6	M

5.2.3

Word Address	Binary Address	Tag	Cache 1		Cache 2		Cache 3	
			index	hit/miss	index	hit/miss	index	hit/miss
3	0000 0011	0	3	M	1	M	0	M
180	1011 0100	22	4	M	2	M	1	M
43	0010 1011	5	3	M	1	M	0	M
2	0000 0010	0	2	M	1	M	0	M
191	1011 1111	23	7	M	3	M	1	M
88	0101 1000	11	0	M	0	M	0	M
190	1011 1110	23	6	M	3	H	1	H
14	0000 1110	1	6	M	3	M	1	M
181	1011 0101	22	5	M	2	H	1	M
44	0010 1100	5	4	M	2	M	1	M
186	1011 1010	23	2	M	1	M	0	M
253	1111 1101	31	5	M	2	M	1	M

Cache 1 miss rate = 100%

Cache 1 total cycles = $12 \times 25 + 12 \times 2 = 324$

Cache 2 miss rate = 10/12 = 83%

Cache 2 total cycles = $10 \times 25 + 12 \times 3 = 286$

Cache 3 miss rate = 11/12 = 92%

Cache 3 total cycles = $11 \times 25 + 12 \times 5 = 335$

Cache 2 provides the best performance.

5. [Cache – associativity]
   The cache has 24/3/2= 4 blocks per way, and thus an index field of 2 bits.
   These are word addresses, so there is a one-bit block offset.

Word Address	Binary Address	Tag	Index	Hit/Miss	Way 0	Way 1	Way 2
3	0000 0011	0	1	M	T(1)=0		
180	1011 0100	22	2	M	T(1)=0 T(2)=22		
43	0010 1011	5	1	M	T(1)=0 T(2)=22	T(1)=5	
2	0000 0010	0	1	H	T(1)=0 T(2)=22	T(1)=5	
191	1011 1111	23	3	M	T(1)=0 T(2)=22 T(3)=23	T(1)=5	
88	0101 1000	11	0	M	T(0)=11 T(1)=0 T(2)=22 T(3)=23	T(1)=5	
190	1011 1110	23	3	H	T(0)=11 T(1)=0 T(2)=22 T(3)=23	T(1)=5	
14	0000 1110	1	3	M	T(0)=11 T(1)=0 T(2)=22 T(3)=23	T(1)=5 T(3)=1	
181	1011 0101	22	2	H	T(0)=11 T(1)=0 T(2)=22 T(3)=23	T(1)=5 T(3)=1	
44	0010 1100	5	2	M	T(0)=11 T(1)=0 T(2)=22 T(3)=23	T(1)=5 T(2)=5 T(3)=1	
186	1011 1010	23	1	M	T(0)=11 T(1)=0 T(2)=22 T(3)=23	T(1)=5 T(2)=5 T(3)=1	T(1)=23
253	1111 1101	31	2	M	T(0)=11 T(1)=0 T(2)=22 T(3)=23	T(1)=5 T(2)=5 T(3)=1	T(1)=23 T(2)=31

5.7.2 Since this cache is fully associative and has one-word blocks, the word address is equivalent to the tag. The only possible way for there to be a hit is a repeated reference to the same word, which doesn't occur for this sequence.

Tag	Hit/Miss	Contents
3	M	3
180	M	3, 180
43	M	3, 180, 43
2	M	3, 180, 43, 2
191	M	3, 180, 43, 2, 191
88	M	3, 180, 43, 2, 191, 88
190	M	3, 180, 43, 2, 191, 88, 190
14	M	3, 180, 43, 2, 191, 88, 190, 14
181	M	181, 180, 43, 2, 191, 88, 190, 14
44	M	181, 44, 43, 2, 191, 88, 190, 14
186	M	181, 44, 186, 2, 191, 88, 190, 14
253	M	181, 44, 186, 253, 191, 88, 190, 14

6. [Virtual Memory]
   Page size = 64KB = 2^{16} → 16 LSBs for page offset
   Address space = 28 bits → number of bits for page selection = 28 – 16 = 12
   Note that the physical memory size is not needed to solve this problem (and the size provided in the problem does not match the provided page table content).
   - Not enough info (no table entry).
   - 0x992345
   - 0xFF4321
   - Not enough info

7. [Virtual Memory]

5.11.1

Address	Virtual Page	TLB H/M	TLB		
			Valid	Tag	Physical Page
4669	1	TLB miss PT hit PF	1	11	12
			1	7	4
			1	3	6
			1 (last access 0)	1	13
2227	0	TLB miss PT hit	1 (last access 1)	0	5
			1	7	4
			1	3	6
			1 (last access 0)	1	13
13916	3	TLB hit	1 (last access 1)	0	5
			1	7	4
			1 (last access 2)	3	6
			1 (last access 0)	1	13
34587	8	TLB miss PT hit PF	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 2)	3	6
			1 (last access 0)	1	13
48870	11	TLB miss PT hit	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 2)	3	6
			1 (last access 4)	11	12
12608	3	TLB hit	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 5)	3	6
			1 (last access 4)	11	12
49225	12	TLB miss PT miss	1 (last access 6)	12	15
			1 (last access 3)	8	14
			1 (last access 5)	3	6
			1 (last access 4)	11	12

5.11.2

Address	Virtual Page	TLB H/M	TLB		
			Valid	Tag	Physical Page
4669	0	TLB miss PT hit	1	11	12
			1	7	4
			1	3	6
			1 (last access 0)	0	5
2227	0	TLB hit	1	11	12
			1	7	4
			1	3	6
			1 (last access 1)	0	5
13916	0	TLB hit	1	11	12
			1	7	4
			1	3	6
			1 (last access 2)	0	5
34587	2	TLB miss PT hit PF	1 (last access 3)	2	13
			1	7	4
			1	3	6
			1 (last access 2)	0	5
48870	2	TLB hit	1 (last access 4)	2	13
			1	7	4
			1	3	6
			1 (last access 2)	0	5
12608	0	TLB hit	1 (last access 4)	2	13
			1	7	4
			1	3	6
			1 (last access 5)	0	5
49225	3	TLB hit	1 (last access 4)	2	13
			1	7	4
			1 (last axxess 6)	3	6
			1 (last access 5)	0	5

A larger page size reduces the TLB miss rate but can lead to higher fragmentation and lower utilization of the physical memory.