Homework 7 – Memory Hierarchy

Out: 4.7.21
Due: 4.14.21

1. [Memory]
   The following memories are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case? How many bytes are stored?
   a) 8K X 32
   b) 256K X 64
   c) 32M X 32

2. [Memory]
   A 128K X 32 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select.
   a) Assuming that the RAM cell array is square, what is the size of each decoder?
   b) Determine the row and column selection lines that are enabled when the input address is 0x39ABCD.
   c) Why is "squareness" a good assumption?

3. [Memory]
   Using the 64K X 8 RAM chip shown in the slides, design a 512K X 16 RAM system. Show the block diagram.

4. [Cache]
   a) What are the major memory technologies?
   b) What is each one good at?
   c) Why are there multiple memory technologies?

5. [Cache]
   On the internet (e.g., the Micron Technologies web site) find the access time and size of a state-of-the-art
   a) DRAM chip
   b) SRAM chip
   c) FLASH chip

6. [Cache]
   For each part, describe the general characteristics of a program that exhibits:
   a) Very little (or a great deal of) temporal locality of data accesses
   b) Very little (or a great deal of) spatial locality of data accesses
   c) Very little (or a great deal of) temporal locality of instruction accesses
   d) Very little (or a great deal of) spatial locality of instruction accesses