

Development of a beam-based phase feed-forward demonstration at the CLIC Test Facility (CTF3).

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Abstract

This is the abstract TeX for the thesis and the stand-alone abstract.

Dedication.

Acknowledgements

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Contents

1 Phase Monitor Performance	1
1.1 Phase Monitor Design	1
1.2 Phase Monitor Electronics	7
1.3 Resolution Definition	8
1.4 Digitisation of Phase Monitor Signals	10
1.5 Fitting Method	12
1.6 Signal Generator Measurements	13
1.6.1 Experimental Setup	15
1.6.2 Results	15
1.6.3 Mixer Performance	16
1.6.4 Diode Performance	23
1.6.5 Consequences for Normal Operation	25
1.7 Calibrations	30
1.7.1 Calibration on SiS Digitisers	31
1.7.2 Calibration on FONT5a Board	34
1.7.3 Multi-Sample Results	35
1.7.4 Zero Crossing	37
1.8 Phase Shifter Noise	38
1.9 Resolution Measurements	41
1.9.1 Best Resolution	44
1.9.2 With Sample Averaging	44
1.9.3 Dependence of Resolution on LO Phase	45
1.10 Bandwidth	45
1.11 Comparison of Measured Phase Along Pulse	48
1.12 Effect of Variations in Calibration Constant	49
1.13 Dependence on Position	51
2 Setup and Commissioning of the PFF System	57
2.1 Feedforward Controller (FONT5a Board)	57
2.1.1 Implementation of PFF Correction	61
2.1.2 ADC Droop Correction	66
2.1.3 Gain Calculation	70
2.1.4 Effect of Using Small Angle Approximation	72
2.2 Amplifier	74
2.2.1 Design	74

2.2.2	Linearity	78
2.2.3	Shape	79
2.3	Data Acquisition and Signal Processing	83
2.3.1	SiS Digitiser Setup	83
2.3.2	Acquisition Tools	83
2.3.3	Monitoring Tools	83
2.3.4	Time Alignment of Signals	85
2.3.5	Definition of Zero Phase	85
2.4	Kicker and Optics Performance Verification	85
2.4.1	Correction Range	85
2.4.2	Variations Along Pulse	88
2.4.3	Shape	88
2.4.4	Orbit Closure	90
2.5	Correction Output Timing	93
2.5.1	Kicker Cable Lengths	93
2.5.2	Absolute Timing	97
2.5.3	Relative Kicker Timing	102
2.6	Early Phase Feedforward Attempts and Simulations	106
2.6.1	Gain Scans	106
2.6.2	Effect of Limited Correction Range	106

Bibliography

107

List of Figures

1.1	Technical drawing of the phase monitor cavity design [REF]. The length and internal diameter of the monitor is shown., Around the centre of the monitor are the four evenly spaced RF feedthroughs.	2
1.2	Schematic of phase monitor design [REF].	3
1.3	Field distribution of Monopole (TM01) and dipole (TE11) modes in the phase monitor cavities. The dipole mode has both horizontal and vertical components - only the horizontal component is shown.	4
1.4	Annotated picture of the two upstream phase monitors installed in the machine.	6
1.5	Simplified schematic of the phase monitor electronics setup.	7
1.6	Comparison of noise on the output of the SiS and FONT5a ADCs.	11
1.7	Example sine fit to generated data with added random noise.	14
1.8	Response of Mixer 1 to signal generator input.	17
1.9	Response of Diode 1 to signal generator input.	17
1.10	Response of Mixer 2 to signal generator input.	18
1.11	Response of Diode 2 to signal generator input.	18
1.12	Response of Mixer 3 to signal generator input.	19
1.13	Response of Diode 3 to signal generator input.	19
1.14	Sinusoidal fit to mixer responses at 27 dBm input power.	20
1.15	Residuals to sinusoidal fit at 27dBm.[TODO: sample numbers don't relate to previous plots]	20
1.16	Sinusoidal fit to mixer responses at 18 dBm input power.	21
1.17	Linear fit to mixer output voltage vs. input voltage.	22
1.18	Mixer maximum and minimum output voltage vs. input voltage.	24
1.19	Relative amplitude vs. input power of cross-talk on the mixer from the diode.	24
1.20	$\text{sqrt}(\text{Diode})$ vs. input voltage.	25
1.21	Linear fits to $\text{sqrt}(\text{Diode})$ vs. input voltage.	26
1.22	Quadratic fits to Diode vs. input voltage.	26
1.23	Sinusoidal fit to cross-talk on diode at 6 dBm input power.	27
1.24	Sinusoidal fit to cross-talk on diode at 18 dBm input power.	27
1.25	Dependence of the relative amplitude of cross-talk on the diode versus the input power.	28
1.26	Comparison of the oscillation on the mixer and the diode, showing a relative phase offset between the two.	28
1.27	Mon 1 phase along the pulse for each LO phase shifter setting during the calibration.	32

1.28	Mon 2 phase along the pulse for each LO phase shifter setting during the calibration.	32
1.29	Mon 3 phase along the pulse for each LO phase shifter setting during the calibration.	33
1.30	Fits to the mixer output vs. LO phase shifter setting at sample 605 on the SiS digitisers.	33
1.31	Results of a calibration performed on the FONT5a board.	34
1.32	Variation in fitted amplitude along the pulse for each phase monitor.	36
1.33	Variation in fitted offset along the pulse for each phase monitor	36
1.34	Phase monitor resolution using initial setup with digital phase shifters in place.	39
1.35	Phase jitter along the pulse with the nominal electronics setup – Mon 1 connected to the first mixer, and Mon 2 connected to the second mixer.	39
1.36	Phase jitter along pulse with Mon 2 connected to the first mixer and Mon 1 connected to the second mixer.	40
1.37	Phase jitter along pulse with Mon 1 connected to the first mixer and Mon 2 connected to the third mixer.	41
1.38	Phase jitter along pulse with the LO swapped between the first mixer and the second mixer.	42
1.39	Phase jitter along pulse with the LO swapped between the third mixer and the first mixer.	42
1.40	Phase jitter along pulse after installation of the mechanical phase shifters.	43
1.41	<code>bestResolution</code>	44
1.42	Effect on resolution by averaging samples.	45
1.43	Resolution.	46
1.44	Resolution.	46
1.45	Response of Mixer 3 to a jump in phase in the middle of the pulse.	47
1.46	Comparison of phase along the pulse in the three PFF phase monitors and an alternative phase measurement from a PETS.	48
1.47	Comparison of Mon 1 and Mon 2 phase along the pulse, with Mon 2 rotated by 2.1° about a time of 850 ns on the horizontal axis.	50
1.48	Difference between Mon 1 and Mon 2 phase along the pulse with and without Mon 2 rotated.	50
1.49	Effect of using a varying calibration constant on the upstream phase.	51
1.50	Effect of using a varying calibration constant on the downstream phase.	52
1.51	Mon 1 and Mon 2 phase dependence on horizontal position during scan.	54
1.52	Mon 1 and Mon 2 diode dependence on horizontal position during scan.	54
1.53	Fit to difference between Mon 1 and Mon 2 phase versus horizontal position.	56
1.54	Mon 1 and Mon 2 dependence on horizontal position during scan.	56
2.1	racks	58

2.2	Front panel of the FONT5a board. All the connectors relevant to PFF operation are highlighted, the remaining connectors are not used at CTF3. All connectors are BNC apart from the power connector, RS232 serial port used to communicate with the LabVIEW data acquisition system (DAQ) and the JTAG connection used to program the firmware on the FPGA. The use of the ADCs, DACs and timing (trigger and clock) connections is summarised in Figure 2.4.	60
2.3	Diode output along the pulse with the IIR filter off and on.	61
2.4	Schematic of connections to and outputs from the FONT5a board, as well as the PFF calculation in firmware in the case where the diode is used. If the diode is not used the ADC1 input is not required.	62
2.5	Diode output along the pulse with the IIR filter off and on.	66
2.6	Exponential fit to diode droop.	67
2.7	Residuals between diode exponential fit and actual diode output.	68
2.8	Diode output along the pulse with the IIR filter off and on. Zoomed in. . . .	69
2.9	Phase along the pulse with the IIR filter off and on.	70
2.10	Difference between the phase reconstruction method used in the PFF algorithm on the FONT5a board (with the small angle approximation) and the full reconstruction used with data acquired from the SiS digitisers.	73
2.11	Achievable PFF jitter versus phase offset for full phase reconstruction and with the small angle approximation.	73
2.12	Front panel of the amplifier. Inputs to the amplifier are highlighted in green, drive outputs in red and monitoring outputs in blue. Inputs to the control module are the trigger (T) and the two DAC outputs from the FONT5a board used to determine the drive to the left (L) and right (R) sides. Each side of the amplifier has two pairs of drive outputs and terminators, A and B. The signal returning to each of the terminators can be observed on their corresponding monitoring outputs. The monitoring output on the control module (ON) shows the $1.4 \mu s$ time during which the amplifiers are able to provide their output. Not highlighted in the figure are the 24 V, 1.1 A power connector at the top of the control module, and also the three [TODO: what type?] connectors used to communicate between the control module and drive modules.	76
2.13	Simplified flow diagram showing the connections between the FONT5a board, the amplifier and the kickers. The kickers are inserted between the drive and terminator modules for the purposes of the diagram, but in reality the terminator modules neighbour the drive modules in the same unit as seen in Figure 2.12. Note that the A and B outputs on each side always have opposite polarity, as needed to create a large potential difference between the kicker strips.	77
2.14	Amplifier output vs. input.	79
2.15	Residual between amplifier output and linear fit.	80
2.16	Amp L along pulse at 1 V input	81
2.17	Amp R along pulse at 1 V input	82
2.18	Flatness of potential difference sent to kickers.	83

2.19	Residual kick along pulse.	84
2.20	Residual kick along pulse: deviation from flat.	84
2.21	Phase shift versus amplifier input voltage.	86
2.22	Phase shift versus amplifier input voltage.	86
2.23	Traces relative timing scan.	89
2.24	Traces relative timing scan.	89
2.25	Horizontal orbit offset in and around the TL2 chicane at different input voltages sent to the amplifier.	91
2.26	Orbit in the TL2 chicane at 1 V amplifier input for the BPM data, nominal model and model taking in to account the difference in amplifier output voltage to each kicker.	91
2.27	Orbit in the TL2 chicane at 1 V amplifier input for the BPM data, nominal model and model taking in to account the quadrupole currents in the real machine setup.	92
2.28	Cabling setup for cables between the amplifier and kickers.	96
2.29	Beam pickup on kicker strips as seen on amplifier monitoring signals.	97
2.30	Output delay of 0 clock cycles. Full pulse.	98
2.31	Output delay scan, end of pulse.	99
2.32	Output delay of 7 clock cycles. Full pulse.	100
2.33	Output delay of 7 clock cycles. End of pulse.	100
2.34	Kick output with no delay as seen on BPM and phase signals.	102
2.35	Fit time offset between kick and beam at different output delays.	103
2.36	Alignment between BPMs and phase signals with optimal delay applied in analysis.	103
2.37	Simulated response to offset kicks.	104
2.38	Measured BPM offset for different relative kick delays.	105
2.39	Fitted peak BPM offset vs. relative kick delay.	106

List of Tables

1.1	Power of the phase monitor signals (hybrid sum outputs) measured in the klystron gallery prior to being processed by the phase monitor electronics.	5
1.2	Specifications of the ADCs on the FONT5a board and SiS digitisers.	11
1.3	ADC jitter on the FONT5a board, SiS digitisers and with the mixer outputs amplified prior to the SiS digitisers expressed in terms of ADC counts, volts and equivalent phase jitter.	12
1.4	Typical upstream phase and energy conditions at CTF3.	13
1.5	Fit parameters from the calibration on the SiS digitisers for each monitor.	31
1.6	Fit parameters from the calibration for each monitor on the FONT5a board.	35
1.7	Standard deviation in calibration fit parameters along the pulse.	37
1.8	Phase shifter setting to obtain the zero crossing for each mixer output and the fit parameters needed to calculate them.	38
1.9	Comparison of phase jitter along the pulse for each measurement with different setups of the electronics. Each row corresponds to the results of one dataset. The left hand side of the table shows the results from Mon 1 in that dataset, and the right hand side of the table the results from Mon 2. Bold text indicates the lower jitter value in that dataset, all of which use LO 1.	43
1.10	Distance of the upstream phase monitors and following BPM CT.0430 to the corrector CT.0360 before the phase monitors.	53
2.1	IIR filter weights for the FONT5a board ADCs.	69
2.2	Feedforward results using combined data from 20th November 2015.	80
2.3	Phase shift at +1 volt input to the amplifier.	85
2.4	Lengths of cables between the amplifier and the patch panel.	95
2.5	Lengths of cables between the patch panel and the kickers.	95

Glossary

Item1 Description.

Item2 Description.

Item3 Description.

Chapter 1

Phase Monitor Performance

In order to successfully correct the phase with the PFF system it is clearly necessary to be able to accurately measure the phase, whilst meeting the low latency (380 ns for the complete system) and high bandwidth (30 MHz) requirements of the correction. Purpose-built phase monitors for the PFF system have been designed and constructed by INFN, Italy [REF]. Three of these monitors are currently installed at CTF3 — two in the CT line at the end of the linac and one after the TL2 chicane in the TBL line. The approximate positions of the monitors are shown on the CTF3 layout in Figure [REF]. The two “upstream” phase monitors in the CT line will be referred to as Mon 1 and Mon 2 (Mon 1 being before Mon 2 in the beam line) in this chapter. The “downstream” phase monitor in TBL will be referred to as Mon 3. Mon 1 is normally used as the PFF correction input, with the neighbouring Mon 2 used for performance cross-checks. Mon 3 is then used to measure the effect of the PFF correction. In the rest of the thesis the phase measurements are generally simply referred to as being from either one of the upstream phase monitors, or the downstream monitor.

The chapter begins with an overview of the design and installation of the phase monitors themselves as well as the associated electronics. The remainder of the chapter then focuses on operational procedures, measurements of the performance of the phase monitors and the changes that have been made in order to improve it. The headline result for the chapter is the achieved resolution of below 0.14° in Section 1.9, which is derived to be necessary to be able to achieve the targeted 0.2° corrected phase jitter in Section 1.3. Several effects have also been identified that can still degrade the accuracy of the phase measurement, such as the position dependence seen in Section 1.13. These are the first areas that should be looked at if an improvement in phase monitor performance is necessary for future PFF tests.

1.1 Phase Monitor Design

The phase monitors are cylindrical cavities with a length of approximately 19 cm and an internal diameter of 23 mm, as shown in Figure 1.1. When a charged beam traverses a cavity the interaction of the beam with the cavity walls creates electromagnetic fields inside the

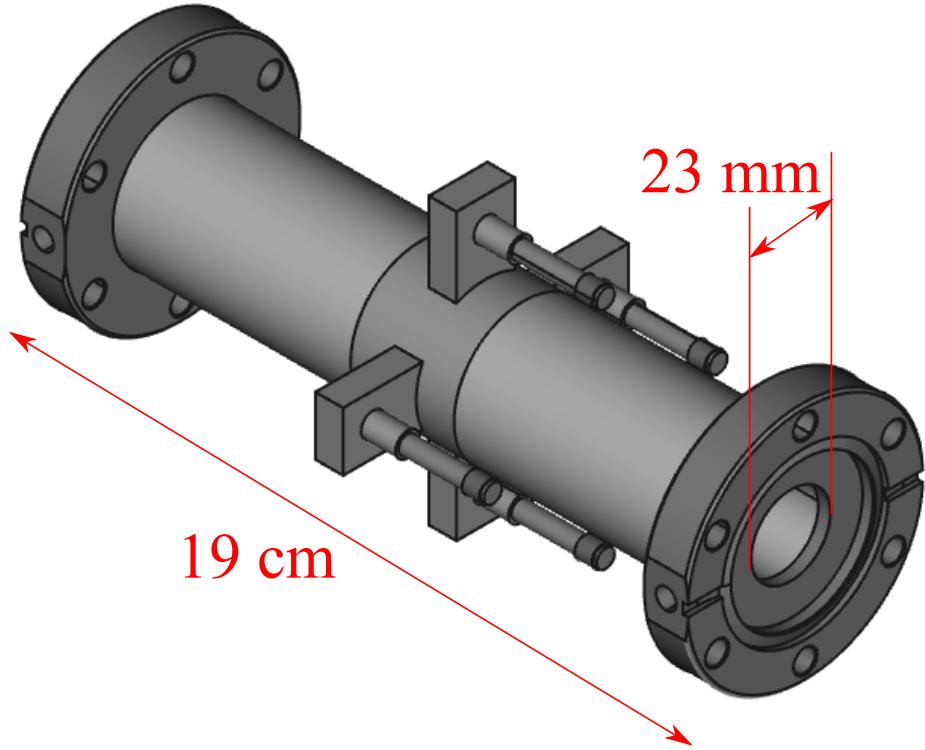


Figure 1.1: Technical drawing of the phase monitor cavity design [REF]. The length and internal diameter of the monitor is shown., Around the centre of the monitor are the four evenly spaced RF feedthroughs.

cavity. The amplitude of the induced fields depends both on the bunch charge and the bunch length [REF]. Small ridges (called notch filters) in the cavity create a volume resonating at 12 GHz (the CLIC combined bunch frequency) that contains the beam induced fields and reflects any stray 12 GHz fields not associated with the beam outside the cavity. This is shown in Figure 1.2. Four rectangular slots, arranged in horizontal and vertical pairs, around the mid-point of the cavity are then used to extract the beam induced resonant fields. The fields leaving the cavity are transported in short rectangular waveguides before a transition to a 50Ω coaxial cable via an RF feedthrough [REF]. The output of the phase monitor cavities is therefore four 12 GHz signals whose time structure depends on the arrival time, or phase, of the drive beam bunches.

The solutions to Maxwell's equations in cavities such as this give a discrete set of transverse electric (TE) and transverse magnetic (TM) modes dependent on the geometry of the cavity [REF]. TE modes are characterised by having only transverse electric field components, and no longitudinal electric field component, whereas TM modes have only transverse magnetic field components and no longitudinal magnetic field component. Each TM and TE mode has an associated cutoff frequency dependent on the number of half-period variations, n and m , in the field horizontally and vertically across the cavity respectively. The amplitude of the 12 GHz signals output from the cavity will contain components of each TM and TE mode with a cutoff frequency below 12 GHz. For cylindrical cavities the cutoff frequency of

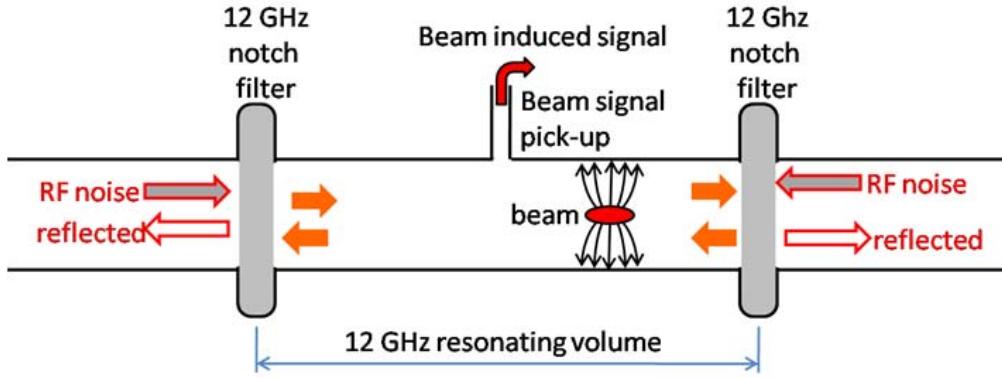


Figure 1.2: Schematic of phase monitor design [REF].

the TM is defined as [REF]:

$$f_{nm} = \frac{c}{2\pi} \frac{p_{nm}}{a} \quad (1.1)$$

And for the TE modes as:

$$f_{nm} = \frac{c}{2\pi} \frac{p'_{nm}}{a} \quad (1.2)$$

Where a is the radius of the cavity, p_{nm} is the m^{th} zero of the Bessel function $J_n(x)$, and p'_{nm} is the m^{th} zero of the derivative of the Bessel function $J'_n(x)$ [REF]. The beam pipe around the location of the phase monitors at CTF3 is usually 4 cm in diameter, and a cavity of this size would support six separate TM or TE modes with a cutoff frequency below 12 GHz [REF]. It is for this reason that the phase monitor diameter was reduced to 23 mm, where only two modes are present: TM01 ($n = 0$, $m = 1$, $p_{01} = 2.4$) and TE11 ($n = 1$, $m = 1$, $p'_{11} = 1.8$).

TM01 is referred to as the monopole mode and TE11 as the dipole mode. The induced field distribution resulting from a bunch entering the cavity for both modes is shown in Figure 1.3. The precise expressions for each field distribution can be found in [REF]. When the beam has been correctly setup it should enter the phase monitor cavity close to its centre. For small (horizontal or vertical) offsets between the beam position and the cavity centre there is no dependence of the monopole mode amplitude on the incoming beam position. However, the amplitude of the dipole mode does depend on the beam position, even for small offsets from the cavity centre. This means the amplitude of any of the four individual RF outputs from the monitor will have a position dependence. This property is used in cavity beam position monitors (BPMs) [REF], but is undesirable for a phase monitor where the measurement should be position independent. For a 1 mm beam position offset the dipole mode is expected to have around 10% the amplitude of the monopole mode [REF].

To remove the unwanted dipole mode the horizontal and vertical pairs of outputs from the cavities can be combined, as the mode is symmetric and has equal magnitude but opposite sign on each side of the cavity. As the CTF3 beam is generally more stable in the vertical plane (as the majority of bends in the beam line are horizontal the energy related orbit jitter resulting from dispersion is larger in the horizontal plane) the vertical pair of RF feedthroughs from the monitors are normally used. The two outputs are summed using 180 degree hybrids [REF] installed next to the phase monitor cavities in the machine hall.

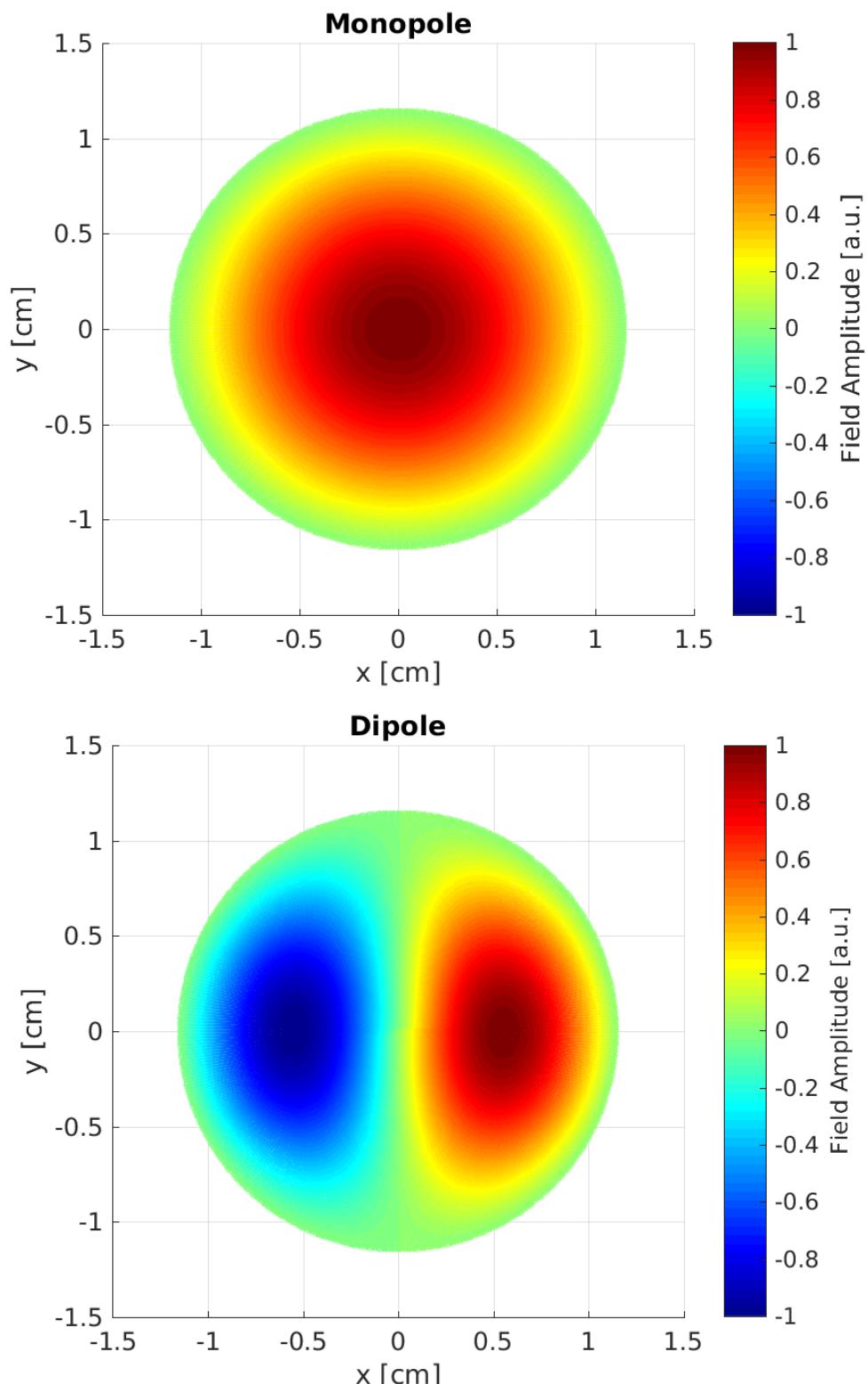


Figure 1.3: Field distribution of Monopole (TM01) and dipole (TE11) modes in the phase monitor cavities. The dipole mode has both horizontal and vertical components - only the horizontal component is shown.

Monitor	Power
Mon 1	27.6 dBm
Mon 2	29.8 dBm
Mon 3	24.5 dBm

Table 1.1: Power of the phase monitor signals (hybrid sum outputs) measured in the klystron gallery prior to being processed by the phase monitor electronics.

The horizontal pair is also instrumented in the same way but the outputs are typically not used. For an ideal (perfectly symmetric) cavity and hybrid this would create an output with only the position independent monopole mode present. In reality small misalignments, for example in the waveguides and RF feedthroughs, cause slight asymmetries in the cavity and signal combination which leaves a small residual dipole component. The signal combination in the hybrids is expected to reduce the dipole amplitude by a further 20 dB at a 1 mm offset, giving a final amplitude around 1% of the monopole mode. The remaining position dependence of the phase measurement is discussed in Section 1.13. How the output from the hybrids is processed to calculate the phase is discussed in the next section.

Figure 1.4 shows the installation of the upstream phase monitors in the CT line. The installation allows up to three phase monitors to be installed neighbouring each other, with the current two monitors installed in the first and third slots leaving approximately a 20 cm gap between the two. The connections between the four RF feedthroughs on the monitors and the hybrids fixed underneath the monitors can be seen in the figure, with the hybrids combining the horizontal pairs visible and two further hybrids placed on the other side of the beam line for the vertical pairs. The outputs from the hybrids are routed up to the klystron gallery on the floor above the accelerator hall, where they are processed and used for the PFF inputs. For reference the power level of the three phase monitor signals as measured once they reach the klystron gallery are quoted in Table 1.1. These are useful to interpret the results of Section 1.6, for example.

1.1 Phase Monitor Design

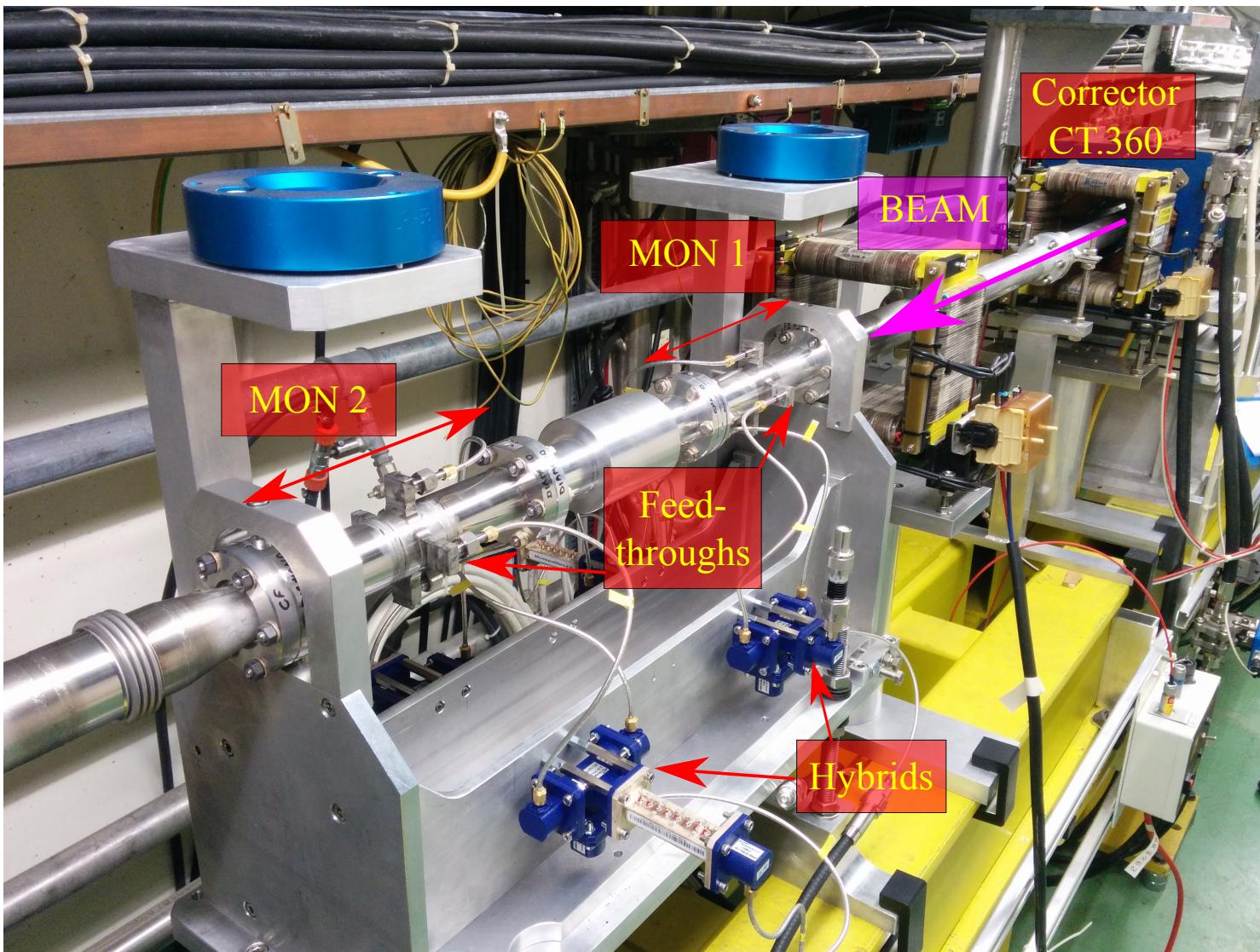


Figure 1.4: Annotated picture of the two upstream phase monitors installed in the machine.

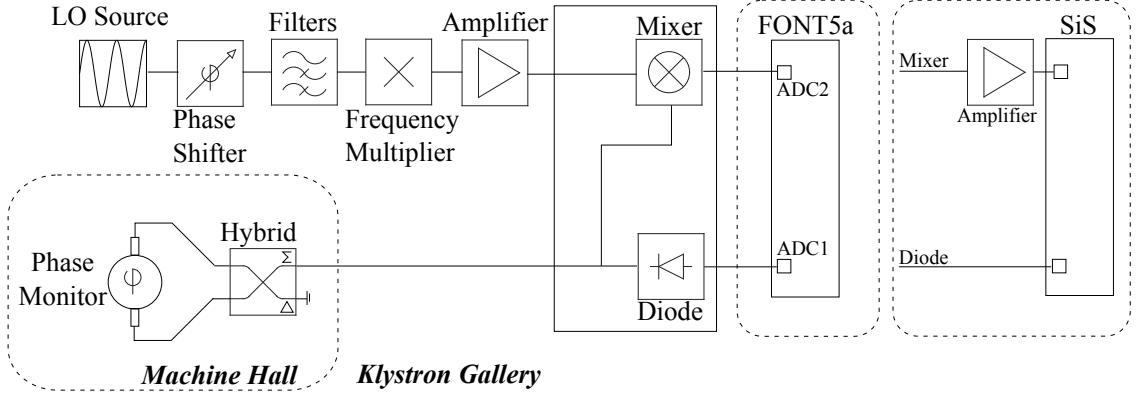


Figure 1.5: Simplified schematic of the phase monitor electronics setup.

1.2 Phase Monitor Electronics

LO should have 5fs stability (0.02 degrees jitter)? What is the source of the LO?

Mixer output

$$RF(t) = A_{RF}(t) \cos[\omega_{RF}t + \phi(t)] \quad (1.3)$$

$$LO(t) = A_{LO} \cos[\omega_{LO}t] \quad (1.4)$$

mixer multiplies

$$\text{Mixer}(t) = RF(t) \times LO(t) \quad (1.5)$$

$$\text{Mixer}(t) = A_{RF}(t)A_{LO} \cos[\omega_{RF}t + \phi(t)] \cos[\omega_{LO}t] \quad (1.6)$$

trig identities

$$\text{Mixer}(t) = \frac{A_{RF}(t)A_{LO}}{2} \{ \cos[(\omega_{LO} + \omega_{RF})t + \phi(t)] + \cos[(\omega_{LO} - \omega_{RF})t + \phi(t)] \} \quad (1.7)$$

filter high frequency

$$\text{Mixer}(t) = \frac{A_{RF}(t)A_{LO}}{2} \cos[(\omega_{LO} - \omega_{RF})t + \phi(t)] \quad (1.8)$$

LO frequency and RF frequency are the same

$$\text{Mixer}(t) = \frac{A_{RF}(t)A_{LO}}{2} \cos[\phi(t)] \quad (1.9)$$

Diode used to measure A_{RF}

$$\text{Diode}(t) = A_{RF}(t)^2 \quad (1.10)$$

The phase can be reconstructed by

$$\frac{\text{Mixer}(t)}{\sqrt{\text{Diode}(t)}} = A \cos[\phi(t)] \quad (1.11)$$

$$\phi(t) = \arccos \left[\frac{\text{Mixer}(t)}{A \sqrt{\text{Diode}(t)}} \right] \quad (1.12)$$

Beam/monitor frequency is 11.994 GHz.

Performance limited by: Device non-linearity – normally better for lower input power
 Signal to noise – better for high power Therefore, split signal to 8 mixers – low input power to each one – to reduce effect of non-linearities. Then sum up results of each mixer to improve signal to noise.

Monitor - \downarrow attenuator? - \downarrow Hybrid sum - \downarrow attenuator? - \downarrow attenuator in gallery - \downarrow mixer RF input LO - \downarrow phase shifter - \downarrow multiplier - \downarrow amplifier - \downarrow mixer LO input Mixer output - \downarrow attenuator - \downarrow amplifier - \downarrow SiS OR - \downarrow attenuator- \downarrow FONT Diode output - \downarrow SiS/FONT

Latest power measurements:

LO1 22.6 dBm LO2 23.6 dBm LO3 25.5 dBm

latency monitor - \downarrow hybrid - \downarrow electronics - \downarrow out = 50 ns

1.3 Resolution Definition

The performance of the PFF system clearly depends on the accuracy to which the phase can be measured. Many of the measurements in this chapter are therefore focused on the phase monitor resolution, or more precisely on the resolution of the combined phase monitor and electronics setup. The resolution is defined as the jitter between the measured phase and the true beam phase. This can be calculated by comparing the difference between the measured phase of two monitors. This is why two phase monitors, Mon 1 and Mon 2 are installed neighbouring each other in the upstream system in the CT line. The beam phase should be identical in these two monitors thus their measurements can always be compared to derive the resolution.

The precise derivation of the resolution dependent on the measurement of two monitors is as follows. First, the measured phase, $\phi_x(t)$ and $\phi_y(t)$, in two monitors at time t can be defined as:

$$\phi_x(t) = \phi_b(t) + n_x(t) \quad (1.13)$$

$$\phi_y(t) = \phi_b(t) + n_y(t) \quad (1.14)$$

Where $\phi_b(t)$ is the true beam phase and $n_x(t)$ and $n_y(t)$ is the noise on the measurement at that time. The time dependence will not be written explicitly from this point. These equations assume the beam phase is identical in each monitor, as should be the case for Mon 1 and Mon 2. The variance of each phase monitor measurement can then be derived from the equations above by adding the variance of the beam phase and the noise in quadrature:

$$\sigma_x^2 = \sigma_b^2 + \sigma_{nx}^2 \quad (1.15)$$

$$\sigma_y^2 = \sigma_b^2 + \sigma_{ny}^2 \quad (1.16)$$

Where σ_x and σ_y are the phase jitters measured by each phase monitor, σ_b is the true beam phase jitter and σ_{nx} and σ_{ny} are the phase monitor resolutions. Assuming each phase monitor has the same resolution, σ_n , this can be simplified to $\sigma_x^2 = \sigma_y^2 = \sigma_b^2 + \sigma_n^2$.

The quantity of interest for calculating the phase monitor resolution is the jitter in the difference between the two measured phases, σ_{x-y} . The variance of the difference between two correlated variables is defined as:

$$\sigma_{x-y}^2 = \sigma_x^2 + \sigma_y^2 - 2\sigma_x\sigma_y\rho_{xy} \quad (1.17)$$

$$(1.18)$$

Where ρ_{xy} is the correlation between the phase measurement of x and y . Substituting in the previously derived expressions for σ_x and σ_y this becomes:

$$\sigma_{x-y}^2 = 2(\sigma_b^2 + \sigma_n^2)(1 - \rho_{xy}) \quad (1.19)$$

The correlation coefficient ρ_{xy} depends on the covariance between x and y , $\text{cov}[x, y]$, as follows:

$$\rho_{xy} = \frac{\text{cov}[x, y]}{\sigma_x\sigma_y} = \frac{\text{cov}[x, y]}{\sigma_b^2 + \sigma_n^2} \quad (1.20)$$

$$(1.21)$$

Where the covariance is defined as:

$$\text{cov}[x, y] = \frac{1}{N} \sum_{i=1}^N \phi_{xi}\phi_{yi} \quad (1.22)$$

$$(1.23)$$

Substituting in the expressions for ϕ_x and ϕ_y above and separating the terms in the sum then gives the following expression for the covariance of x and y :

$$\begin{aligned} \text{cov}[x, y] &= \frac{1}{N} \sum_{i=1}^N (\phi_{bi} + n_{xi})(\phi_{bi} + n_{yi}) \\ \text{cov}[x, y] &= \frac{1}{N} \sum_{i=1}^N \phi_{bi}^2 + \frac{1}{N} \sum_{i=1}^N \phi_{bi}n_{xi} + \frac{1}{N} \sum_{i=1}^N \phi_{bi}n_{yi} + \frac{1}{N} \sum_{i=1}^N n_{xi}n_{yi} \end{aligned} \quad (1.24)$$

The first term is the definition of the variance of the beam phase, σ_b^2 . The remaining terms are the covariance between the beam phase and the monitor noises, and the covariance between the two monitor noises. Assuming the noise is uncorrelated all these terms are zero. The remaining equation for the covariance between x and y is therefore simply: $\text{cov}[x, y] = \sigma_b^2$. Finally, the correlation between the phase measurement of x and y becomes:

$$\rho_{xy} = \frac{\sigma_b^2}{\sigma_b^2 + \sigma_n^2} \quad (1.25)$$

Substituting this expression for the correlation in to the derived equation for the variance between the two phase measurements gives the following simple dependence on the phase monitor resolution:

$$\begin{aligned} \sigma_{x-y}^2 &= 2(\sigma_b^2 + \sigma_n^2) \left(1 - \frac{\sigma_b^2}{\sigma_b^2 + \sigma_n^2}\right) \\ \sigma_{x-y}^2 &= 2\sigma_n^2 \end{aligned} \quad (1.26)$$

Finally, the resolution is defined as:

$$\sigma_n = \frac{\sigma_{x-y}}{\sqrt{2}} \quad (1.27)$$

In terms of a resolution calculation these equations only apply to the two upstream phase monitors. All the resolution values quoted in this chapter use this equation and the difference between the measurement of Mon 1 and Mon 2.

However, as the act of the PFF system can also be thought of as subtracting two phases (removing the upstream phase from the downstream phase) the same equations can be directly applied to determine the limitations that the phase monitor resolution places on the PFF performance. Equation 1.26 shows that the lowest possible corrected downstream phase jitter is a factor $\sqrt{2}$ times larger than the phase monitor resolution. In order to reduce the downstream phase jitter to the CLIC target of 0.2° the phase monitor resolution must therefore be better than 0.14° . Equation 1.25 shows that with this 0.14° resolution and a typical beam phase jitter of 0.8° (Section ??) the measured correlation between two phase monitor measurements would be 97%.

1.4 Digitisation of Phase Monitor Signals

The mixer and diode outputs from the phase monitor electronics must be digitised on analogue to digital converters (ADCs) so the signals can be processed and used for the PFF correction and offline data analysis. Two different types of ADCs have been used to digitise the phase monitor signals — the Texas Instruments ADS5474 ADCs [REF] on the purpose-built FONT5a board used as the PFF controller and a commercially available SiS 3320 digitiser [REF]. The design and use of the FONT5a board is discussed in more detail in Section 2.1. Table 1.2 summarises the specifications of each type of ADC.

The SiS digitisers are used in addition to the FONT5a board as the PFF correction running on the FONT5a board is operated as a standalone system independent from other acquisition systems at CTF3. The PFF algorithm requires only the signals from one of the upstream phase monitors to be connected to the FONT5a board, with the convention being to use Mon 1. Mon 2 and Mon 3 are then normally connected to the SiS digitisers instead. The SiS digitisers are setup with the same trigger and sampling frequency (192 MHz) used for other signals at CTF3, and data from them can be acquired together with other devices using the standard systems in place at CTF3. This allows the Mon 2 and Mon 3 signals to be easily compared to other measurements, such as beam position signals, which has been indispensable for optimising the setup of the PFF system and in particular the phase propagation (Chater ??).

Digitising the phase monitor signals contributes additional noise to the overall phase monitor electronics setup. The purpose of this section is to ensure that the digitiser noise makes only a negligible contribution to the resolution on the phase measurement. The main parameters of interest needed to determine this are the input range and resolution of the ADCs, with the SiS ADCs being 12-bit with a range of ± 2.5 V and the FONT5a ADCs being

Digitiser	No. ADCs	Resolution	Input Range	Sampling Rate	Bandwidth
SiS 3320	8	12-bit	± 2.5 V	up to 250 MHz	100 MHz
FONT5a	9	14-bit (13-bit used)	± 0.5 V	up to 400 MHz	1.4 GHz

Table 1.2: Specifications of the ADCs on the FONT5a board and SiS digitisers.

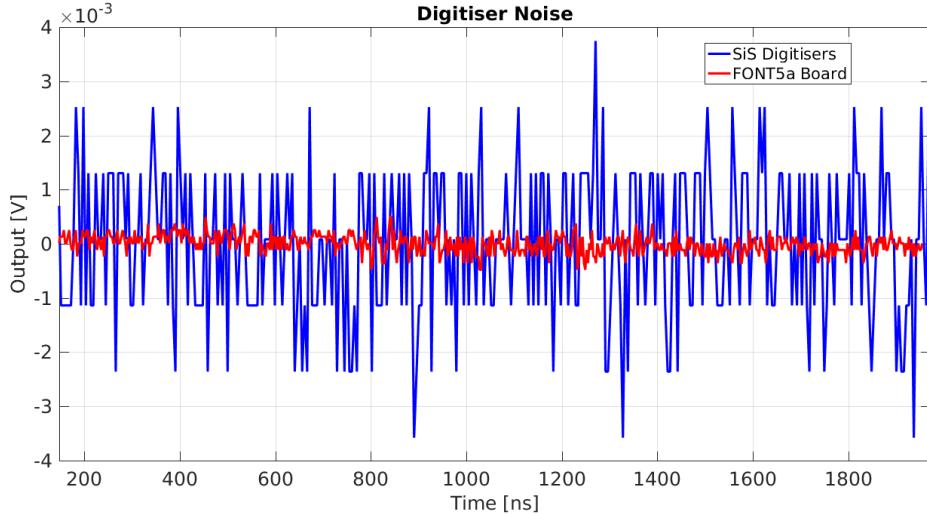


Figure 1.6: Comparison of noise on the output of the SiS and FONT5a ADCs.

13-bit with an input range of ± 0.5 V. The full 5 V peak-to-peak input range of the SiS ADCs is therefore split across $2^{12} = 4096$ values, or ADC ‘counts’, with each count corresponding to roughly 1.2 mV. The equivalent 1 V peak-to-peak range and $2^{13} = 8192$ counts of the FONT5a board corresponds to a factor 10 lower interval of 0.12 mV per ADC count. The voltage jitter added by the digitisation of the phase monitor signals cannot be expected to be better than 1 count. This already indicates that the FONT5a board should give a much lower contribution to the phase resolution than the SiS digitisers.

Figure 1.6 shows the ADC noise, converted from counts in to an equivalent voltage, for both the SiS and FONT5a ADCs. As expected the noise on the FONT5a board is much lower than on the SiS digitisers. The actual ADC jitter values are 1.47 ± 0.04 counts or 0.179 ± 0.005 mV on the FONT5a board, and 1.11 ± 0.03 counts or 1.36 ± 0.03 mV on the SiS digitisers. These values can be converted in to an equivalent phase jitter using the phase reconstruction method described later in Section 1.6.5 and the monitor calibration constants determined in Section 1.7. For reference the peak output of the three phase monitor mixers varies between approximately 400 mV and 500 mV, which is well matched to the input range of the FONT5a ADCs. Taking the worst case scenario of Mon 3, which gives the lowest output voltage, the ADC jitter corresponds to $0.0245 \pm 0.0007^\circ$ on the FONT5a board but $0.198 \pm 0.005^\circ$ on the SiS digitisers. These values are summarised in Table 1.3.

As derived in the previous section the phase resolution must be better than 0.14° in order to achieve a corrected downstream phase jitter of 0.2° with the PFF system. The $\sim 0.02^\circ$ contribution of ADC noise on the FONT5a board is therefore insignificant compared to the resolution requirements. However, although it does not directly impact the PFF performance

Digitiser	Jitter [counts]	Jitter [mV]	Phase Jitter [degrees]
FONT5a	1.47 ± 0.04	0.179 ± 0.005	0.0245 ± 0.0007
SiS 3320	1.11 ± 0.03	1.36 ± 0.03	0.198 ± 0.005
SiS 3320 Amplified	1.11 ± 0.03	1.36 ± 0.03	0.078 ± 0.002

Table 1.3: ADC jitter on the FONT5a board, SiS digitisers and with the mixer outputs amplified prior to the SiS digitisers expressed in terms of ADC counts, volts and equivalent phase jitter.

the $\sim 0.2^\circ$ ADC jitter on the SiS digitisers would greatly degrade the resolution of the measurements of Mon 2 and Mon 3 usually connected to the SiS digitisers and used for offline data analysis of the PFF results.

The high phase jitter contribution from the SiS digitisers originates from the roughly 500 mV maximum mixer output being much lower than the SiS ADC range of ± 2.5 V. In order to rectify this the mixer outputs are boosted by roughly a factor 2.5 in voltage using an amplifier prior to the SiS digitisers. The specifications of the amplifier used are documented in [REF]. With the amplifier in place the peak signal level sent to the SiS digitisers is around 1 V, and the equivalent phase jitter is reduced to $0.078 \pm 0.002^\circ$. This no longer prevents 0.14° resolution from being achieved on measurements using the SiS digitisers, as proven later in Section 1.9. A small further improvement in measured resolution could be achieved using a different amplifier and boosting the peak output voltage closer to 2 V.

1.5 Fitting Method

Due to the dependence of the mixer output on $\cos(\phi)$ as seen in Section 1.2, many of the measurements in this chapter require a sinusoidal fit of the form:

$$y = A \sin(bx + c) + d \quad (1.28)$$

The use of sine rather than cosine makes no difference to the fitted amplitude, A , and offset, d which are usually the only parameters of interest in this chapter. It is also convenient to consider a mixer output of zero to correspond to zero phase (rather than 90° as in Equation 1.11). All the fits of this type have been performed using a weighted nonlinear least squares fit implemented in MatLab fitting libraries [?]. Each data point is weighted by the inverse of its standard error squared.

Care must be taken to select suitable initial values for the four parameters in the fit in order to avoid local minima and ensure a reasonable fit. This is particularly important for a sinusoidal fit as there are many solutions with different frequencies and phase offsets that can match the data. The frequency, b , is the most critical parameter but for all the applications in this chapter this is already known, e.g. from the properties of the used phase

Parameter	Value	Initial	Fit
A	1	1.03	0.99 ± 0.02
b	1	1	1.00 ± 0.02
c	1	0.81	1.00 ± 0.06
d	1	0.99	0.99 ± 0.02

Table 1.4: Typical upstream phase and energy conditions at CTF3.

shifters. Initial values for the three remaining parameters are estimated as follows:

$$A = \frac{\max(y) - \min(y)}{2} \quad (1.29)$$

$$d = \frac{\max(y) + \min(y)}{2} \quad (1.30)$$

$$c = \arcsin\left(\frac{y - d}{A}\right) - bx \quad (1.31)$$

The initial amplitude, A , and offset, d , of the sine curve are simply determined by comparing the minimum and maximum output. These initial estimates are therefore highly biased by any large outliers around the minimum and maximum output, but this is rarely the case for the application here and these simple estimators are sufficient. Rearranging Equation 1.28 gives the expression for c above. Due to its use of \arcsin the equation is only valid in the first and fourth quadrants, between $-\pi/2$ and $+\pi/2$ where the gradient of the sine curve is positive. The y value at each data point is compared to its neighbours to determine whether it is on the rising slope. The initial value of c is the mean value calculated across all the data points that meet this criteria.

Figure 1.7 and Table 1.4 show the results of an example fit using this approach. An initial distribution of points with $y = \sin(x + 1) + 1$ is used ($A = b = c = d = 1$), with random noise added. b is assumed to be known, as is normal. The initial estimates for A and d are within a few percent of their true value. The initial estimate for c is within 20% of the correct value. After fitting all four parameters are in agreement with the expected values within error bars.

1.6 Signal Generator Measurements

Measurements have been taken using a 12 GHz signal generator to determine the performance of the three sets of phase monitor electronics independently from the phase monitors themselves. In particular, these tests were focused on identifying the saturation and cross-talk characteristics of the output mixer and diode signals in order to determine a suitable input power range to use during normal operation.

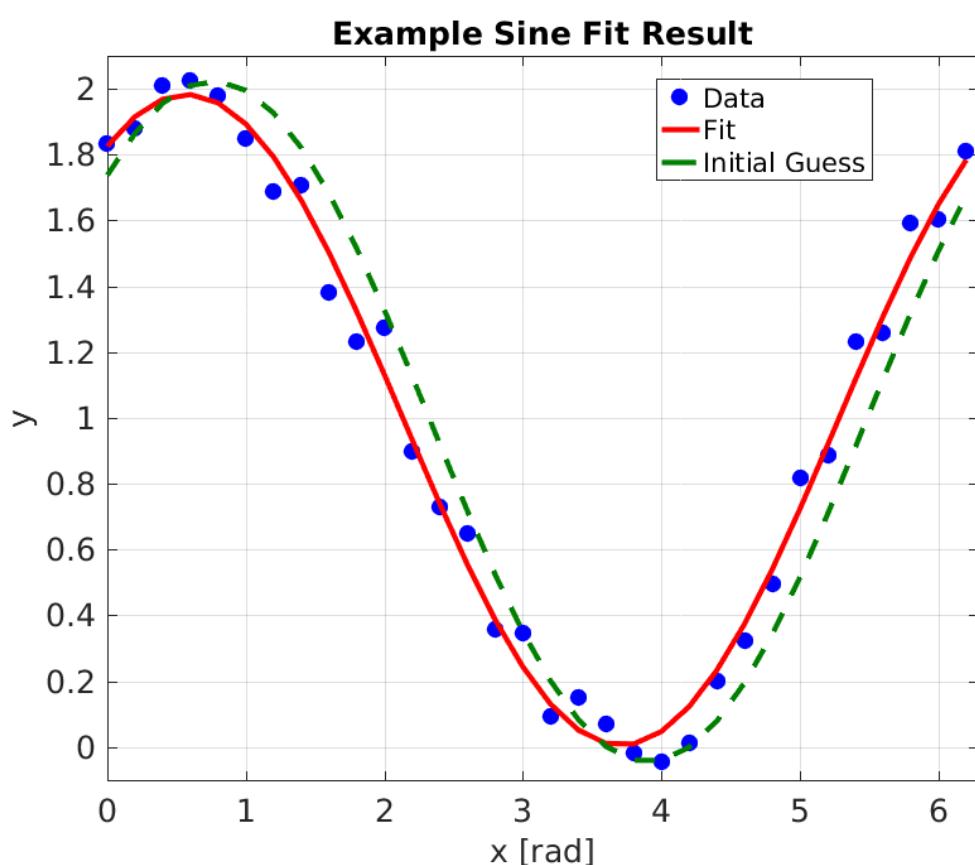


Figure 1.7: Example sine fit to generated data with added random noise.

1.6.1 Experimental Setup

Two changes were made to the setup shown in Figure [REF] for these tests. Firstly, the beam induced signal from the phase monitors usually connected to the RF port of the mixers is replaced by the output from a 12 GHz signal generator. To be able to reach the same input power levels as the beam signals the signal generator output is amplified using a [TODO:amplifierInfo]. This allows the input power to the mixers to be varied in a wide range between 0 and 33dBm, or between 0.2 and 10.0 V in terms of voltage. The precise power sent to the mixer is verified between each measurement using a power meter.

Secondly, the diode outputs were amplified during these tests (using the same amplifier introduced in Section ??) by a factor 10 in voltage to reduce digitiser noise in the measurement. The non-amplified peak diode output is therefore 170 mV, rather than the 1.7 V seen in the plots in this section. The ± 500 mV mixer outputs have not been amplified. Usually the mixer output is amplified and the diode not amplified, as in Figure [REF], for reasons that will become clear later in this chapter.

There are some differences between the properties of the generated signal and the beam signal that would be used in normal operation. Firstly, unlike the pulsed beam signal the used generated signal is continuous. It has been verified that the response of the mixers is equivalent for both the continuous and pulsed signals, at least in terms of output power and saturation levels [REF]. The cross-talk properties are difficult to characterise with beam based measurements alone, but assumed to be similar.

Secondly, the phase of the generated signal does not vary with time, compared to the beam signal which has a large $\sim 40^\circ$ phase sag along the pulse and much larger phase jitter. If the signal generator was used at the same frequency as the beam and LO signals, 11.994 GHz, the mixer output would therefore be constant as it depends only on the static phase as per Equation 1.9. Instead, a generated signal with a slightly lower frequency of 11.991 GHz has been used. From Equation 1.8 it can be seen that in this case the mixer output voltage is sinusoidal, with a frequency equal to the frequency difference between the LO and RF inputs – or $11.994 - 11.991$ GHz = 3 MHz with the setup used here. This has the benefit of being able to see the response of the electronics to all input phases in one measurement, rather than having to take multiple measurements varying the LO phase shifter between each one.

1.6.2 Results

Figures 1.8–1.13 show the mixer and diode outputs for all three sets of electronics at each of the input power levels sent from the signal generator. These will be referred back to and discussed in more detail in the remainder of this section. Some initial observations that are immediately clear from these figures are as follows. All mixer outputs show a sinusoidal oscillation with a frequency of 3 MHz, or 60 samples at the sampling frequency of 192 MHz, as expected. An oscillation with the same frequency is also visible on the diode outputs, with the largest amplitude for the 2nd set of electronics. This is the first hint of the non-ideal characteristics of the diodes. Finally, output of the mixer and diode increases with the input

power, as expected. At high input powers the outputs begin to saturate. This is apparent by observing the diode signals, on which the output is much flatter at the highest power levels, without the oscillation seen at low input powers. The characteristics of the mixers are discussed in Section 1.6.3 and the diodes in Section 1.6.4.

1.6.3 Mixer Performance

Sinusoidal Characteristics

Figure 1.14 shows fits to the response of all mixer outputs at an input power of 27 dBm, close to the typical input power from the beam signals when they are connected. Markers show the data points and the lines are sine fits to the data. The phase offset (displacement in peaks) between the output of each mixer holds no significance for the electronics performance. This is set only by the relative phase between the signal generator and the LO at the time the measurement was started. For normal operation with beam the LO phase shifters are changed to match the phasing of each set of electronics (Section 1.7).

The reconstruction of the phase from the mixer output depends on the mixer output being sinusoidal. In particular the maximum mixer output, or equivalently the gradient around zero mixer output (using the small angle approximation) is critical due to the dependence on the amplitude in Equation 1.12. Each set of electronics has a different output amplitude due to slight differences in the LO power for each set of electronics and between the individual components used. At an input power of 27 dBm Mixer 1 has a higher peak output of 510 mV, compared to 410 mV and 380 mV for Mixer 2 and Mixer 3 respectively.

Overall, the agreement between the actual mixer output and the sinusoidal fits at this input power is good. However, there is some distortion away from the ideal sine curve that is most visible around the maximum and minimum mixer output. Figure 1.15 shows the residuals between the mixer outputs and the sine fits across one half wavelength – from maximum output to minimum output. In the figure the plotted residual is the difference between the fit and the data expressed in terms of an equivalent phase offset, $\Delta\phi$, using:

$$\Delta\phi(t) = \arcsin\left(\frac{V_{MIXER}(t) - V_{FIT}(t)}{A}\right) \quad (1.32)$$

Where $V_{MIXER}(t)$ and $V_{FIT}(t)$ are the mixer voltage and fitted voltage at sample t respectively, and A is the fitted mixer amplitude. On the falling slope between the peaks there is only a slight oscillation about the ideal sinusoidal behaviour. The deviation from ideal is at the level of $0.25 \pm 0.03^\circ$ and $0.30 \pm 0.04^\circ$ for the first and third mixers, with a slightly larger effect of $0.45 \pm 0.04^\circ$ for the second mixer. This applies within $\pm 80^\circ$ of the zero crossing in the mixer output. Within $\pm 10^\circ$ of the maximum or minimum output the deviation from the sine fit rapidly increases, reaching several degrees for each mixer. For operation with the beam this means that the accuracy of the phase measurement cannot be guaranteed when the LO phase is set so that the mixer is giving close to its maximum or minimum output. This is also true for other reasons, as seen in Section ???. The PFF system can only correct small offsets at the level of around $\pm 5^\circ$ (Section 2.4.1), so the non-ideal response close to peak output is not an issue for the PFF performance.

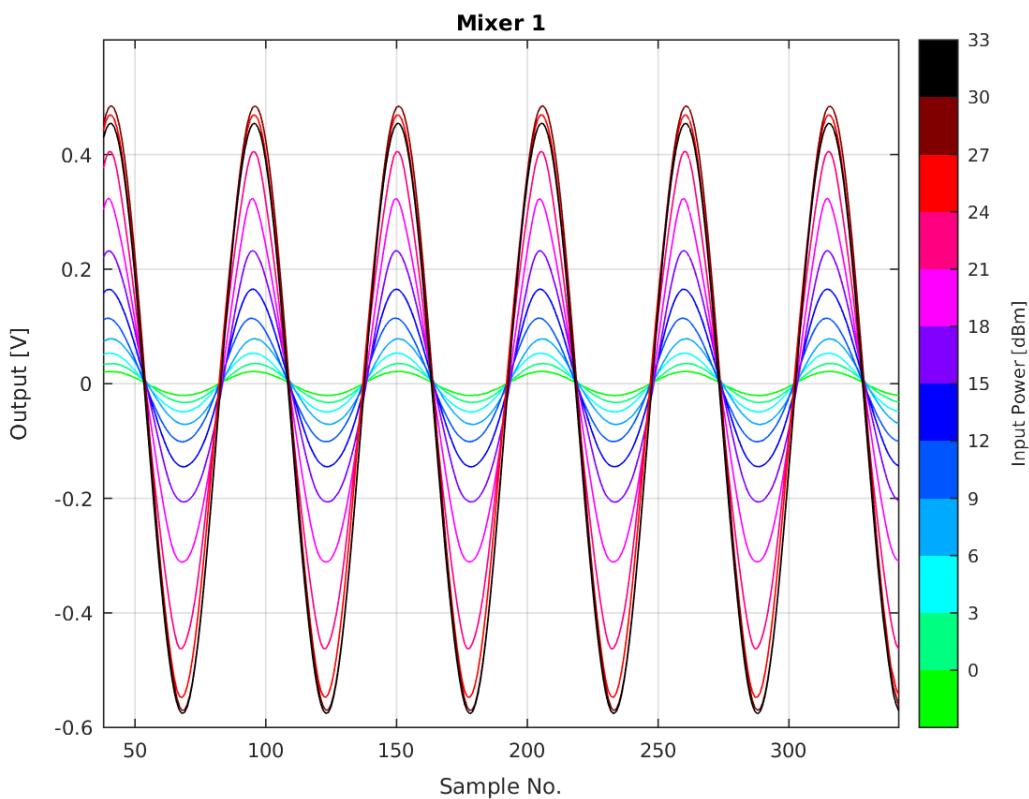


Figure 1.8: Response of Mixer 1 to signal generator input.

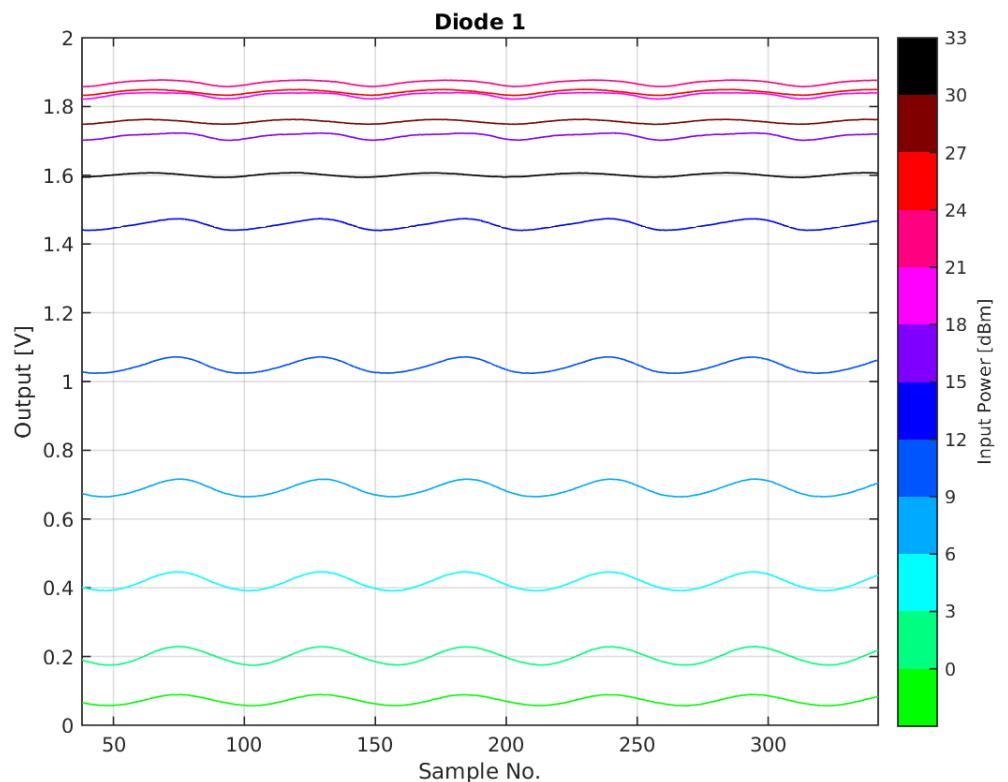


Figure 1.9: Response of Diode 1 to signal generator input.

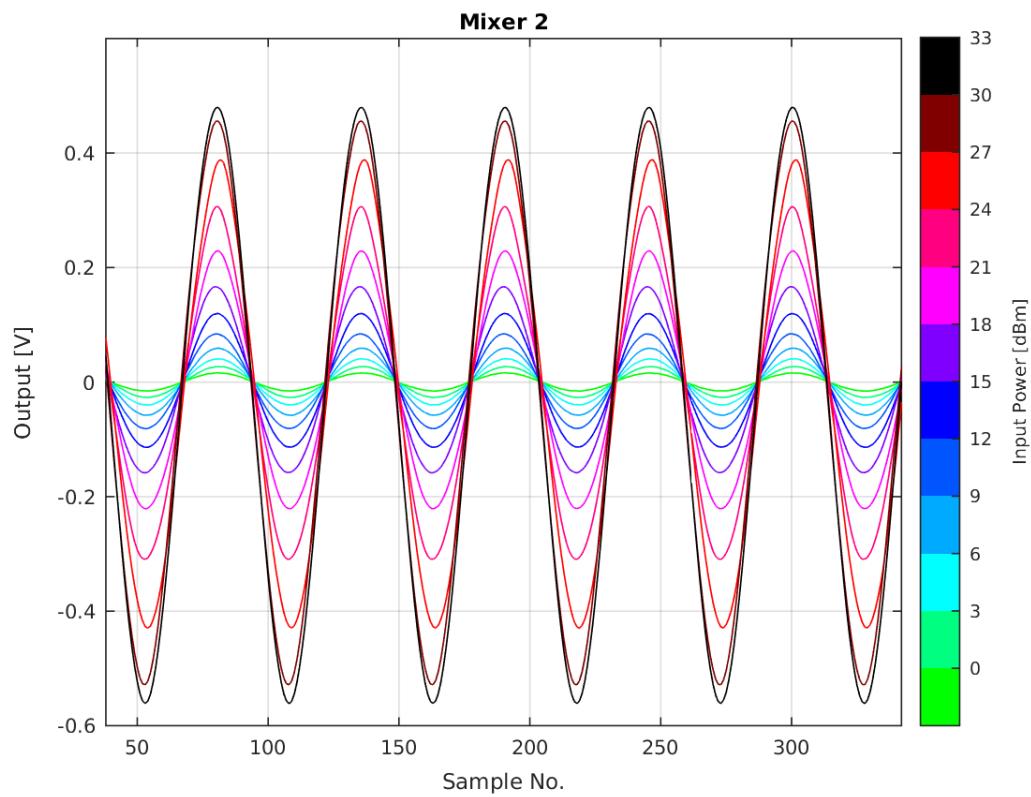


Figure 1.10: Response of Mixer 2 to signal generator input.

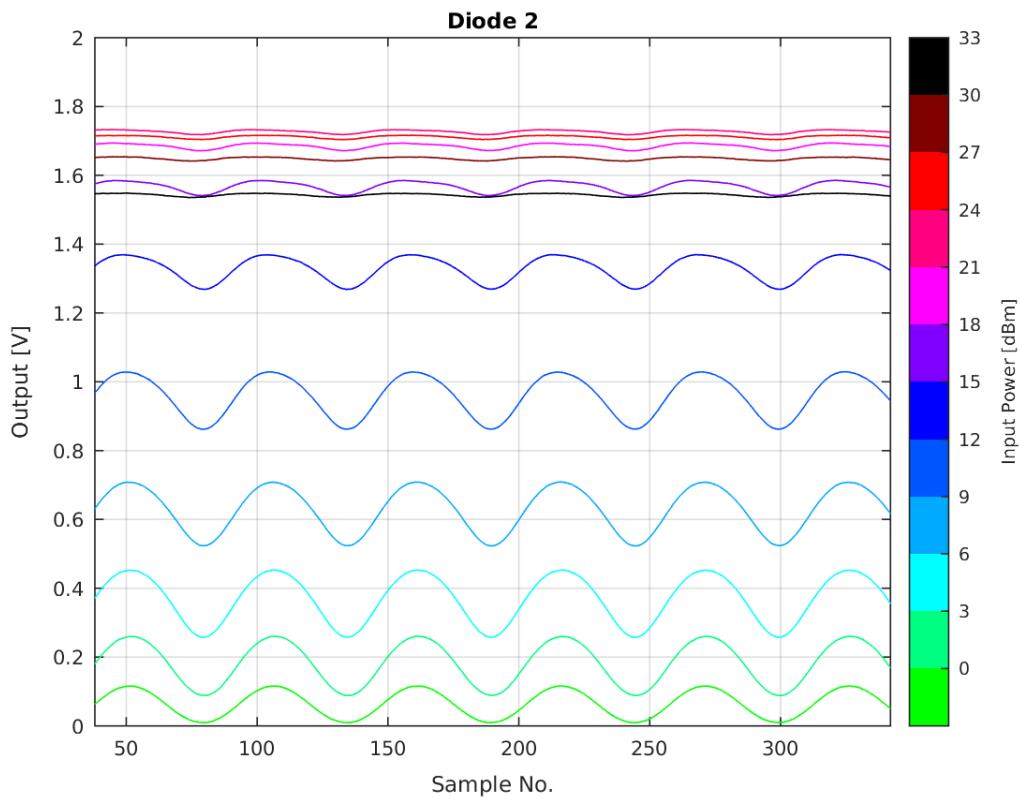


Figure 1.11: Response of Diode 2 to signal generator input.

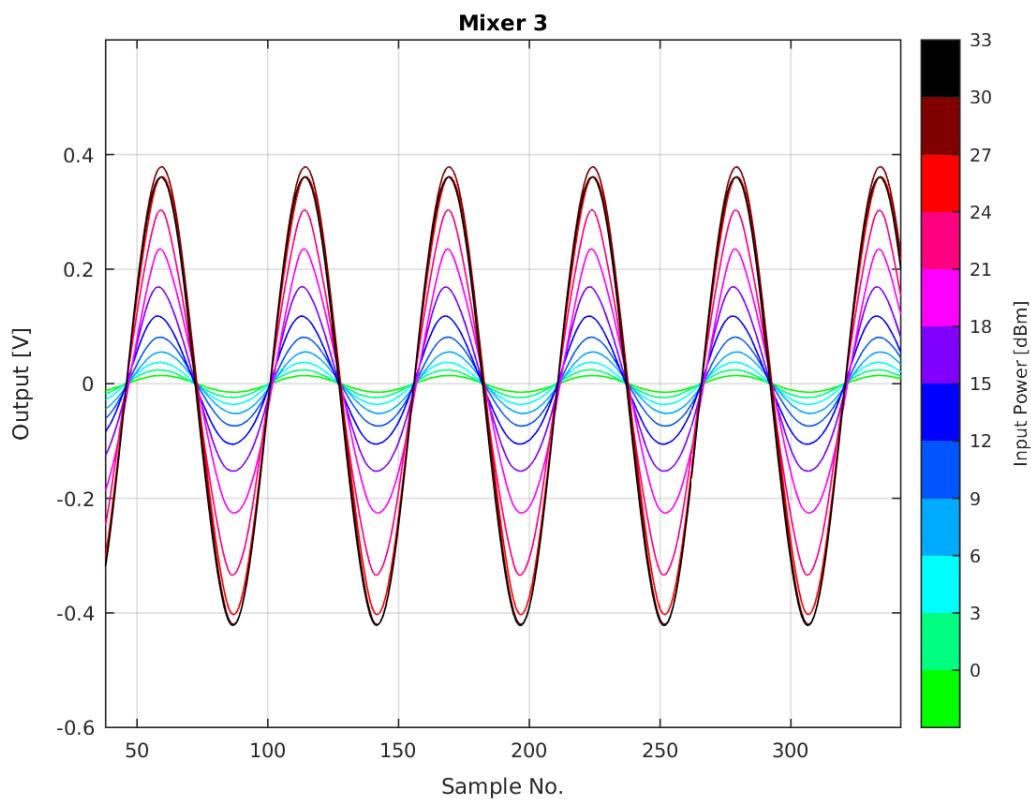


Figure 1.12: Response of Mixer 3 to signal generator input.

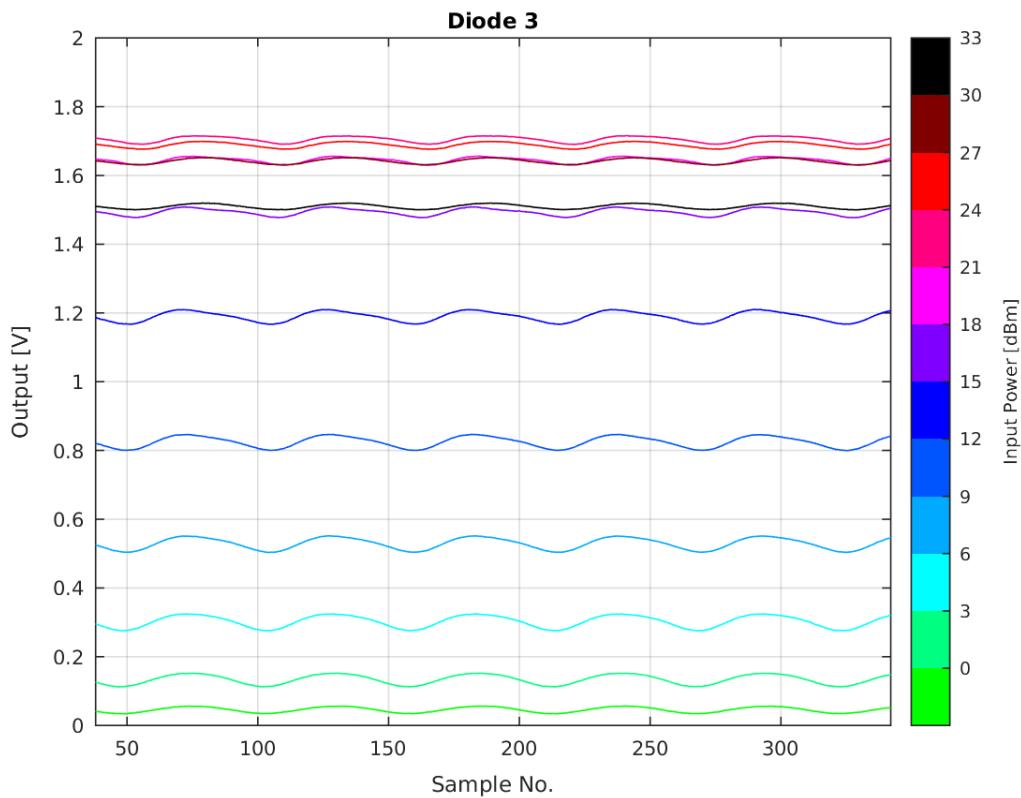


Figure 1.13: Response of Diode 3 to signal generator input.

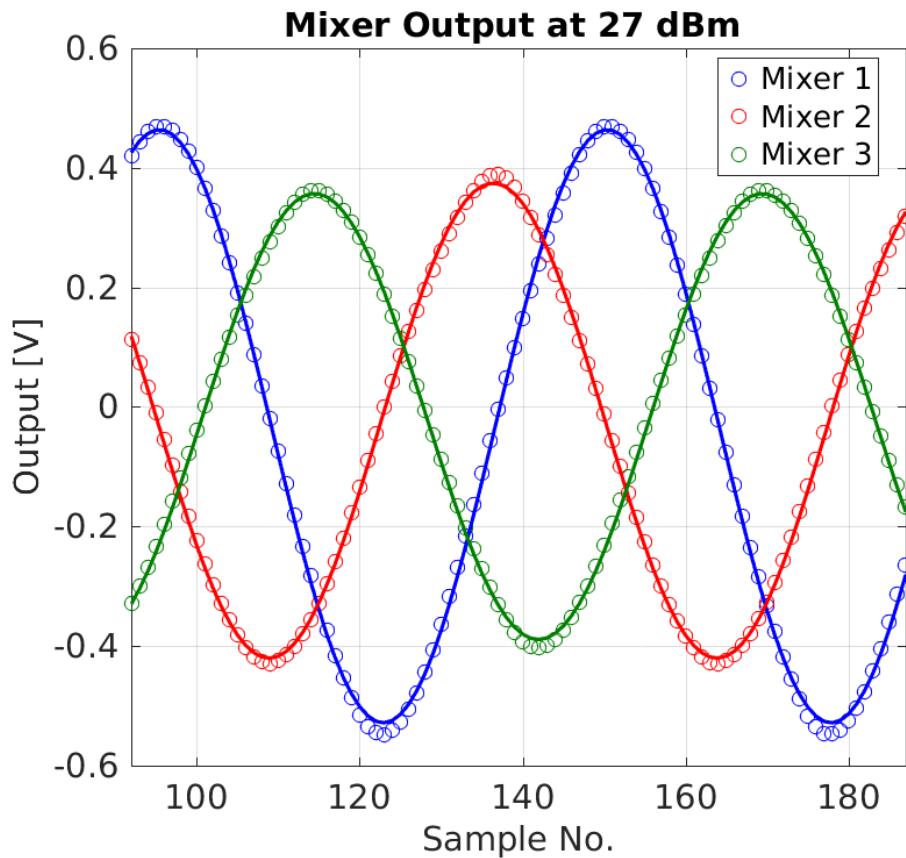


Figure 1.14: Sinusoidal fit to mixer responses at 27 dBm input power.

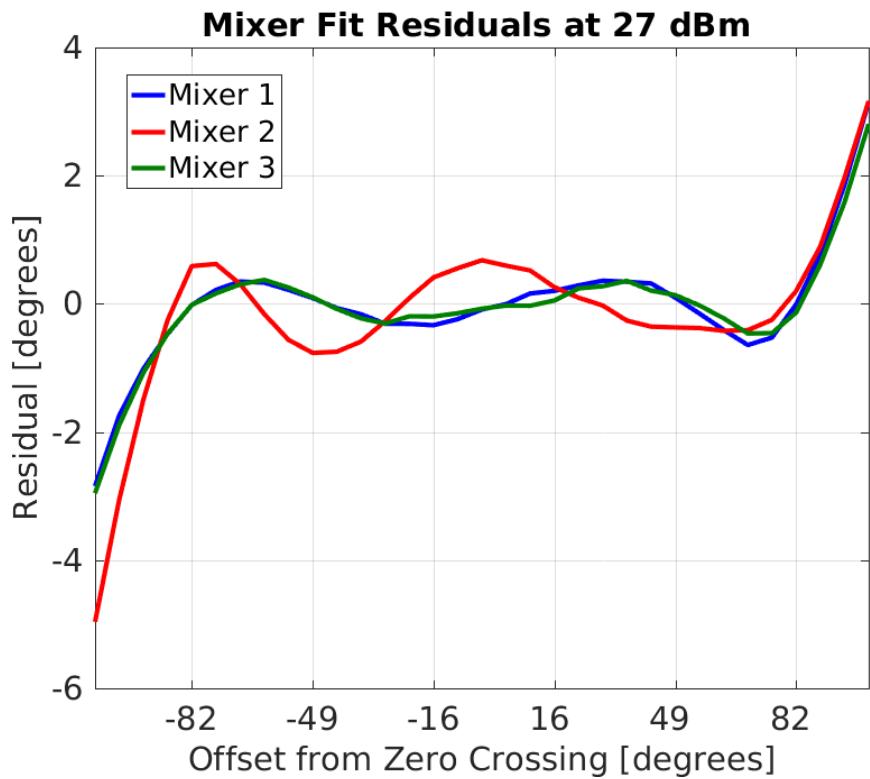


Figure 1.15: Residuals to sinusoidal fit at 27dBm.[TODO: sample numbers don't relate to previous plots]

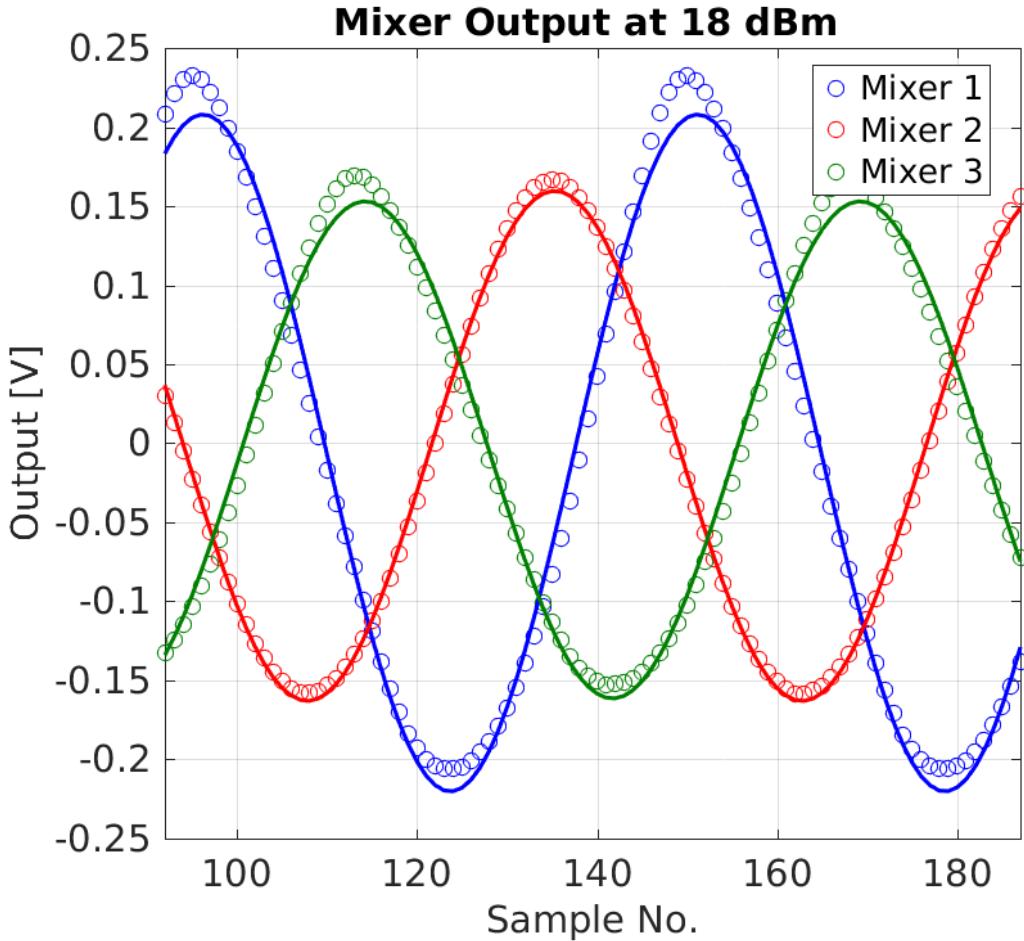


Figure 1.16: Sinusoidal fit to mixer responses at 18 dBm input power.

However, for input powers in the range from 15–21 dBm the non-ideal characteristics of the mixers are larger. One example of this is shown in Figure 1.16, at an input power of 18 dBm. If input powers in this range are used calibrations of the mixer response should normally be restricted to around the zero crossing so that the fitted amplitude gives the best approximation to the true behaviour for small phase offsets.

Dependence on Input Power

The mixer output is expected to linearly depend on the input voltage and the square of the input voltage. Both these dependencies must hold in order to use Equation 1.12 and obtain a phase measurement that does not depend on the input voltage to the electronics (therefore making the calculated phase insensitive to any possible variations in power along the pulse from the beam signal, for example). For these measurements the input voltage can be calculated using the known input power and $50\ \Omega$ impedance of the electronics.

Figure 1.17 shows the dependence of the mixer output amplitudes on the input voltage. As seen previously the first mixer gives a larger output than the other two mixers. The 2nd and 3rd mixers give a similar response up to an input voltage of 3.5 V (24 dBm). Dashed

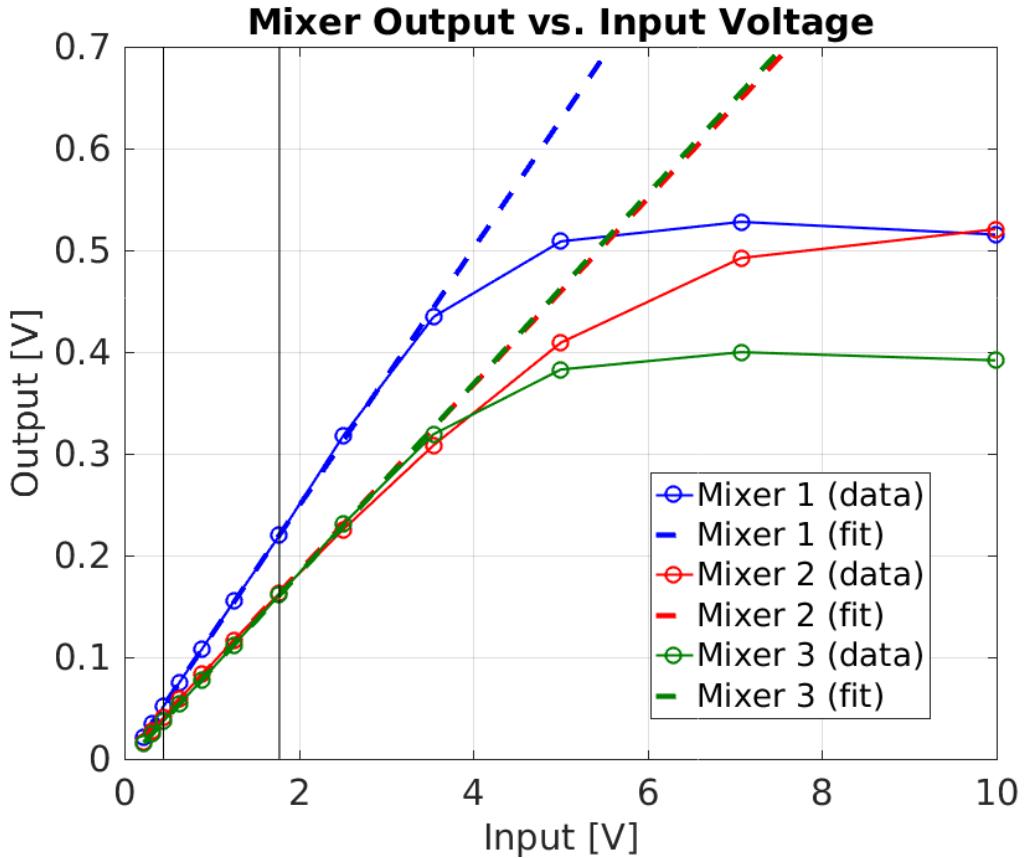


Figure 1.17: Linear fit to mixer output voltage vs. input voltage.

lines in the figure show a linear fit to the mixer output restricted to the range between 0.45 V and 1.75 V (6 dBm to 18 dBm) in each case, as marked by the vertical black lines. All three mixers give a linear response up to an input voltage of around 3 V (23 dBm), after which the effects of saturation begin to appear. By an input voltage of 5 V (27 dBm) the first and third mixers are almost fully saturated with almost no remaining power dependence in the output. The second mixer begins to enter saturation at the same voltage as the other two mixers but retains a strong power dependence up to a higher input voltage of 7 V (30 dBm).

Asymmetry in Output

One final interesting property of the mixers is that the output is not symmetric about zero, in other words the maximum output voltage is different to the absolute value of the minimum output voltage. This is perhaps most visible looking back to the Mixer 1 output at all power levels in Figure 1.8, where the maximum output is around +0.45 V but the minimum output is around -0.55 V.

Figure 1.18 shows how the mixer amplitude at maximum and minimum output varies with the input voltage. Mixer 1 asymmetry is largest for Mixer 1 and smallest for Mixer 3. The effect appears to increase in magnitude with the input voltage, with the ~ 100 mV difference mentioned previously for Mixer 1 at an input of 10 V, but differences of only

several mV at low input powers. For each mixer the amplitude at maximum output is larger for input voltages up to 2.5 V (21 dBm). Above 2.5 V input voltage this flips, with the minimum mixer amplitude being larger than the maximum amplitude.

For input voltages between 0.45 V and 1.25 V (6 dBm to 15 dBm) the mixer asymmetry has an approximate quadratic dependence on the input voltage, as shown in Figure 1.19. Outside this range there is no simple relationship that can explain the dependence of the asymmetry on the input voltage. One explanation for the asymmetry in the mixer outputs is cross-talk coming from the diode signals. Above 15 dBm the diodes enter saturation, as discussed in the next section, which may explain why the quadratic fit to the mixer asymmetry is only valid at power levels up to this value.

Taking the power dependent asymmetry into account the actual mixer response can be modified from Equation 1.9 to become:

$$\text{Mixer}(t) = m_1 A(t) \sin[\phi(t)] + m_2 A(t)^2 + m_3 A(t) + m_4 \quad (1.33)$$

Where $A(t)$ is the input voltage at time t , and m_1 , m_2 , m_3 , and m_4 are calibration constants.

1.6.4 Diode Performance

Dependence on Input Power

The dependence of the three diode outputs on the input power is shown in Figure 1.20, with the square root of the diode output plotted rather than the diode directly as this is the expected linear relationship. Immediately it is apparent that the diode signals saturate at much lower input voltages than the mixer signals. All three diodes are almost fully saturated at an input of 2 V (20 dBm), with the effects of saturation already beginning to appear above 1.25 V (15 dBm). Figure 1.21 shows a linear fit to the square root of the diode, using the range of input voltages between 0.45 V and 1.25 V (6–15 dBm). Even below saturation the response of $\text{sqrt}(\text{Diode})$ is not well approximated by a linear dependence as desired. However, in the range from 0.30 V to 1.25 V (3 dBm to 15 dBm) a quadratic fit to the diode output directly (not $\text{sqrt}(\text{Diode})$) does give a good approximation to the true dependence of the diodes on the input voltage. This is shown in Figure 1.22.

Cross-Talk

As seen previously in Figures 1.9, 1.11 and 1.13 the diode outputs show a sinusoidal oscillation. Like there is cross-talk from the diode on the mixer outputs, there is also cross-talk from the mixers on the diode outputs. Figure 1.23 shows a sinusoidal fit to the cross-talk on Diode 1 at an input power of 6 dBm. It has the same characteristics as the mixer output, including the slight distortion away from ideal sinusoidal behaviour around the peaks. However, as the diodes enter saturation the oscillation is initially distorted, and then has a much smaller amplitude when the diode output is fully saturated. One example of this is shown for the Diode 1 output at 18 dBm in Figure 1.24. The peaks around the maximum output are clearly non-sinusoidal in this case.

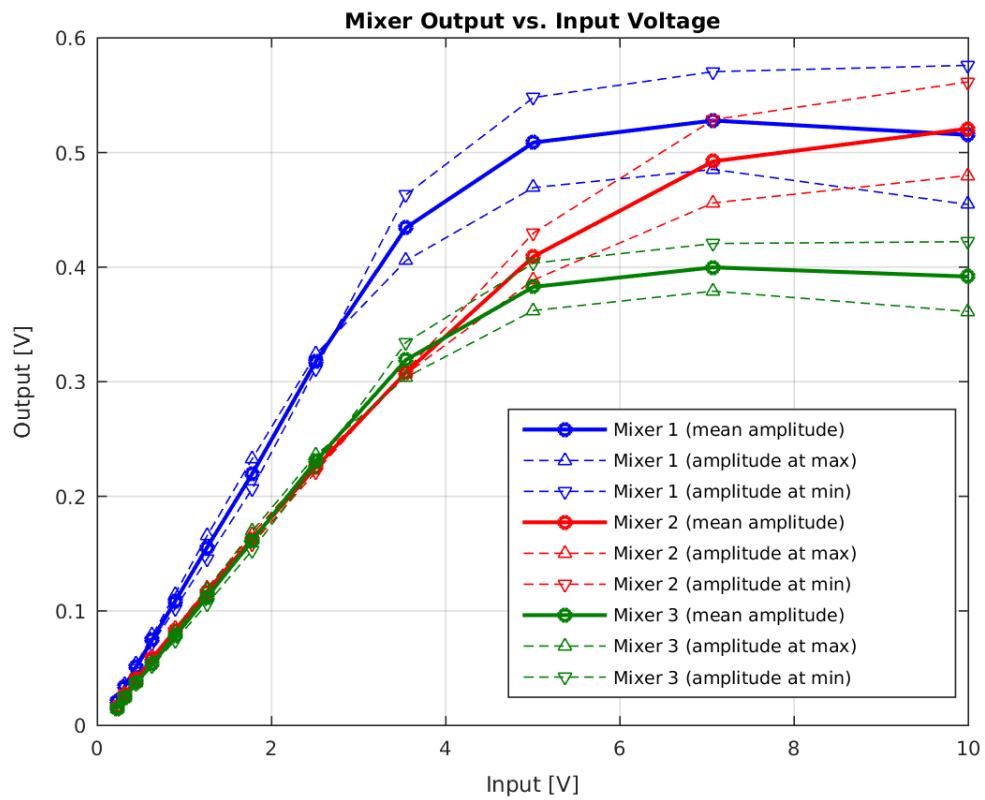


Figure 1.18: Mixer maximum and minimum output voltage vs. input voltage.

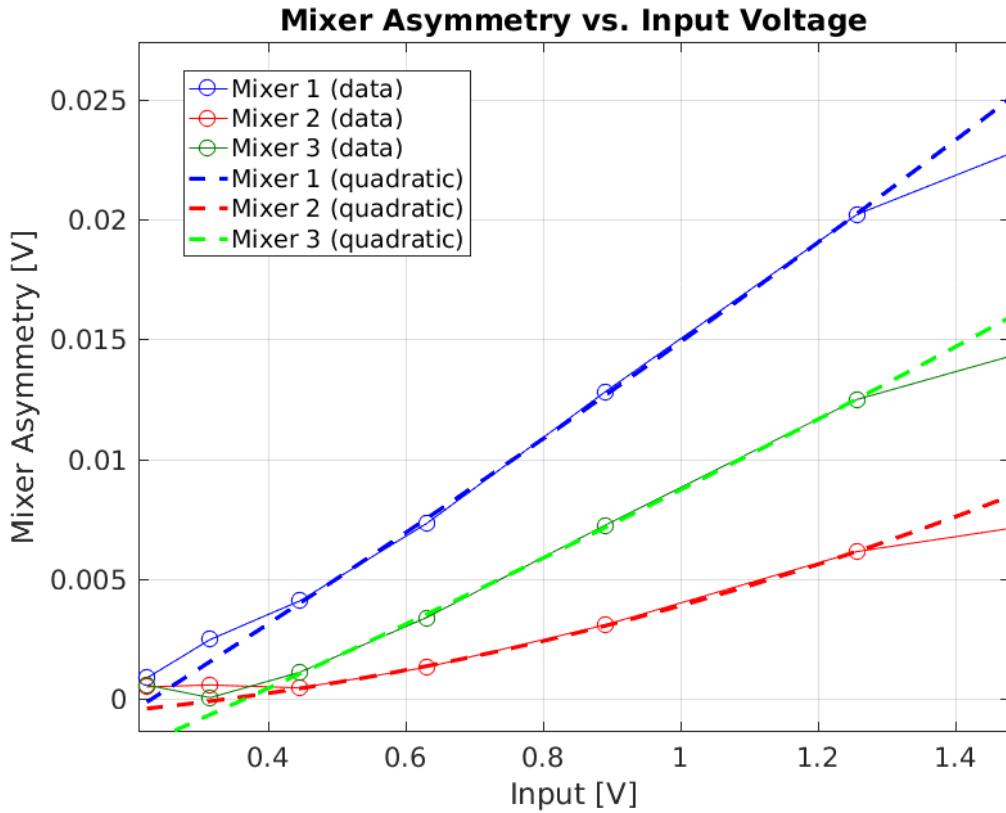


Figure 1.19: Relative amplitude vs. input power of cross-talk on the mixer from the diode.

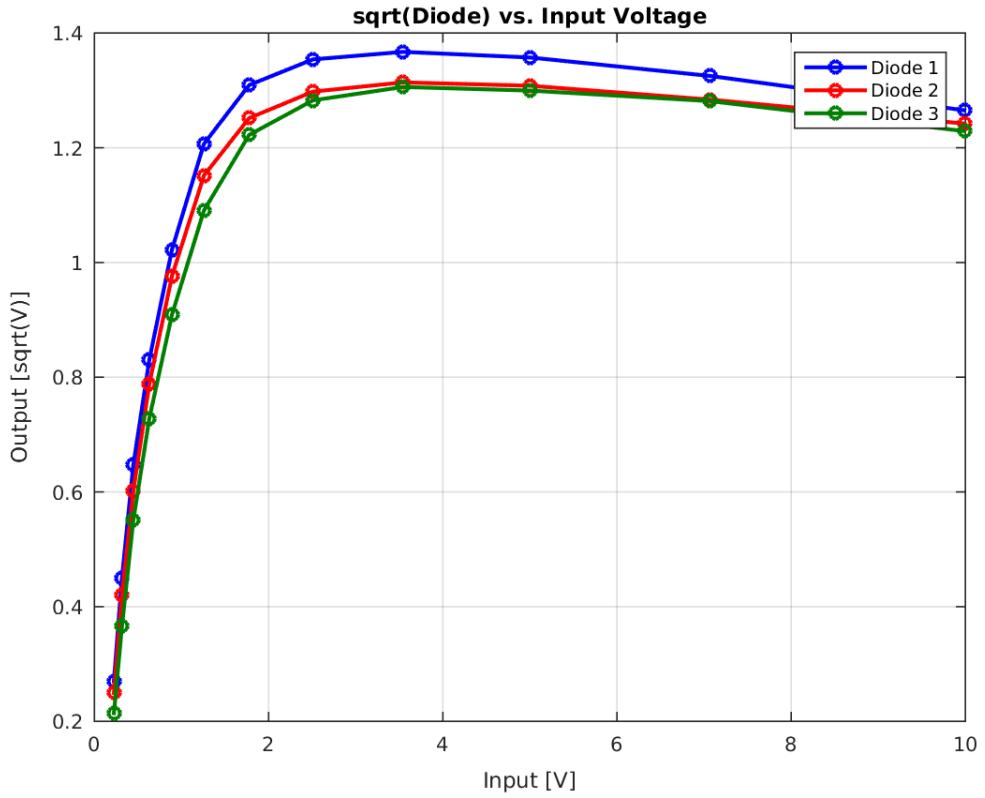


Figure 1.20: $\text{sqrt}(\text{Diode})$ vs. input voltage.

Figure 1.25 shows the dependence of the relative amplitude of the cross-talk on the input power. The relative amplitude of the cross-talk means the fitted amplitude of the sinusoidal oscillation on the diode divided by the mean diode output. Up until the diode outputs are fully saturated the relative amplitude of the cross-talk is around a factor two larger for the second diode. For example, at an input power of 12 dBm the relative cross-talk is at around the level of 30% for the second diode, or 15% for the first and third diode outputs. Up to input powers of 15 dBm the relative cross-talk is always above 10%.

Finally, Figure 1.26 compares the oscillation on the diode to the oscillation on the mixer. It can be seen that there is a phase shift between the two, which adds a further complication to the necessary phase reconstruction method. Taking in to account the actual characteristics of the diodes, including the cross-talk and quadratic dependence on the input power, the expected expression for the diode output from Equation 1.10 can be modified to:

$$\text{Diode}(t) = d_1 A(t)^2 + d_2 A + d_3 + d_4 A(t) \sin[\phi(t) + \delta] \quad (1.34)$$

Where d_1, d_2, d_3, d_4 and δ are calibration constants.

1.6.5 Consequences for Normal Operation

The results of the signal generator tests have several consequences for the setup of the electronics and phase reconstruction during normal operation with the beam induced signals

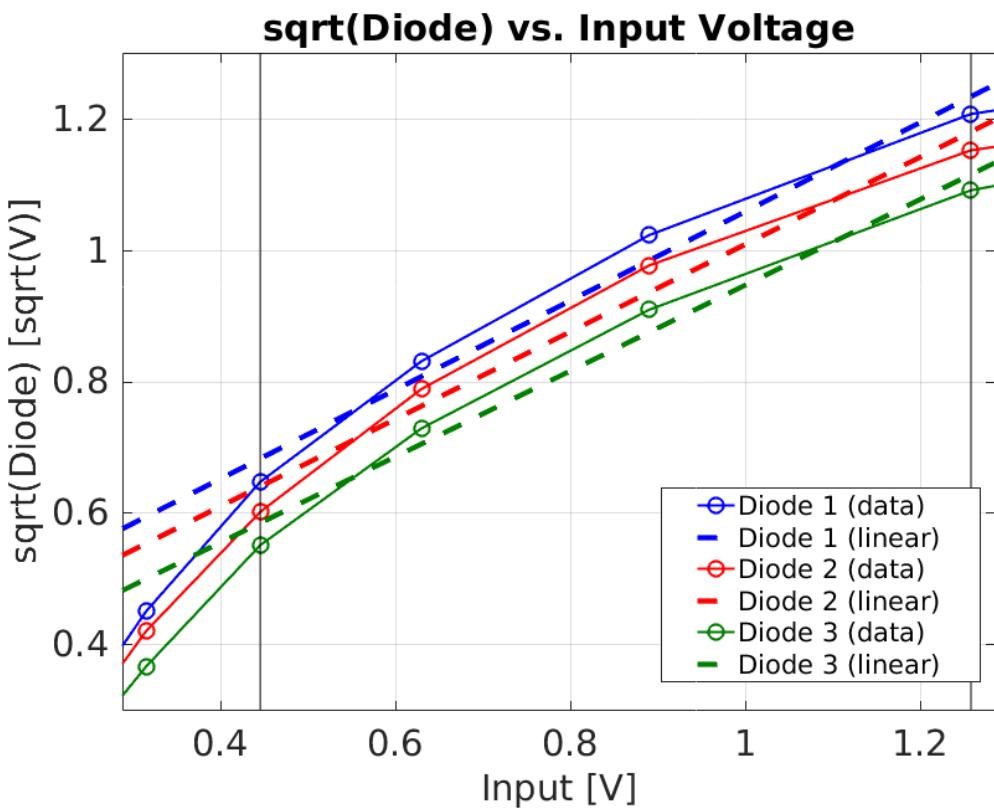
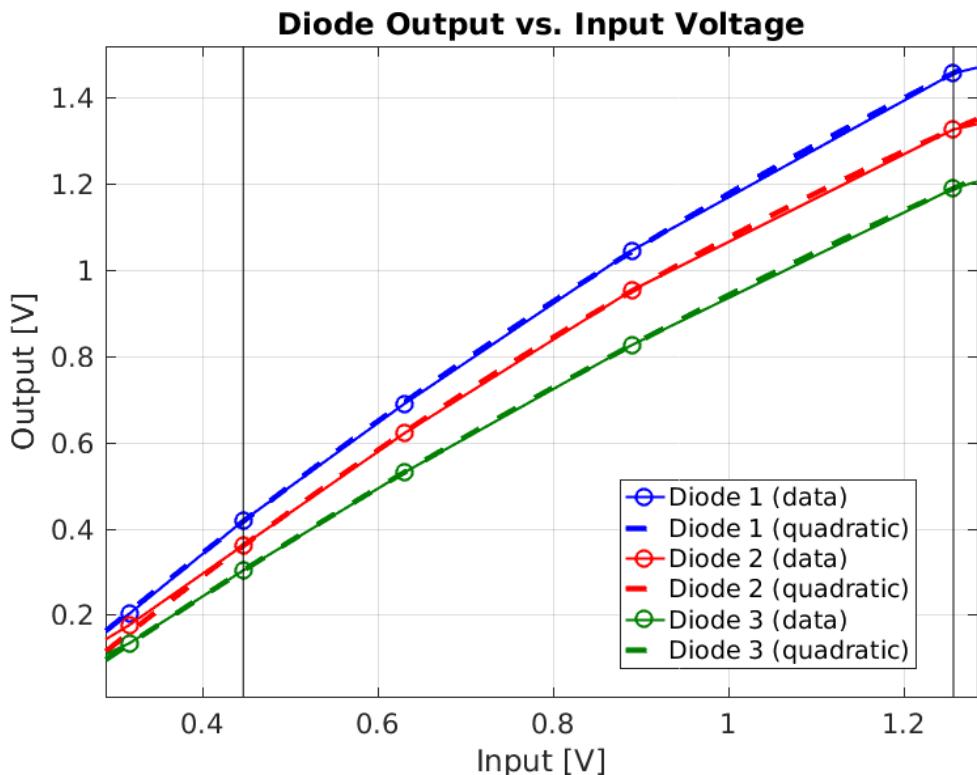
Figure 1.21: Linear fits to $\text{sqrt}(\text{Diode})$ vs. input voltage.

Figure 1.22: Quadratic fits to Diode vs. input voltage.

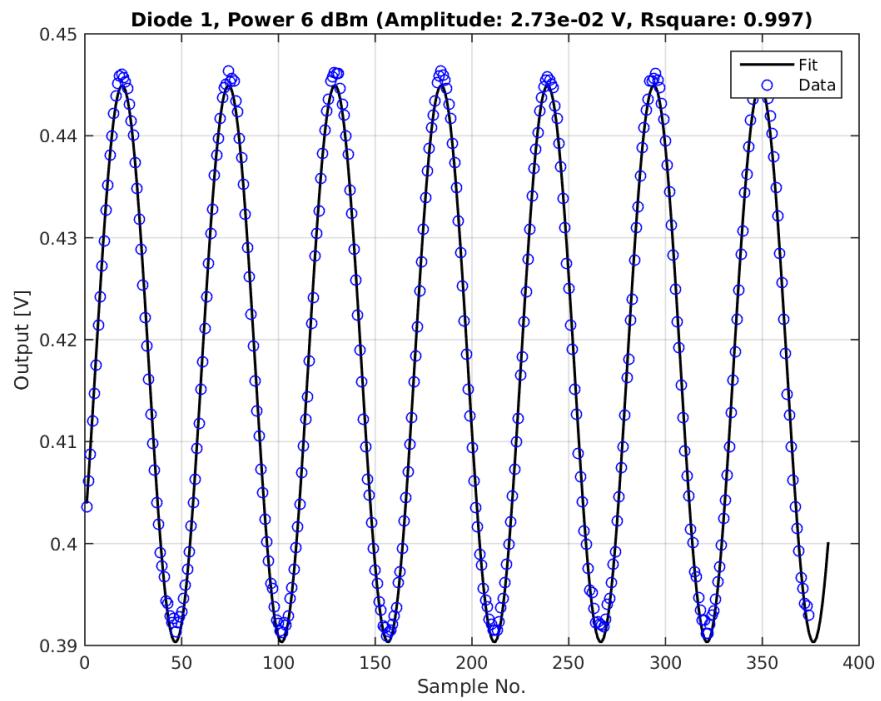


Figure 1.23: Sinusoidal fit to cross-talk on diode at 6 dBm input power.

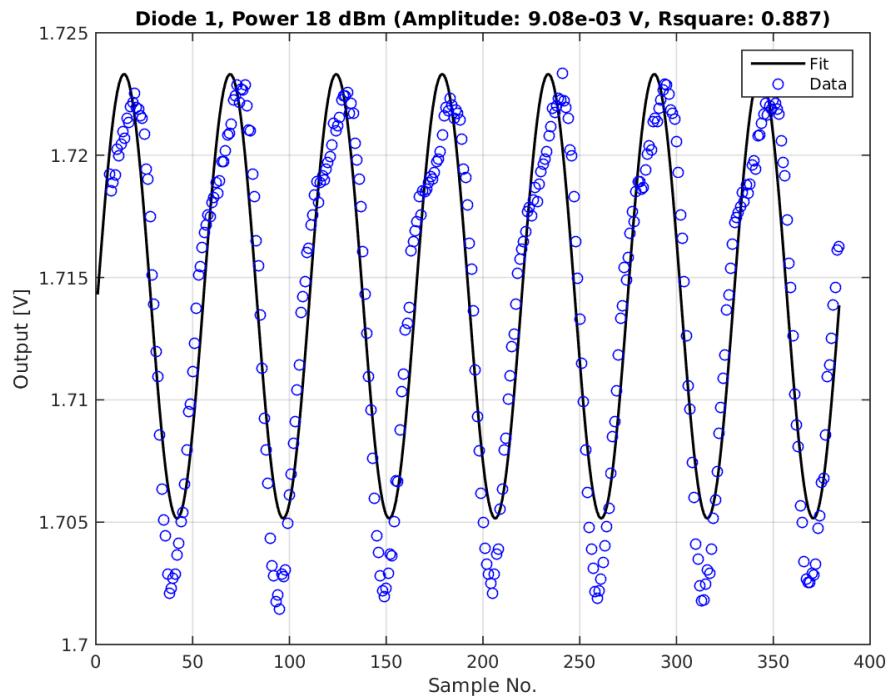


Figure 1.24: Sinusoidal fit to cross-talk on diode at 18 dBm input power.

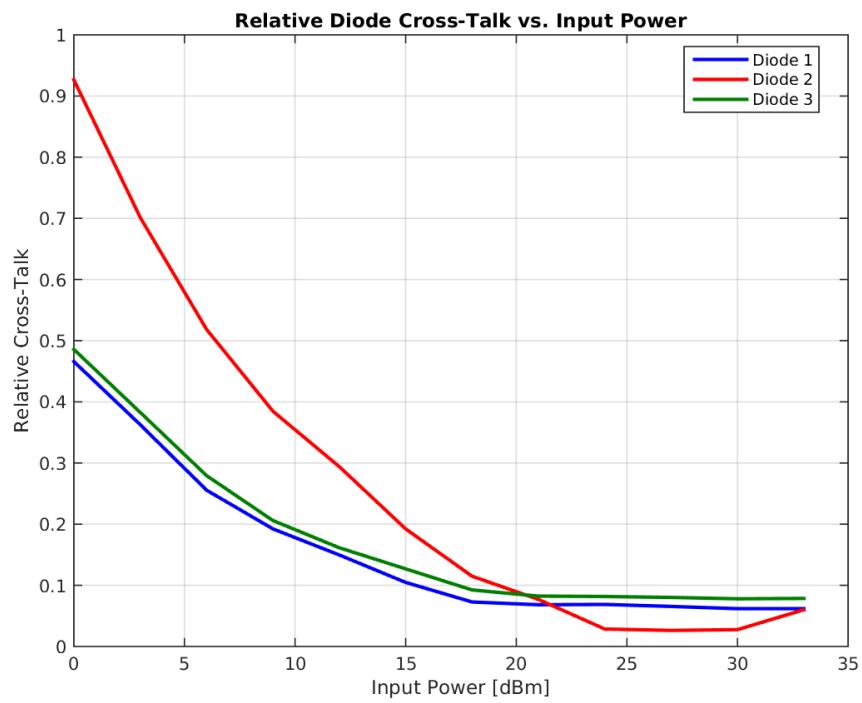


Figure 1.25: Dependence of the relative amplitude of cross-talk on the diode versus the input power.

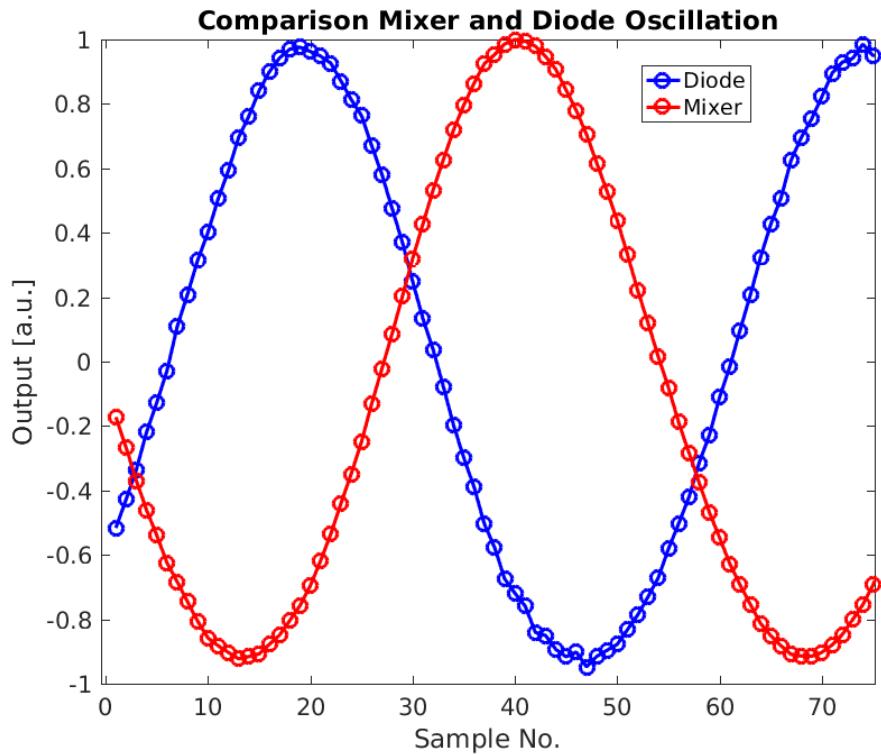


Figure 1.26: Comparison of the oscillation on the mixer and the diode, showing a relative phase offset between the two.

from the phase monitors. Firstly, in order to maximise the signal to noise ratio and yield the best possible resolution on the phase measurement the highest possible input power below saturation should normally be used. The degradation of the phase resolution with the input power is seen for beam based measurements in Section [REF]. However, the diodes begin to enter saturation much earlier than the mixers, at around 15 dBm rather than 23 dBm. This means that in order to be able to use the diode measurement as part of the phase reconstruction the input power would have to be limited to below 15 dBm, 8 dBm lower than would be ideal for the mixer performance. There is no way to use different input powers for the mixers and diodes without a complete redesign of the electronics.

Secondly, the modifications that the cross-talk on the mixer and diode make to Equations 1.33 and 1.34 above makes the needed calculation to reconstruct the phase much more complex than the ideal case using Mixer/sqrt(Diode) in Equation 1.12. In particular, the dependence of the diode output on $\sin(\phi + \delta)$ means there is no simple expression that can be derived to create an input power independent phase measurement. An iterative process would have to be used to estimate the phase instead, converging towards the true diode output without cross-talk after each iteration using the estimated phase value. This may be possible in offline data analysis but would be difficult to implement in the PFF algorithm whilst still meeting latency requirements.

Due to these reasons, and with no possibility to make modifications to the electronics, the decision was eventually taken to not include the diode measurement in the phase reconstruction process. For operation with the beam this means making the assumption that the output power from the phase monitors is constant along the pulse, and that the jitter in the output power is small. This is a good approximation, as seen later in Section [REF]. To reduce the sensitivity to any slow drifts in the output power due to changes in the beam conditions calibrations are taken at regular intervals between measurements.

With this treatment of the electronics outputs the phase is reconstructed as follows:

$$\text{Mixer}(t) = A \sin[\phi(t)] + d \quad (1.35)$$

$$\phi(t) = \arcsin\left(\frac{\text{Mixer}(t) - d}{A}\right) \quad (1.36)$$

Two calibration constants are needed – A and d . A is the fitted amplitude of the sinusoidal mixer output, and d is the asymmetry or offset between the maximum and minimum mixer output. This is a simplified form of Equation 1.33 given the assumption that the power is constant. In reality both A and d have a power dependence.

As any variations in input power are not removed by this method there is a benefit to operating the mixer in a region where the power dependence of the output is reduced. The best phase resolution achieved to date has been achieved with input powers to the electronics in the range between 24.5 dBm and 27 dBm (as stated in [REF]), where the mixers have actually begun to enter saturation, as a result. Operating in this range also has the benefit of reducing the deviation from ideal sinusoidal behaviour at lower input powers as seen in Section 1.6.3.

All the beam based measurements in the remainder of this chapter and the rest of the thesis use this phase reconstruction approach. Although the diodes are no longer directly

used as part of the phase measurement they are still useful for the purposes of the time alignment of signals and for monitoring whether there have been any large changes in input power. The PFF firmware on the FONT5a feedforward controller has also been changed to add the option to not include the diode in the correction calculation (Section ??). The nominal PFF setup, as used for the results presented in Chapter ??, now does not use diode normalisation.

1.7 Calibrations

The remainder of this chapter presents the performance of the complete phase monitor and electronics system for normal operation with the beam, replacing the signal generator with the RF output from the phase monitors.

The first step in using the the phase monitor measurements is to calibrate the mixer outputs. Calibrations of the phase monitor signals are typically taken on a daily basis during data taking periods, as well as additional calibrations when there have been any changes in beam conditions or to the setup of the electronics. These are needed to determine the calibration constants, amplitude and offset, to be able to determine the phase from the mixer output as previously discussed. This section presents typical calibration results for all three phase monitors and discusses aspects such as the stability of the calibration along the pulse and determining the optimal set point for the LO phase shifters.

For beam based measurements calibrations are performed using the LO phase shifters. By varying the LO phase shifter the phase between the LO and the beam signal is changed. During a calibration the phase shifters are moved through 360° at 12 GHz so that the response of the mixer to all phase offsets between the beam and LO can be determined. Normally calibrations are taken at 12 shifter settings across the full 360° range, with 10 pulses acquired at each setting and the whole scan taking approximately 10 minutes. These choices are a compromise between having enough points for a good quality fit whilst reducing the possibility of large drifts in beam phase during the scan which would degrade the fit results. All the calibrations presented use the electronics setup with the mechanical LO phase shifters in place (Section 1.8). The settings on these phase shifters approximately correspond to degrees at 4 GHz, thus a phase shifter change of 120 units corresponds to 360° at 12 GHz.

A calibration from both the SiS digitiser and FONT5a setup will be shown. During operation of the PFF system Mon 1 is usually connected to the FONT5a board as the correction input, whilst Mon 2 and Mon 3 are connected to the SiS digitisers where they can be acquired together with other signals at CTF3. The difference in measured output voltage between the two setups results from the use of an amplifier before the SiS digitisers to reduce noise in that setup (Section 1.4). Also, when using the FONT5a board the mixer outputs are attenuated by 1 dB to avoid saturating the FONT ADCs. The calibration constants from Mon 1 on the FONT5a board are needed for the PFF gain calculation in Section 2.1.1. All measurements of the upstream and downstream phase after this chapter use Mon 2 and Mon 3 on the SiS digitisers and their respective calibration constants.

Monitor	A (amplitude)	d (offset)
Mon 1	1167 ± 10 mV	86 ± 9 mV
Mon 2	1064 ± 6 mV	69 ± 7 mV
Mon 3	990 ± 12 mV	150 ± 10 mV

Table 1.5: Fit parameters from the calibration on the SiS digitisers for each monitor.

1.7.1 Calibration on SiS Digitisers

Figures 1.27–1.29 show the output of the mixer for each phase monitor along the pulse for all the phase shifter settings used during the LO scan. Away from the minimum and maximum output each mixer shows the expected phase sag along the beam pulse resulting from the RF pulse compression used at CTF3 [REF]. The shape of the phase sag as seen on the mixer changes sign depending on whether the LO phase places the mixer on the rising or falling slope of its sinusoidal output. Usually the mixers are operated on the falling slope where the measured phase sag is ‘u’-shaped, rather than ‘n’-shaped, as this is also the convention for other phase dependent signals at CTF3 [REF].

Near the minimum or maximum mixer amplitude the beam phase sag causes a much smaller variation in the mixer output voltage along the pulse. The phase resolution close to the peaks in the mixer output is therefore greatly reduced, as seen in Section ???. LO phase scans are used to not only calculate the calibration constants but also to determine the phase shifter settings that zero the mixer output, where the resolution is maximal. This process is documented in Section 1.7.4.

The noisier appearance of the output on Mon 3 is not an effect of the phase monitors or phase monitor electronics but is rather caused by real differences between the beam phase upstream (Mon 1, Mon 2) and downstream (Mon 3). Reducing the differences between the upstream and downstream phase is the focus of Chapter ??.

Figure 1.30 shows the result of fitting the mixer output versus the phase shifter setting at sample 605 along the pulse. The mixer response is sinusoidal as expected and as seen previously in the signal generator tests. In the signal generator tests there was some visible distortion away from the sine fit around the peaks at some input power levels (Section 1.6.3). There is no visible effect at the powers of the phase monitor signals (Section 1.1). Differences in the peak output of each monitor are expected due to differences in the input power from each phase monitor as well as differences between the sets of electronics. Small offsets between the data and the fit at some shifter settings are caused by drifts in the beam phase during the scan (particularly for Mon 3 where the beam is less stable), as well as human error in setting the shifter values.

The fitted values of the mixer amplitude, A , and offset, d , are found in Table 1.5. These values are used to calculate the beam phase as per Equation 1.36.

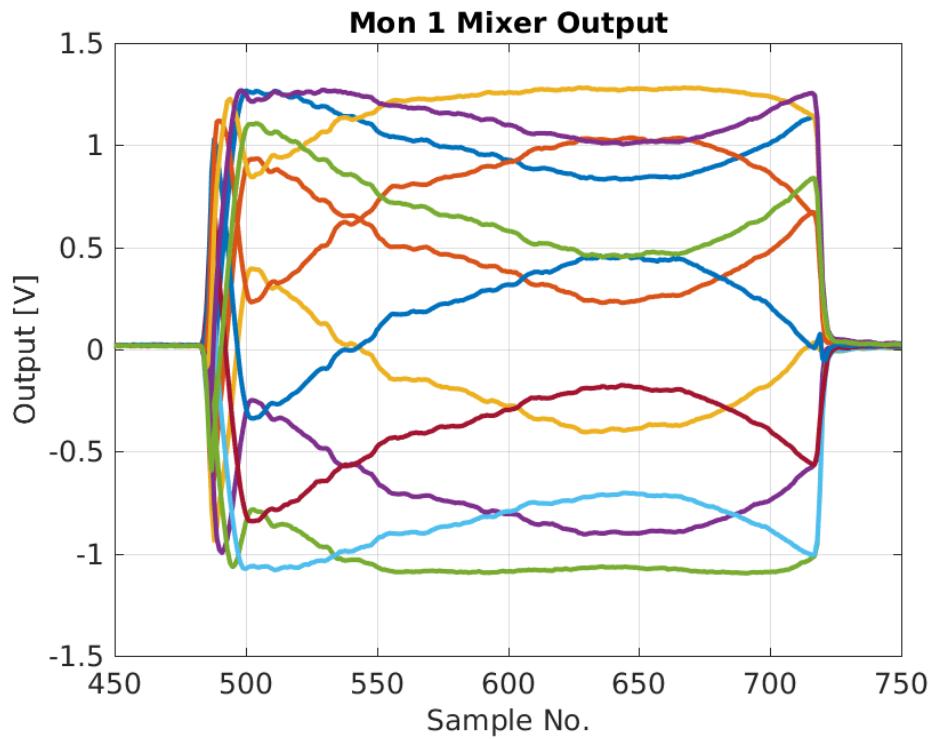


Figure 1.27: Mon 1 phase along the pulse for each LO phase shifter setting during the calibration.

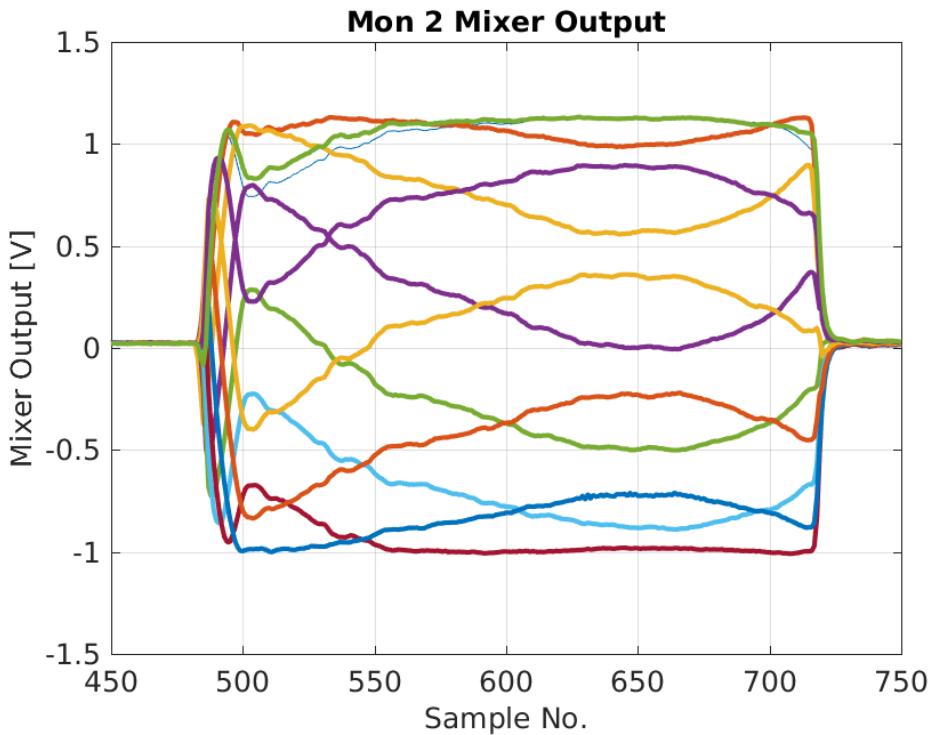


Figure 1.28: Mon 2 phase along the pulse for each LO phase shifter setting during the calibration.

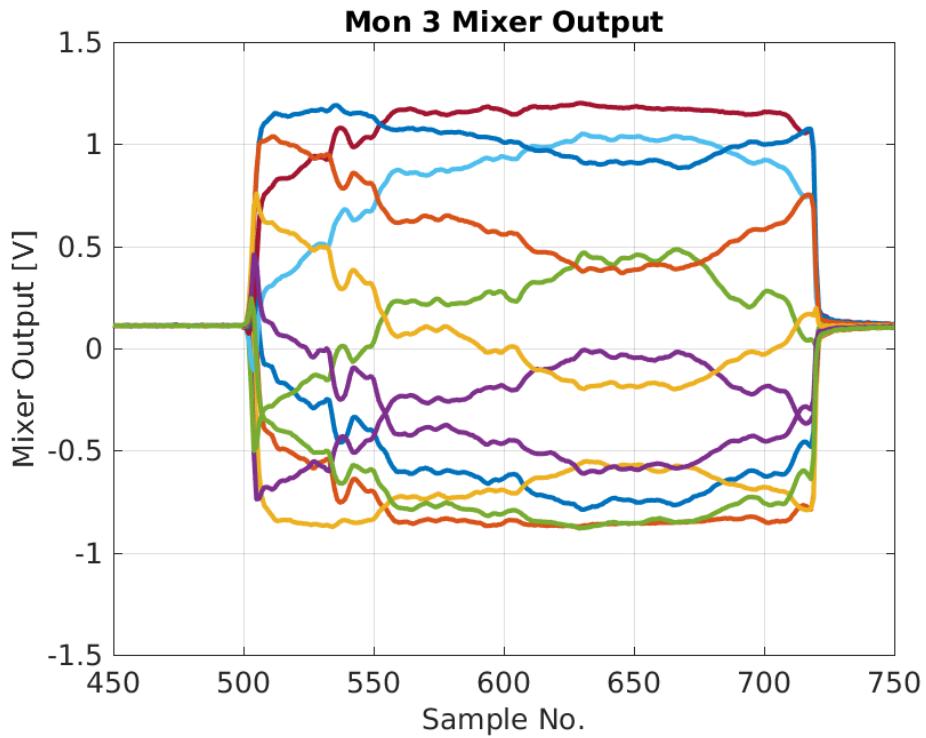


Figure 1.29: Mon 3 phase along the pulse for each LO phase shifter setting during the calibration.

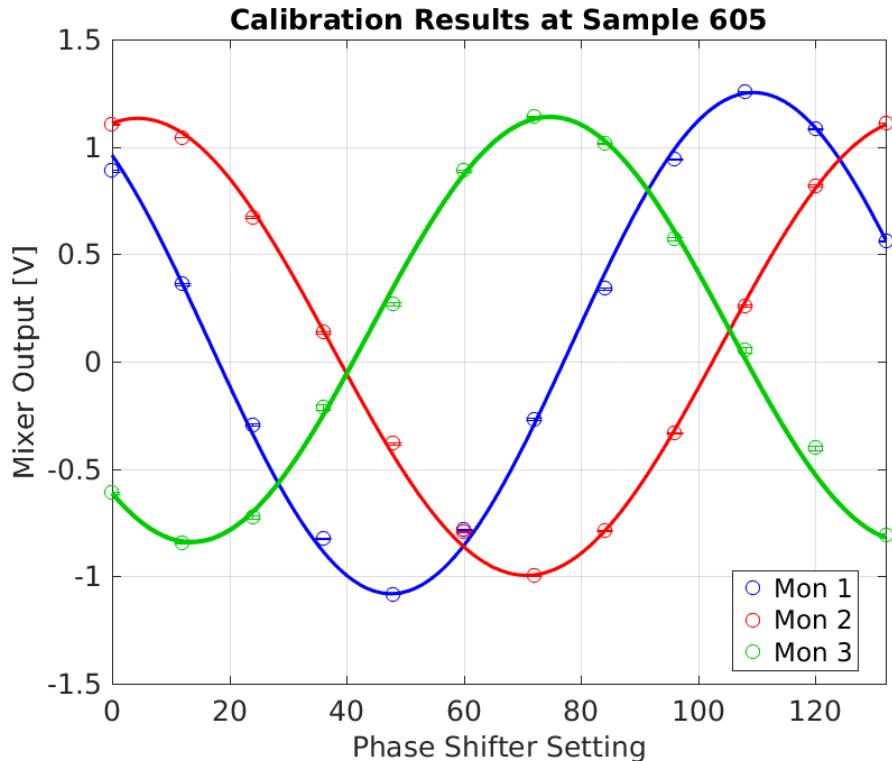


Figure 1.30: Fits to the mixer output vs. LO phase shifter setting at sample 605 on the SiS digitisers.

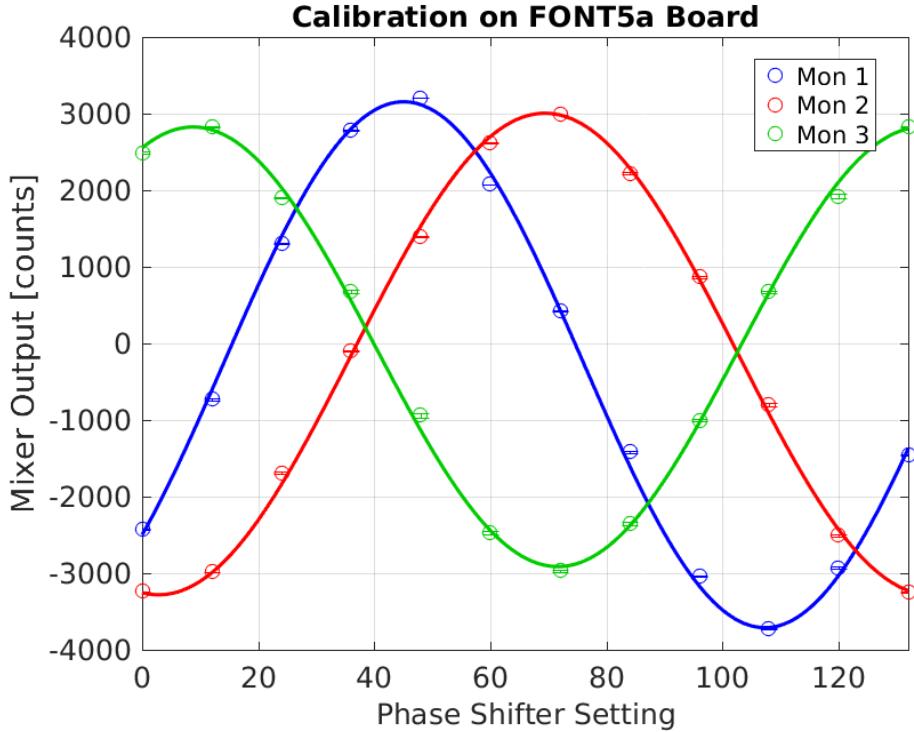


Figure 1.31: Results of a calibration performed on the FONT5a board.

1.7.2 Calibration on FONT5a Board

Figure 1.31 and Table 1.6 show the results of a calibration performed in exactly the same way but on the FONT5a board. The FONT5a board ADCs flip the sign of the input [REF], so a positive ADC output in counts corresponds to a negative input voltage and vice-versa. This explains why the apparent mixer output is on the rising slope at a phase shifter setting of zero on the FONT5a board in Figure 1.31, but on the falling slope on the SiS digitisers in Figure 1.30. For operation of the PFF system this difference must be taken in to account either by operating the mixer on the rising slope as seen on the FONT5a board (which in reality is the falling slope, as desired), or alternatively by using negative gain values for the correction output. The fitted values for d in Table 1.6 are also negative rather than positive as a result of this sign flip. Apart from these differences the overall shape of the mixer output follows the sinusoidal dependence as expected.

The FONT5a ADC outputs are 13-bit, or ± 4096 counts, with an input range of ± 500 mV (Section 2.1). The fitted Mon 1 output, with 1 dB attenuation added after the mixer, of between -3712 counts and +3156 counts therefore corresponds to an input voltage range of between +453 mV and -385 mV. Without the attenuator, which reduces the voltage by roughly 10%, the Mon 1 mixer would saturate the ADC at its peak output. As the contribution of digitiser noise is small on the FONT5a board (Section 1.4) a 1 dB attenuator is also added to the Mon 2 and Mon 3 outputs so that the overall setup for each monitor is the same in this measurement. However, during normal operation of the PFF system Mon 2 and Mon 3 are connected to the SiS digitisers, with their mixer outputs then being amplified rather than attenuated.

Monitor	A (amplitude)	d (offset)
Mon 1	3434 ± 41 counts	-278 ± 34 counts
Mon 2	3144 ± 16 counts	-138 ± 17 counts
Mon 3	2870 ± 43 counts	-44 ± 44 counts

Table 1.6: Fit parameters from the calibration for each monitor on the FONT5a board.

1.7.3 Multi-Sample Results

The calibration results on both the SiS digitisers and FONT5a board have been presented at one sample number around the middle of the pulse close to where the phase sag along the pulse is flattest. In this section the variation in the fitted calibration constants along the pulse is discussed. This is particularly important after taking the decision to not use the diodes, as the intended purpose of using the diodes was to normalise the mixer response to give an output independent of the input power. Without using the diodes any variations in input power along the pulse will also create differences in the calibration constants along the pulse.

The current implementation of the PFF algorithm on the FONT5a board uses the mixer multiplied by one gain value that is constant along the full pulse length to create the correction output (Section 2.1.1). It therefore cannot take in to account any variations in calibration constants along the pulse. Offline data analysis is usually performed in the same way so that the quoted resolutions are representative of the values that apply to the implementation of the PFF correction. The effect of taking in to account the variations in calibration parameters along the pulse seen here is shown in Section 1.9.2.

Figures 1.32 and 1.33 show the variation in the fitted calibration amplitude and offset across the full pulse length, using the same calibration on the SiS digitisers presented in Section 1.7.1. Differences in both the amplitude and offset along the pulse are visible. These are summarised in Table 1.7 in terms of the standard deviation of the fitted parameter values along the pulse.

The stability of the fitted amplitude along the pulse is similar for the upstream monitors (Mon 1 and Mon 2), with a jitter of around 8 mV in both cases. As the downstream beam is less stable than the upstream beam the variations in fitted amplitude along the pulse are larger for Mon 3, at the 15 mV level. In terms of a relative difference these values correspond to roughly a 0.7% variation in fitted amplitude for Mon 1 and Mon 2, or 1.5% for Mon 3. With further optimisation of the downstream beam, as documented in Chapter ??, it should be possible to achieve similar Mon 3 amplitude stability to that seen for Mon 1 and Mon 2.

Absolute stability in the fitted offset along the pulse is similar to that of the amplitude but therefore much larger as a relative difference at the level of several percent. The variation in fitted offset along the pulse is smallest for Mon 2 at around 3 mV. For both Mon 1 and Mon 3 the variation is around a factor two larger, at 6 mV.

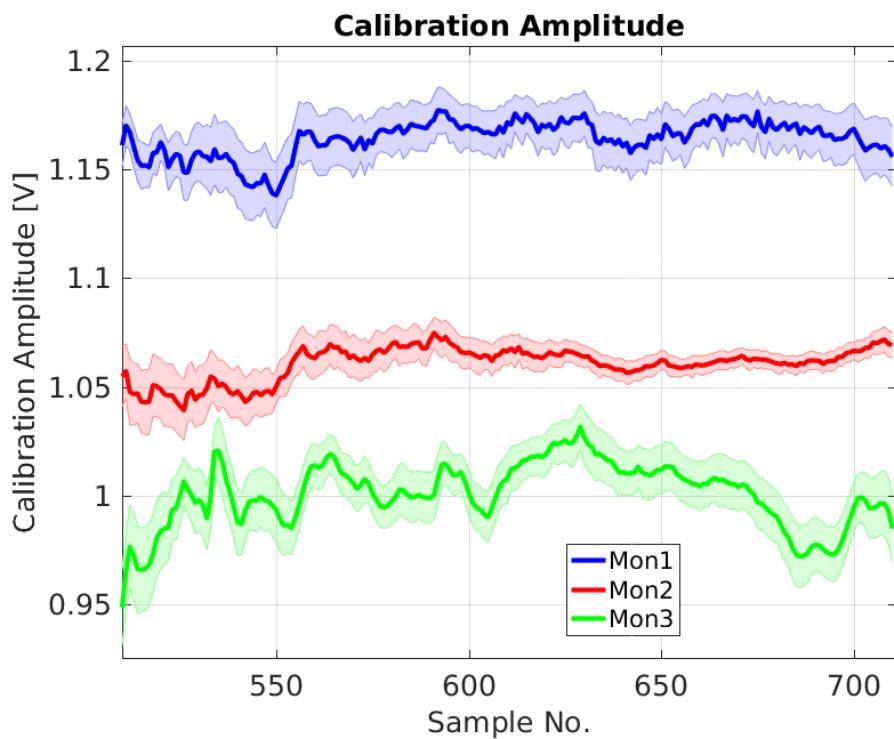


Figure 1.32: Variation in fitted amplitude along the pulse for each phase monitor.

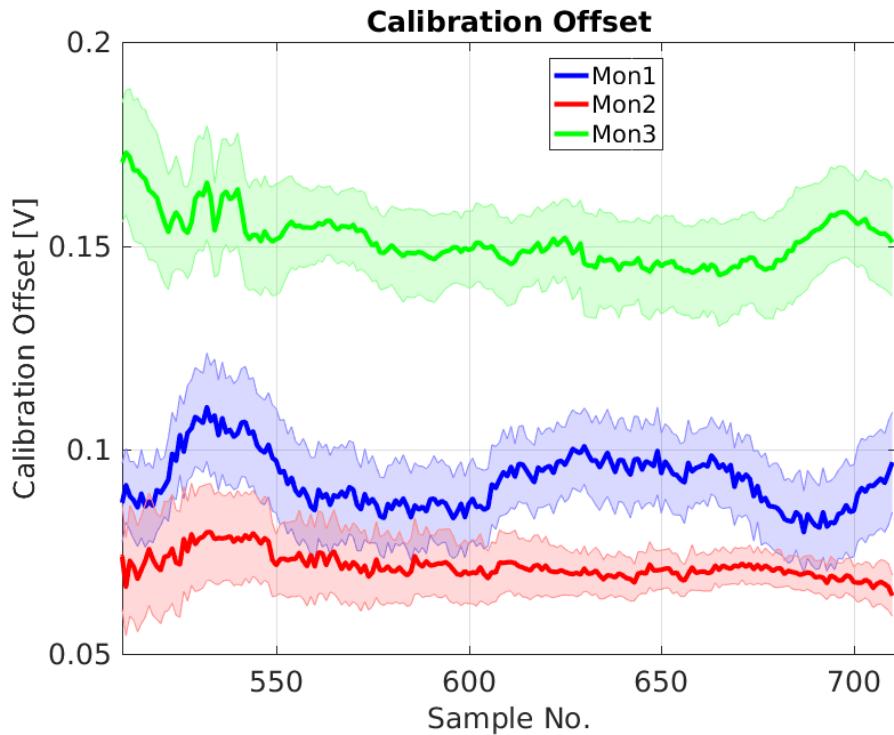


Figure 1.33: Variation in fitted offset along the pulse for each phase monitor

Monitor	A (amplitude)	d (offset)
Mon 1	8.3 ± 0.4 mV	6.7 ± 0.3 mV
Mon 2	7.7 ± 0.4 mV	3.0 ± 0.3 mV
Mon 3	14.7 ± 0.7 mV	6.1 ± 0.3 mV

Table 1.7: Standard deviation in calibration fit parameters along the pulse.

1.7.4 Zero Crossing

The full fit to the calibration result that is performed is:

$$\text{Mixer} = A \sin(bx + c) + d \quad (1.37)$$

Where x is the phase shifter setting. A and d are the calibration constants used to reconstruct the phase, with their values already quoted in Table ???. The remaining fit parameters b and c convert the phase shifter setting in to the phase offset between the LO and the beam. As the shifter readings are approximately in 4 GHz degrees, the expected value for b that converts the shifter value in to 12 GHz radians is $(12/4) * (\pi/180) \simeq 50$ mrad/unit.

To obtain the best resolution for the measurement the mixers should be operated where the dependence of the output voltage on the phase is maximal. This means maximising the partial derivative of the mixer output with respect to the phase shifter setting:

$$\frac{\partial \text{Mixer}}{\partial x} = Ab \cos(bx + c) \quad (1.38)$$

This is maximised when $bx + c = n\pi$, where n is any positive or negative integer. The optimal phase shifter settings therefore meet this criteria:

$$x = \frac{n\pi - c}{b} \quad (1.39)$$

Where the mixer output is $\text{Mixer} = A \sin(n\pi) + d = d$. In the case where there is no offset between the minimum and maximum mixer output ($d = 0$) the optimal point to operate the mixers is at zero output. Because of this the optimal shifter setting will be referred to as the zero crossing. In reality the small asymmetry in the mixer output means the optimal shifter setting is where mixer output is d . The effect of operating the mixers away from the zero crossing on the resolution is shown in Section ??.

In addition, as previously mentioned the convention is to operate the mixers on the falling slope where the partial derivative above is negative. The set shifter values are obtained using the smallest positive integer n that leads to this criteria being met. Table 1.8 shows an example of values for the fit parameters b and c and the calculated phase shifter settings to be on the zero crossing for each monitor. These values are taken from the same calibration and sample number presented in Section 1.7.1 (on the SiS digitisers). The reader may be interested to compare where the shifter settings fall along the mixer output traces during the calibration in Figure ??.

Due to the large phase sag along the beam pulse it is clearly not possible to be at the zero crossing of the mixer for the full pulse length. For the PFF system the region of interest

Monitor	b	c	Zero Crossing
Mon 1	50.8 ± 0.5 mrad/unit	2.29 ± 0.04 rad	16.7 ± 0.9 units
Mon 2	47.4 ± 0.5 mrad/unit	1.36 ± 0.04 rad	37.5 ± 0.8 units
Mon 3	51.3 ± 0.6 mrad/unit	4.02 ± 0.04 rad	105.5 ± 1.5 units

Table 1.8: Phase shifter setting to obtain the zero crossing for each mixer output and the fit parameters needed to calculate them.

is the central portion of the pulse where the phase sag is flattest. The shifters are therefore set to zero the mixer output in this region, giving best resolution in the central part of the pulse but degraded resolution near the start and end of the pulse. In addition to this, slow drifts in the beam phase, particularly downstream, mean that the shifters must routinely be changed to stay at the zero crossing. With the current setup using mechanical phase shifters this must be done by hand, with no possibility to implement an automatic feedback on the shifter settings, for example.

1.8 Phase Shifter Noise

In the first tests with all three phase monitors in their final positions at CTF3 the measured phase resolution was far in excess of the 0.14° derived to be necessary to achieve a 0.2° corrected downstream phase jitter in Section 1.3. Figure 1.34 shows a typical example of the measured resolution along the pulse at that time with an achieved resolution of around 0.4° , three times larger than required. The lowest downstream phase jitter that could be achieved with the PFF system in these conditions is above 0.55° , only about 30% smaller than the initial upstream phase jitter at CTF3 (Chapter ??). To be able to achieve a large reduction in downstream phase jitter with the PFF prototype the source of the poor phase monitor resolution had to be identified and removed.

The first hint towards identifying the cause of the degraded resolution came by comparing the measured phase jitter from Mon 1 and Mon 2, with one example shown in Figure 1.35. Note that for all the results in this section it is not the absolute value of the phase jitter (which depends mostly on the beam conditions in that dataset) that is important but rather the difference between the measured phase jitter in each monitor. The measured phase jitter along the pulse in Mon 2 with a mean of $1.38 \pm 0.01^\circ$ is 1.7 times larger than the $0.83 \pm 0.01^\circ$ phase jitter in Mon 1. Jitter values from this and all the other datasets presented in this section are shown in Table 1.9. As Mon 1 and Mon 2 are neighbouring each other in the beam line the actual phase jitter in the two should be close to identical.

The overall phase monitor and electronics setup can be roughly split in to three systems – the RF signal from the beam (dependent on the phase monitors themselves and the hybrids), the LO reference signal and the mixers. An issue with any one of these systems could explain the larger phase jitter measured from Mon 2 (usually connected to Mixer 2 and LO 2) compared to the phase jitter from Mon 1 (usually connected to Mixer 1 and LO 1). To determine whether the issue was with the RF signal of one of the monitors measurements

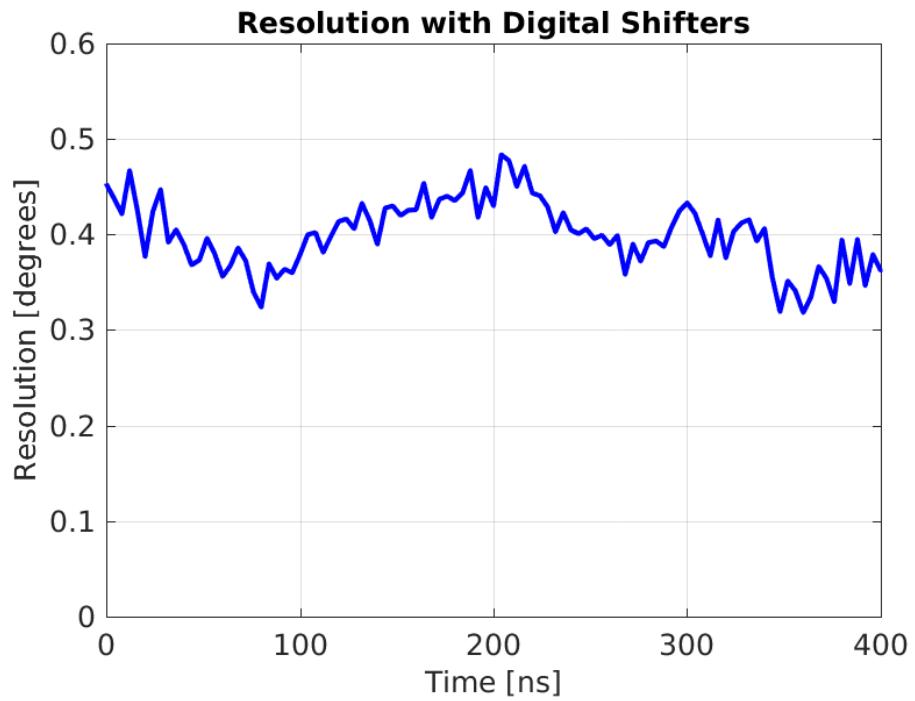


Figure 1.34: Phase monitor resolution using initial setup with digital phase shifters in place.

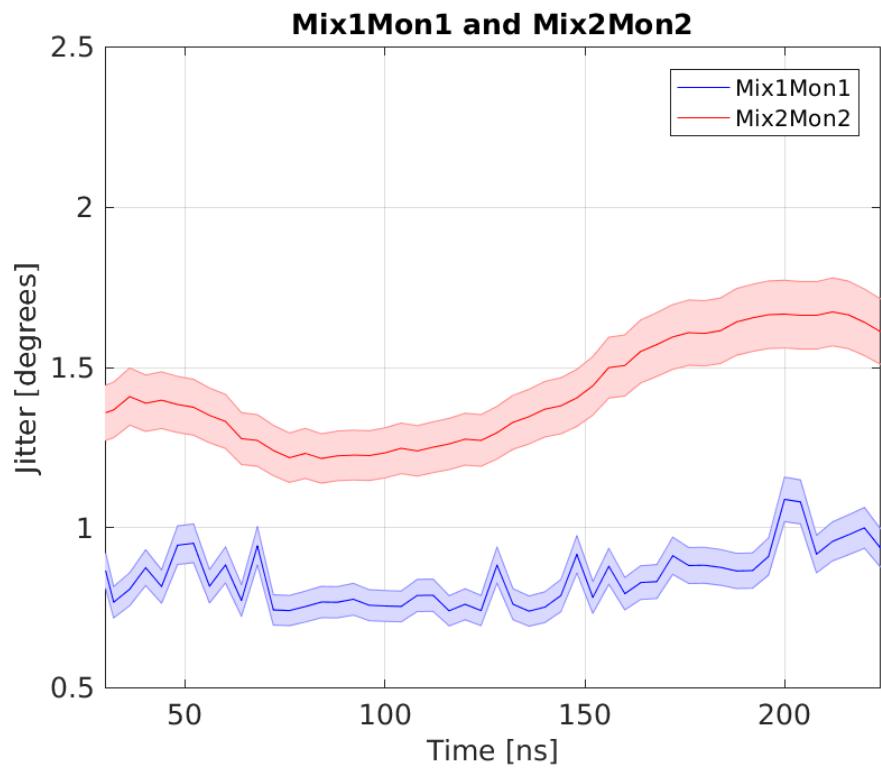


Figure 1.35: Phase jitter along the pulse with the nominal electronics setup – Mon 1 connected to the first mixer, and Mon 2 connected to the second mixer.

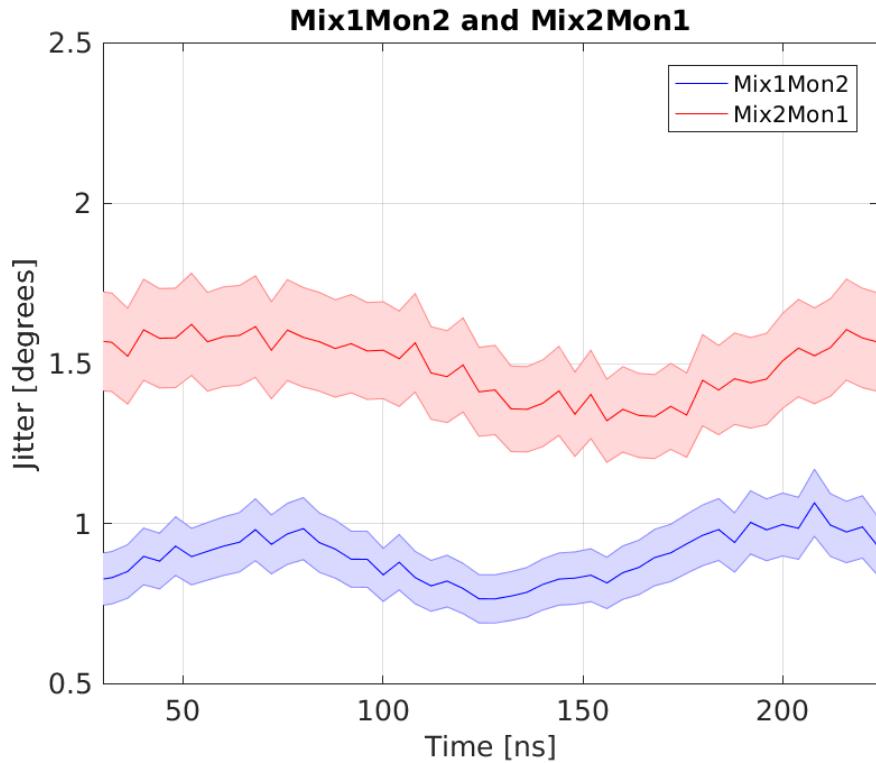


Figure 1.36: Phase jitter along pulse with Mon 2 connected to the first mixer and Mon 1 connected to the second mixer.

were taken with Mon 1 and Mon 2 swapped between the three mixers.

Figure 1.36 shows the measured phase jitter along the pulse when Mon 2 is moved on to Mixer 1 (and LO 1) and with Mon 1 moved on to Mixer 2 (and LO 2). The colours in all the plots in this section correspond to the mixer that measurement is from – blue for Mixer 1, red for Mixer 2 and green for Mixer 3. With the phase monitors swapped the higher measured phase jitter stays with Mixer 2 with the same ratio of 1.7, in this case $1.48 \pm 0.01^\circ$ on Mixer 2 (connected to Mon 1) and $0.89 \pm 0.01^\circ$ on Mixer 1 (connected to Mon 2). This rules out that the difference in phase jitter is coming from the phase monitors themselves, and suggests the problem is with either Mixer 2 or the reference signal LO 2 for that mixer. The same exercise can then be repeated with Mon 2 moved on to Mixer 3 (and LO 3) and the nominal setup used for Mon 1. Mixer 3 gives similar results to Mixer 2, with 1.7 times larger phase jitter than Mixer 1. This is seen in Figure 1.37. The remaining task is therefore to identify whether the additional source of noise is from Mixer 2 or LO 2, and from Mixer 3 or LO 3.

This was determined by swapping the LO reference signals between the mixers. Figure 1.38 shows the measured phase jitter with LO 2 connected to Mixer 1, and LO 1 connected to Mixer 2. In this case the lower measured phase jitter stays with LO 1, with $1.10 \pm 0.01^\circ$ jitter on Mixer 2 (with LO 1) and $1.68 \pm 0.01^\circ$ on Mixer 1 (with LO 2). In Figure 1.39 the same is seen with LO 3 connected to Mixer 1, and LO 1 connected to Mixer 3, with the lower phase jitter coming from Mixer 3 (LO 1) in this case. In Table 1.9 it can also be seen that the lowest phase jitter in every dataset always comes from the phase monitor

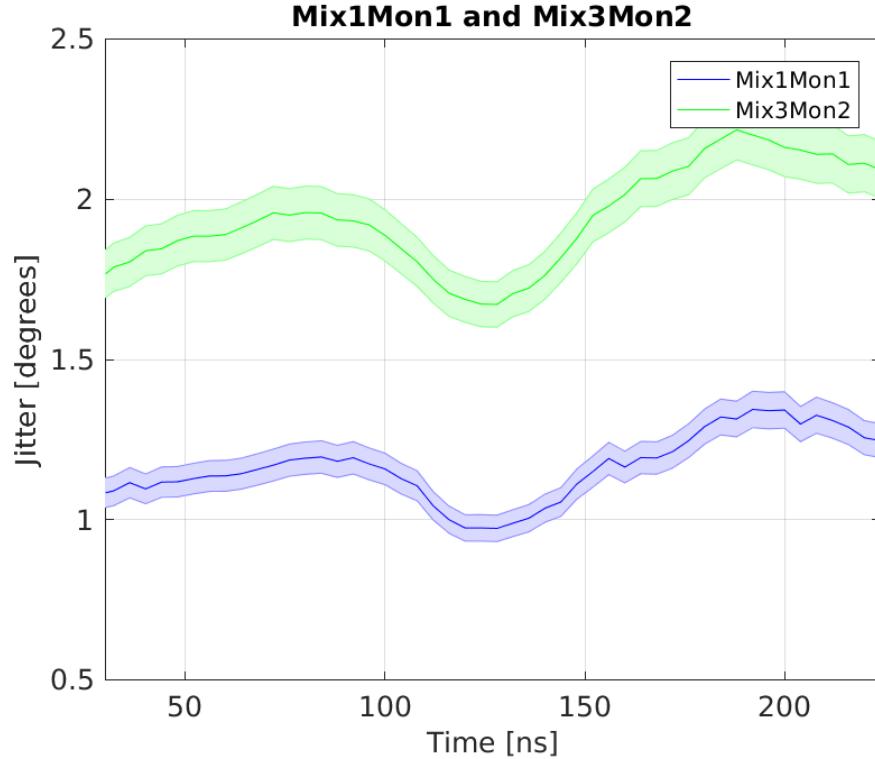


Figure 1.37: Phase jitter along pulse with Mon 1 connected to the first mixer and Mon 2 connected to the third mixer.

for which LO 1 was used.

In this way an issue with LO 2 and LO 3 was identified. The generation of the LO reference signals (Section 1.2) consists of a 3 GHz source that is common to all three signals, plus separate phase shifters, frequency multipliers (to create the 12 GHz reference) and amplifiers for each LO signal. The digital phase shifters were thought to be the most likely culprit to be adding noise in to the system, and preliminary tests replacing one of the digital phase shifters with a mechanical alternative provided an immediate gain in resolution. Finally, all three digital shifters were replaced with mechanical phase shifters (the specifications of the shifters were introduced in Section 1.2). With this setup the measured phase jitter for Mon 1 and Mon 2 is the same irrespective of which mixer or LO the signal is connected to, as shown in Figure 1.40. The final achieved resolution is presented in the next section.

1.9 Resolution Measurements

This section presents resolution measurements with the mechanical phase shifters in place and the same overall electronics setup that was used to achieve the best PFF results in Chapter ???. All measurements use the upstream phase monitors Mon 1 and Mon 2. There is no way to directly verify the resolution of the downstream phase monitor Mon 3, but it should match that of Mon 1 and Mon 2 and the achieved phase stabilisation in Chapter ?? suggests it does have below 0.2° resolution.

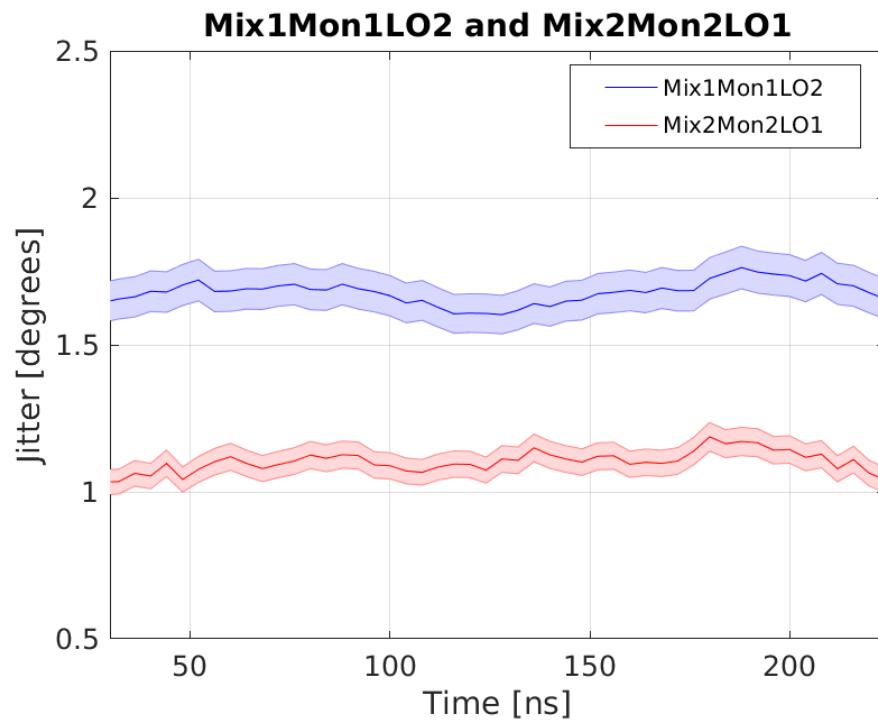


Figure 1.38: Phase jitter along pulse with the LO swapped between the first mixer and the second mixer.

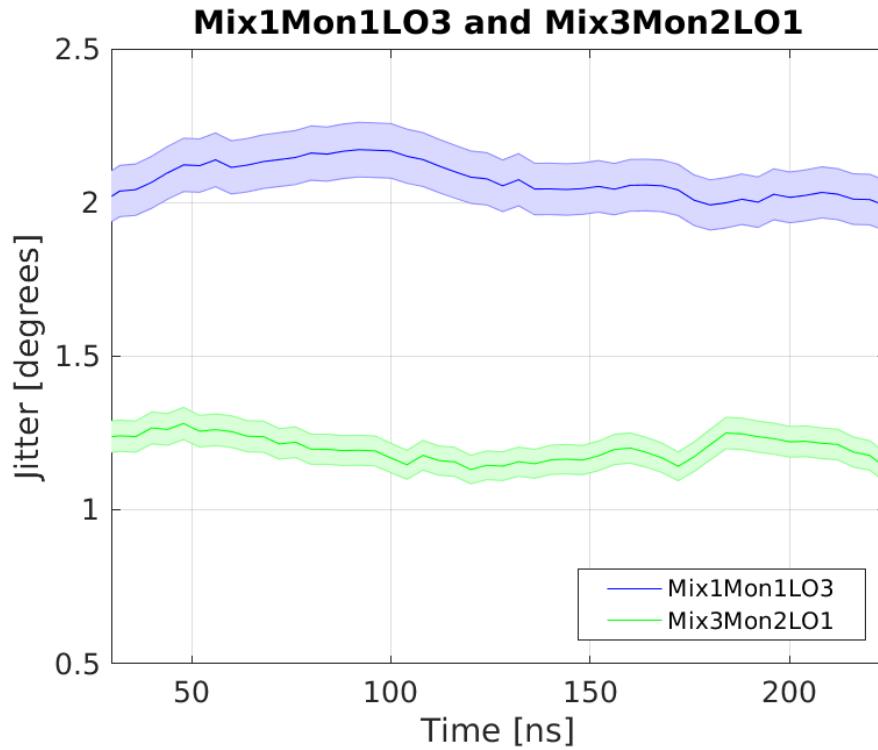


Figure 1.39: Phase jitter along pulse with the LO swapped between the third mixer and the first mixer.

Mon 1			Mon 2		
Mixer	LO	Jitter	Mixer	LO	Jitter
1	1	$0.83 \pm 0.01^\circ$	2	2	$1.38 \pm 0.01^\circ$
2	2	$1.48 \pm 0.02^\circ$	1	1	$0.89 \pm 0.01^\circ$
1	1	$1.15 \pm 0.01^\circ$	3	3	$1.91 \pm 0.01^\circ$
1	2	$1.68 \pm 0.01^\circ$	2	1	$1.10 \pm 0.01^\circ$
1	3	$2.07 \pm 0.01^\circ$	3	1	$1.20 \pm 0.01^\circ$

Table 1.9: Comparison of phase jitter along the pulse for each measurement with different setups of the electronics. Each row corresponds to the results of one dataset. The left hand side of the table shows the results from Mon 1 in that dataset, and the right hand side of the table the results from Mon 2. Bold text indicates the lower jitter value in that dataset, all of which use LO 1.

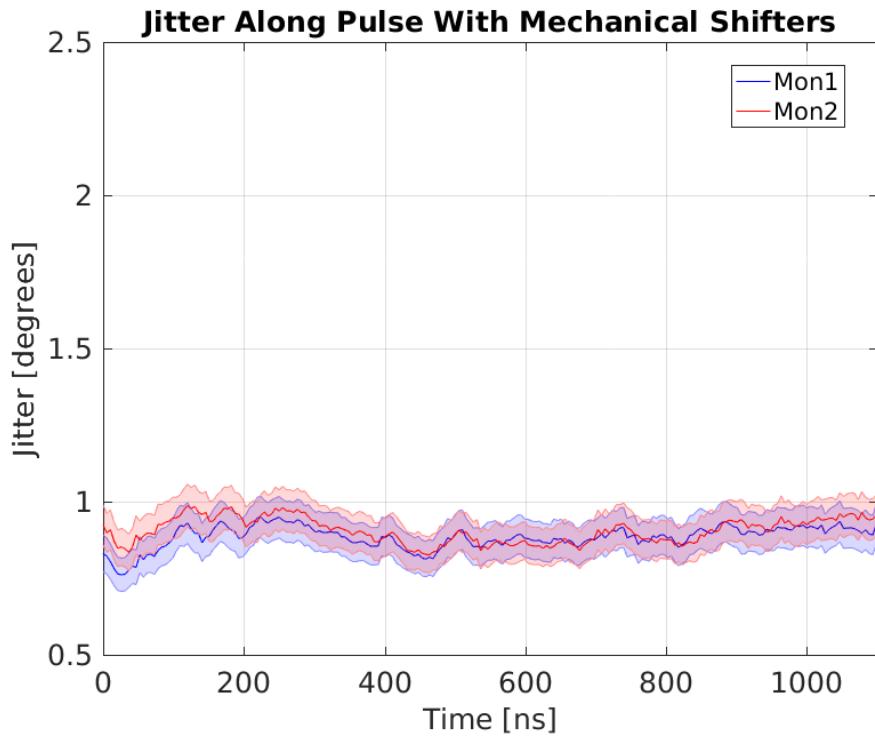


Figure 1.40: Phase jitter along pulse after installation of the mechanical phase shifters.

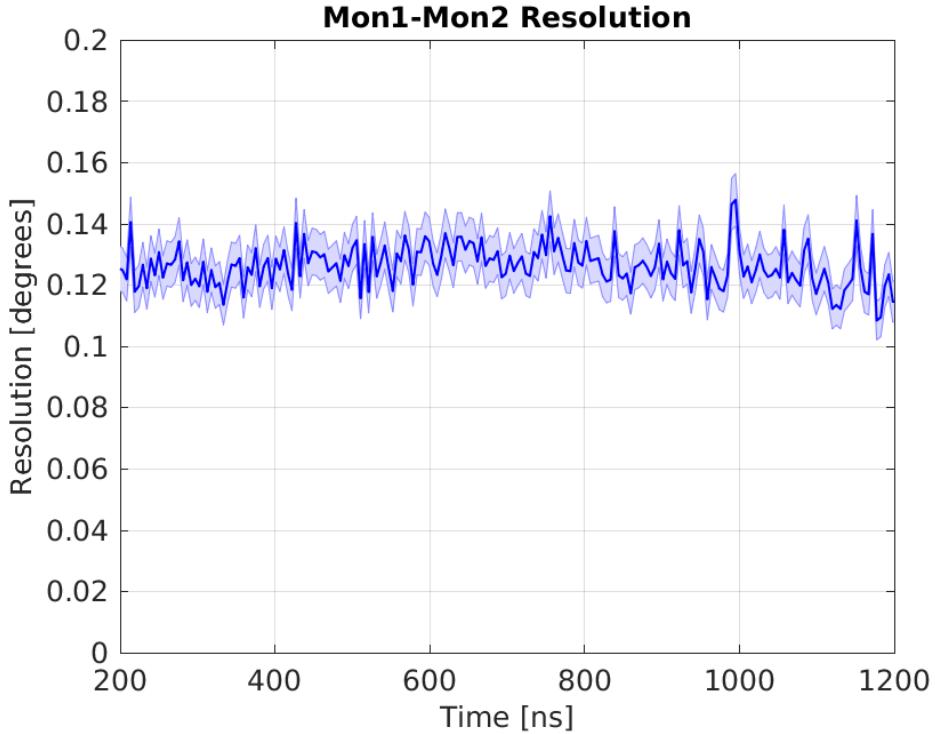


Figure 1.41: bestResolution

1.9.1 Best Resolution

Figure 1.41 shows the best phase resolution that has been achieved to date sample by sample along the pulse. Each point corresponds to the phase jitter in the difference between the measured Mon 1 and Mon 2 phase divided by $\sqrt{2}$ as per Equation 1.27. The resolution is quite stable along the pulse, with a mean value of $0.1257 \pm 0.0005^\circ$. This is below the 0.14° needed to be able to theoretically achieve a 0.2° correction with the PFF prototype, as derived in Section 1.3. The achieved resolution corresponds to a theoretical limit of around 0.18° in the corrected downstream phase jitter.

1.9.2 With Sample Averaging

The phase monitor signals are digitised with a much higher sampling rate, 357 MHz on the FONT5a board or 192 MHz on the SiS digitisers, than the PFF correction bandwidth of around 30 MHz. This means the results from several samples could be averaged to reduce noise on the measurement whilst maintaining the same correction bandwidth. For example, for a measurement on the SiS digitisers, such as those shown here, 5 samples can be averaged to effectively create a signal with 38.4 MHz sampling rate, reduced from the initial 192 MHz. The effect of doing this is shown in Figure 1.42. The resolution is decreased from $0.1257 \pm 0.0005^\circ$ as seen previously to $0.1077 \pm 0.0005^\circ$ with 5 samples averaged. Currently the phase propagation (Chapter ??) is the main limiting factor for the PFF performance rather than the phase monitor resolution. However, it would be possible to implement sample averaging in the PFF firmware on the FONT5a board if deemed necessary for future tests

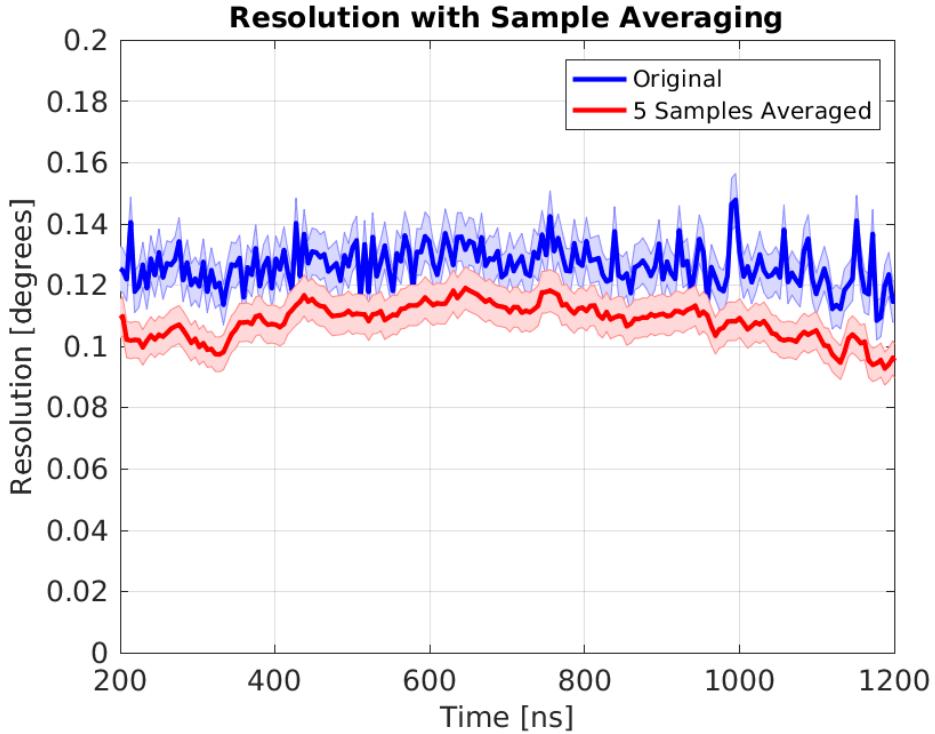


Figure 1.42: Effect on resolution by averaging samples.

[REF].

1.9.3 Dependence of Resolution on LO Phase

The process of setting the mixers on their zero crossing after calibrations was documented in Section 1.7.4. This is necessary to operate the mixers where there output voltage is most sensitive to variations in the phase (close to the peaks of the mixer output there is negligible change in output voltage for small changes in phase). The dependence of the phase resolution on the beam phase across the full $\pm 180^\circ$ range is shown in Figure 1.43. The plotted phase is the offset between the LO phase shifter setting and the calculated optimal setting. More than 50° away from the zero crossing there is a large degradation in resolution, reaching above 1 degree at the $+90^\circ$ peak.

However, for the PFF system the phase resolution only needs to be guaranteed within its correction range, which is close to $\pm 6^\circ$ as seen in Section 2.4.1. In Figure 1.44 it is seen that there is no noticeable degradation in resolution in the range between $\pm 15^\circ$.

1.10 Bandwidth

The overall targeted bandwidth for the prototype PFF correction is 30 MHz, which means each individual hardware component must have a bandwidth in excess of 30 MHz. [TODO: What was the bandwidth target for the phase monitors? Some mentions of 100 MHz when

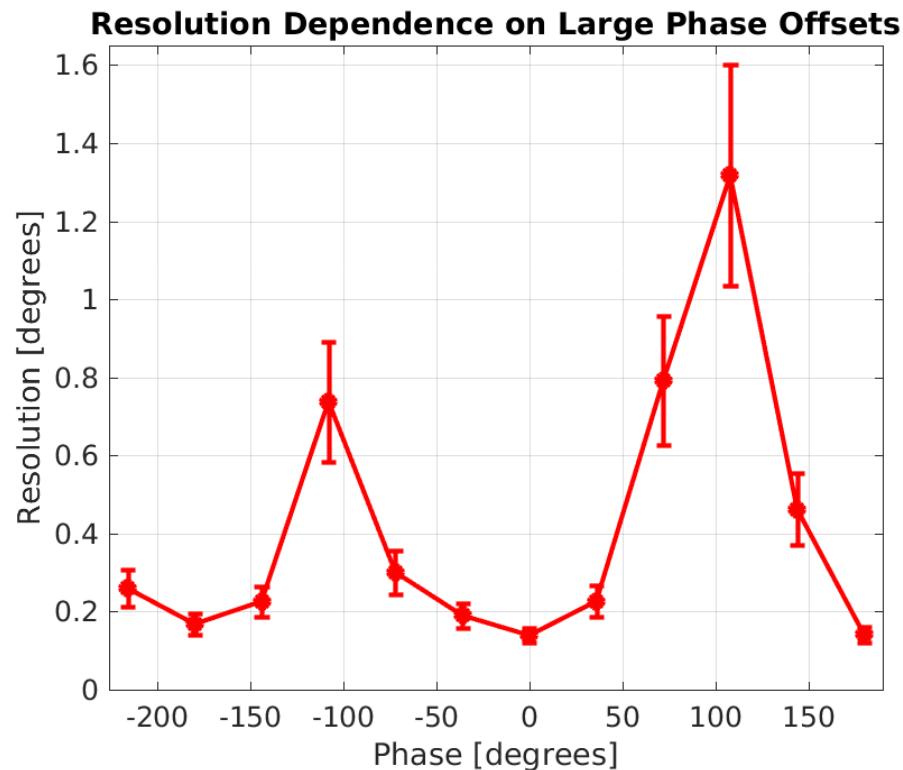


Figure 1.43: Resolution.

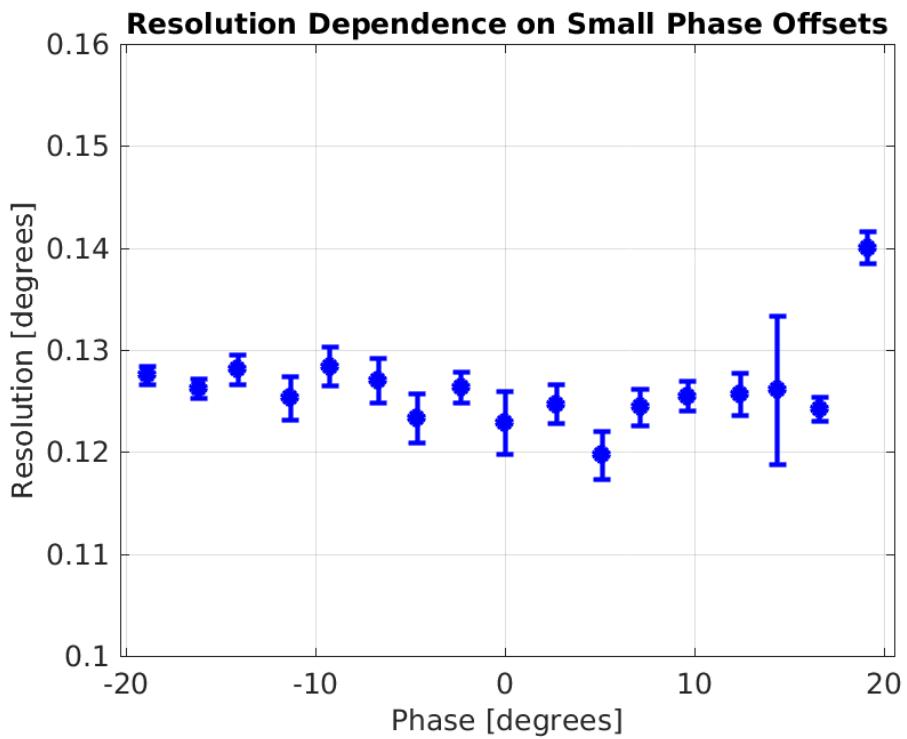


Figure 1.44: Resolution.

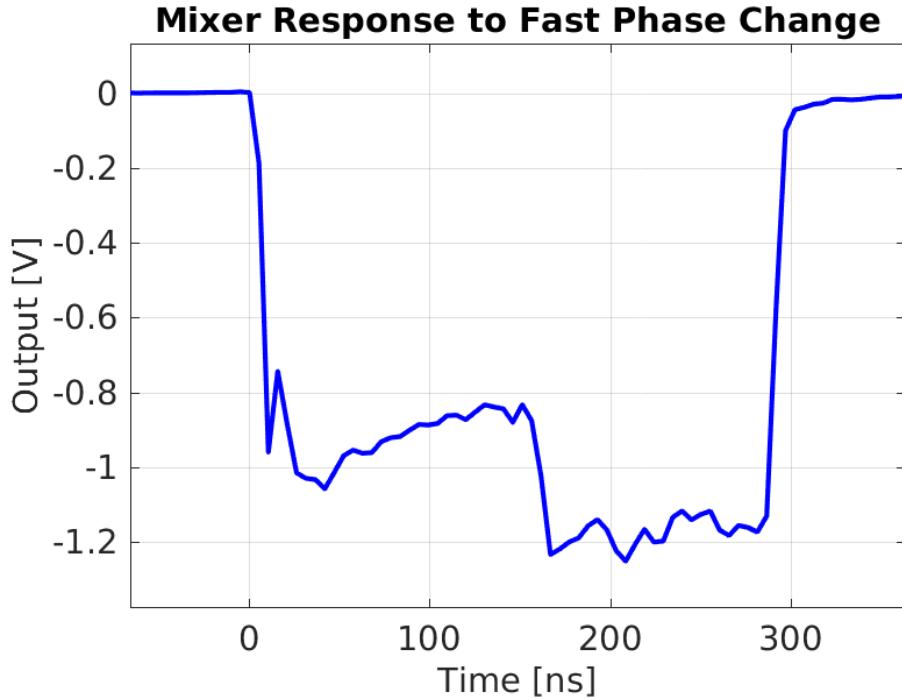


Figure 1.45: Response of Mixer 3 to a jump in phase in the middle of the pulse.

talking about some reflection parameter in design paper. Maybe electronics is the main limitation?]

To estimate the bandwidth of the phase measurement the delay loop can be used to create a sharp jump in the phase mid-way along the pulse. [TODO: don't understand how to create a 280 ns continuous pulse with half delayed beam and half straight beam.] As Mon 1 and Mon 2 are prior to the delay loop only the bandwidth of Mon 3 can be verified in this way.

Figure 1.45 shows the response of Mon 3 mixer to a beam pulse with a phase step setup in this way, where the first 140 ns of the pulse corresponds to the beam bypassing the delay loop and the second half of the pulse corresponding to the beam entering the delay loop.

The time taken for the mixer output to respond to the fast phase change can be related to the bandwidth by this approximate relationship [REF]:

$$\text{BW} = \frac{350}{t} \quad (1.40)$$

Where BW is the bandwidth in MHz and t is the rise time of the signal in ns.

The transition between the two phase states as seen on the mixer output occurs between 156.6 ns and 167.0 ns, a rise time of 10.4 ns corresponding to a bandwidth of approximately 34 MHz. In addition, the falling edge of the mixer output at the end of the pulse also takes around a 10 ns, also leading to a bandwidth estimate in the region of 35 MHz.

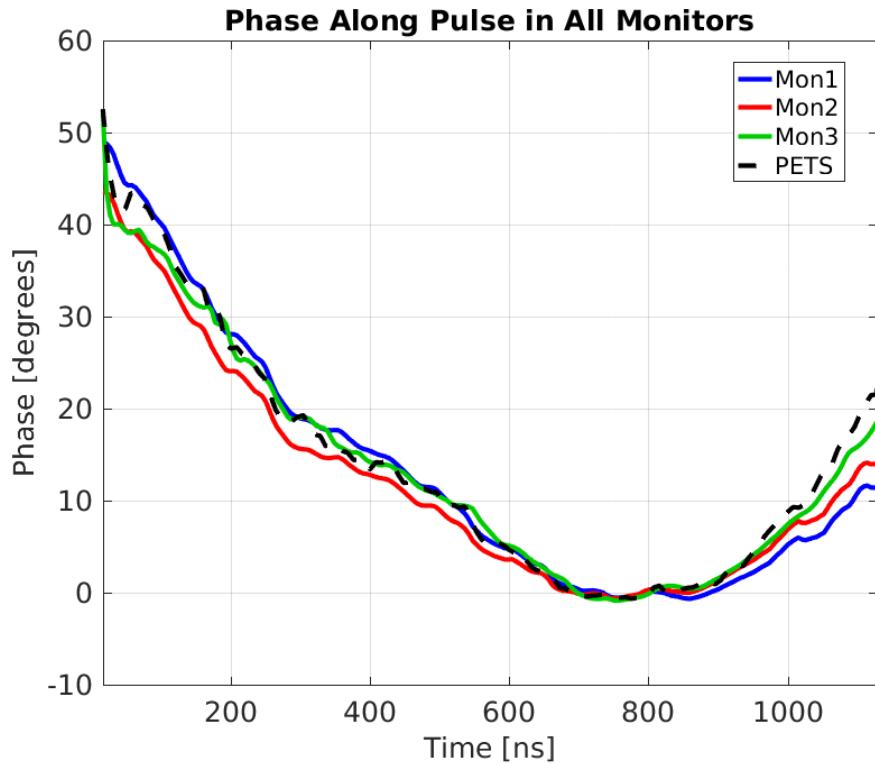


Figure 1.46: Comparison of phase along the pulse in the three PFF phase monitors and an alternative phase measurement from a PETS.

1.11 Comparison of Measured Phase Along Pulse

It has been shown that the phase jitter is at the same level in each monitor after the installation of mechanical phase shifters, and that the achieved resolution is better than the level needed to be able to theoretically achieve a 0.2° PFF correction. Nevertheless there are several remaining effects that have been identified which may limit the PFF performance in a way not described by the resolution. These are the focus of the remainder of this chapter, starting with differences between the measured shape of the phase along the pulse here. Neither the phase jitter nor the resolution are sensitive to any static differences in the measured phase in each monitor. For the PFF system to remove not only phase jitter but also to flatten the phase sag along the pulse the shape of the upstream and downstream phase must be the same.

Figure 1.46 shows an example of the measured phase along the pulse in all three monitors, as well as a fourth phase measurement taken from one of the power extraction and transfer structures (PETS) in the TBL line after Mon 3 [REF]. The PETS measurement provides an independent cross-check of the response and calibration of the three PFF monitors. All four phase measurements show approximately the same overall phase sag of around 45° along the full pulse length, as desired.

Nevertheless, there are differences between the measurements. As described later in Chapter ?? there are many mechanisms by which the beam phase can change between the

upstream and downstream monitors. Small discrepancies between the Mon 1 and Mon 2 phase compared to the Mon 3 and PETS phase are therefore not unexpected. However, as Mon 1 and Mon 2 are neighbouring each other in the beam line their measurements are expected to agree almost perfectly but this is not the case. At the start of the pulse the Mon 2 phase is around 6° lower than the Mon 1 phase, whereas at the end of the pulse the Mon 2 phase is around 2° higher than the Mon 1 phase, for example.

Two possible explanations could have been an error in the fitted calibration amplitude or a time offset between the two signals. The fact that the Mon 2 phase is lower at one end of the pulse but higher at the other means that the difference is not simply a scale factor between the two, and therefore cannot be described by an error in calibration amplitude. Neither can it be explained by differences in the calibration constants along the pulse, as seen in the next section. Similarly, by observing small variations along the pulse, for example at the end of the pulse after a time of 1000 ns in the figure, it can be seen that the two measurements are well aligned in time.

The blue line in Figure 1.48 shows the difference between the Mon 1 and Mon 2 phase along the pulse. The offset between the two has a clear linear dependence on the time along the pulse. As a result, one way in which the agreement between the two measurements can be improved is by rotating Mon 2 with respect to Mon 1 about a time of 850 ns where the offset between the two is zero. With an optimal rotation of 2.1° the mean absolute offset between Mon 1 and Mon 2 between 370 ns and 1080 ns can be reduced from $1.44 \pm 0.08^\circ$ to $0.12 \pm 0.01^\circ$. The red line in the figure shows the difference along the pulse after performing this rotation. Figure 1.46 then shows a comparison between the mean phase along the pulse in Mon 1 and Mon 2 after the rotation, with the original measurement from Mon 2 also shown for reference. The agreement in shape between the two is now excellent, with only a slight discrepancy at the end of the pulse.

The source of this apparent rotation between Mon 1 and Mon 2 is not clear and could be an effect of the monitors themselves, the calibration process or a real difference between the beam phase in each monitor. If there was a real rotation in the phase sag between monitors or if there was an issue with Mon 1, used as the PFF correction input, it would not be possible to completely flatten the phase sag along the pulse with the PFF system. The excellent flattening of the pulse that has in reality been achieved with the PFF system (Chapter ??) suggests this may be an issue affecting only Mon 2, as the correction input is based solely on Mon 1. An issue with the measured pulse shape from Mon 2 may also help to explain differences between the shape of the applied kick and the upstream phase (measured by Mon 2) seen later in Section 2.4.3.

1.12 Effect of Variations in Calibration Constant

In Section 1.7.3 it was shown how the calibration parameters vary along the pulse. In the PFF algorithm, and usually also in data analysis, single values for each calibration constant are used across the full pulse length. This will lead to small discrepancies between the measured phase and the true beam phase. Examples of the size of this effect are shown in

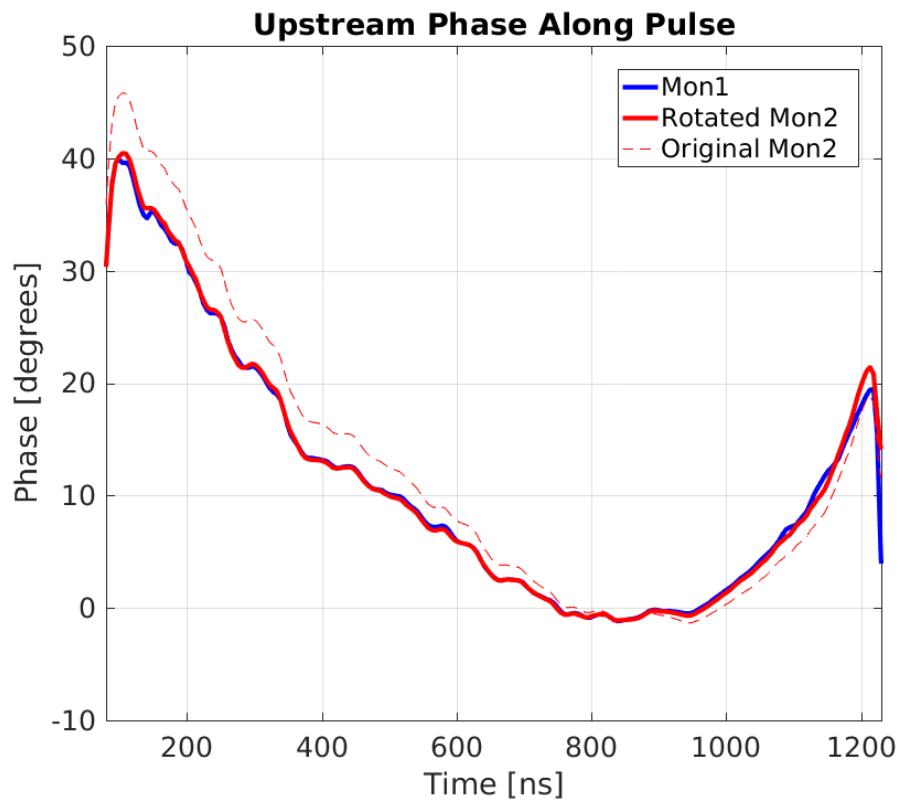


Figure 1.47: Comparison of Mon 1 and Mon 2 phase along the pulse, with Mon 2 rotated by 2.1° about a time of 850 ns on the horizontal axis.

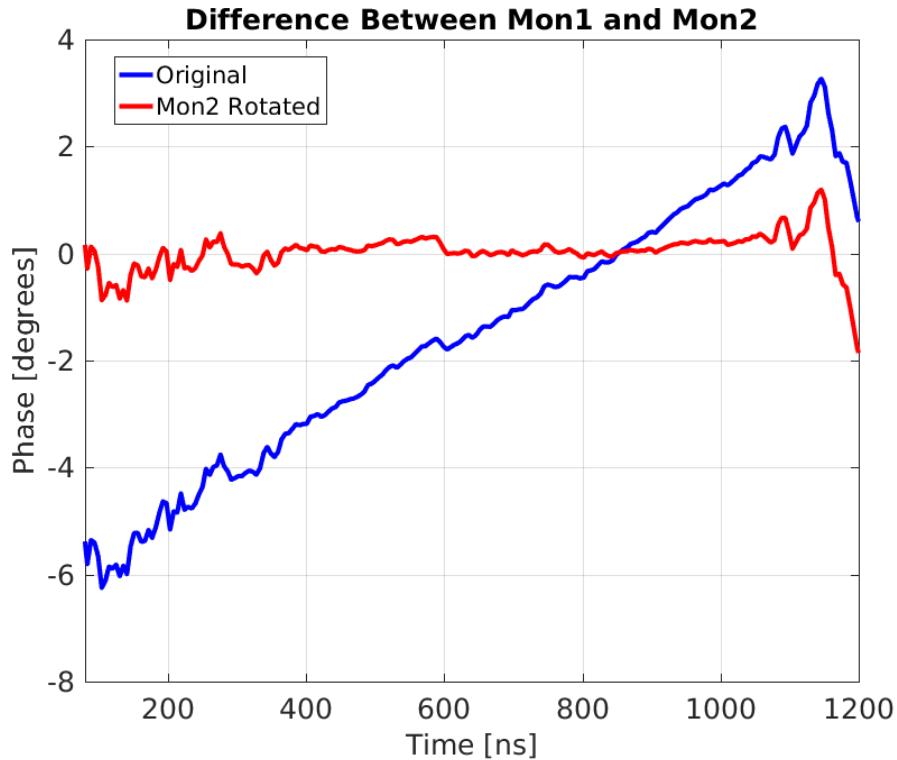


Figure 1.48: Difference between Mon 1 and Mon 2 phase along the pulse with and without Mon 2 rotated.

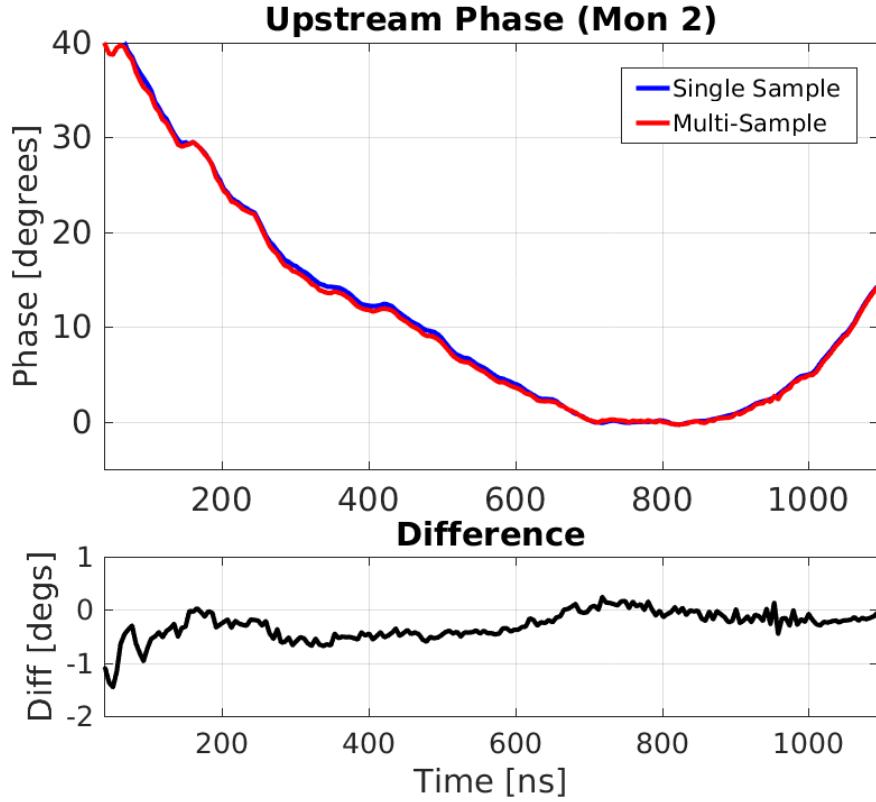


Figure 1.49: Effect of using a varying calibration constant on the upstream phase.

Figures 1.49, for Mon 2, and in Figure 1.50 for Mon 3, comparing the measured phase along the pulse when using single value calibration constants or varying calibration constants along the pulse. In the range between 600 ns and 1000 ns around the middle of the pulse where the phase sag is flattest (the part of interest for the PFF system) using a varying calibration constant along the pulse makes almost no difference to the measured upstream phase. This is unsurprising as the calibration constants normally used are calculated from one sample in this range. Outside this range the difference between the two reaches a peak of 1.5° near the start of the pulse.

For the downstream phase the differences are larger, including up to 1.5° offsets between the two methods in the range of interest for the PFF system. However, the example shown is without fully optimised downstream beam conditions achieved in Chapter ?? and so represents a worst case scenario for normal PFF operation. The PFF correction quality also does not directly depend on the downstream phase measurement (apart from for the gain calculation, as derived in Section ??), so these differences can be removed in offline analysis if deemed necessary.

1.13 Dependence on Position

As discussed in Section 1.1 the phase monitor output from the two vertical RF feedthroughs are summed in hybrids, and it is this sum signal that is connected to the mixers. This

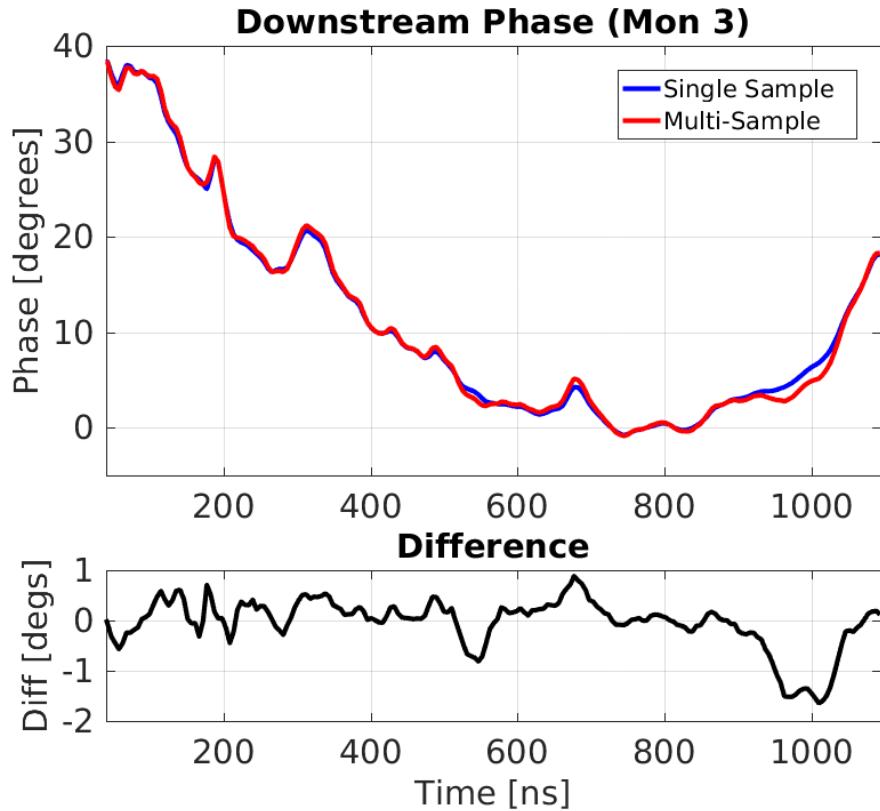


Figure 1.50: Effect of using a varying calibration constant on the downstream phase.

reduces, but does not remove completely, the dependence of the phase monitor signal power on the beam position in the monitor. In this section the remaining position dependence of the phase measurement is determined. Understanding the magnitude of the effect is particularly important considering the diodes are no longer used to power normalise the mixer output as originally intended.

The magnetic corrector placed roughly 1 m prior to Mon 1 (labelled CT.DHD0360) has been used to scan the beam position in the upstream phase monitors both horizontally and vertically. Around 1 m following Mon 2 there is a quadrupole (CT.QFF0420) followed by a beam position monitor or BPM (CT.BPM0430). For the purposes of this measurement the quadrupole is turned off so that the whole 3.5 m length of beam line between the corrector and the BPM is a drift space. It is then straightforward to reconstruct the position offset in the two phase monitors based on the BPM measurement without having to rely on the MADX model to take in to account the effect of the quadrupole on the beam orbit. A diagram of the locations of the correctors, phase monitors, quadrupole and BPM is shown in Figure [REF]. Distances between the elements are shown in Table 1.10.

[TODO: Diagram of corrector, mon1, mon2, quad, bpm locations]

In these conditions a position offset of x_{430} measured in the BPM (in horizontal or

Device	Distance From CT.0360	Label
Mon 1	104.5 cm	s_{M1}
Mon 2	144.5 cm	s_{M2}
CT.BPM0430	357.0 cm	s_{430}

Table 1.10: Distance of the upstream phase monitors and following BPM CT.0430 to the corrector CT.0360 before the phase monitors.

vertical) corresponds to the following position offsets, x_{M1} and x_{M2} , in each phase monitor:

$$x_{M1} = r_{M1}x_{430} \quad (1.41)$$

$$x_{M2} = r_{M2}x_{430} \quad (1.42)$$

Where r_{M1} and r_{M2} are the position offsets in the phase monitors per unit position offset in the BPM, given by:

$$r_{M1} = \frac{s_{M1}}{s_{430}} \quad (1.43)$$

$$r_{M2} = \frac{s_{M2}}{s_{430}} \quad (1.44)$$

Where s_{M1} , s_{M2} and s_{430} are the distances between the corrector and the phase monitors (s_{M1} , s_{M2}) or BPM (s_{430}). Substituting in the values from Table 1.10 gives values of $r_{M1} = 0.29$ and $r_{M2} = 0.41$.

Figure 1.51 shows the results of a horizontal position scan in the upstream phase monitors, with the phase plotted against the horizontal position in the BPM. Position scans of this type require a long time to complete in order to be able to acquire enough statistics at multiple corrector settings. The scan presented represents a data taking period of around one hour, for example. This means real drifts in beam phase (aside from any position dependent effects on the monitor signals) are unavoidable during the scan. The first impression of Figure 1.51 is that the only visible change in measured phase is due to actual drifts in beam phase rather than being as a result of the changes in position. However, Figure 1.52 shows the response of the phase monitor diode signals to the horizontal position in the BPM during the scan. Even though the diodes are heavily saturated a dependence of their output, and so a dependence of power, on the position is visible. This suggests there should also be a visible effect on the phase.

To remove the effects of drifts in the beam phase the difference between the measured Mon 1 and Mon 2 phase can be considered instead. The true beam phase, ϕ_b , should be identical in Mon 1 and Mon 2, so any differences between their measurements ϕ_{M1} and ϕ_{M2} during the scan can be modelled as coming from the beam position in the monitor, as follows:

$$\phi_{M1} = \phi_b + c_{M1}x_{M1} \quad (1.45)$$

$$\phi_{M2} = \phi_b + c_{M2}x_{M2} \quad (1.46)$$

Where c_{M1} and c_{M2} are constants expressing the phase shift per unit position offset in each monitor. The difference between the measured phase in Mon 1 and Mon 2 is therefore given

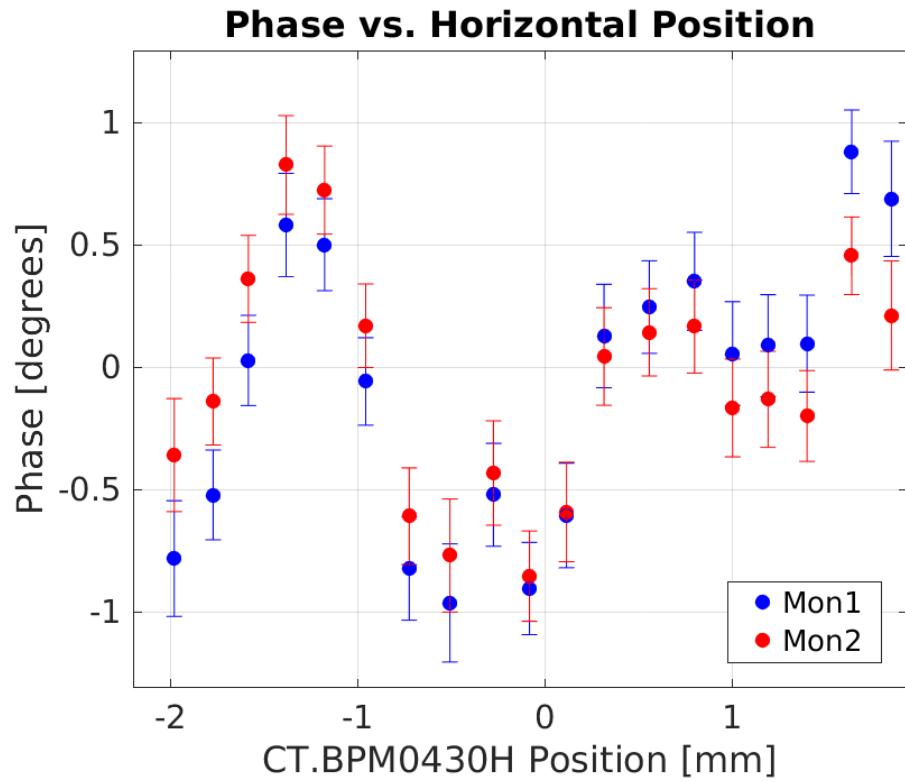


Figure 1.51: Mon 1 and Mon 2 phase dependence on horizontal position during scan.

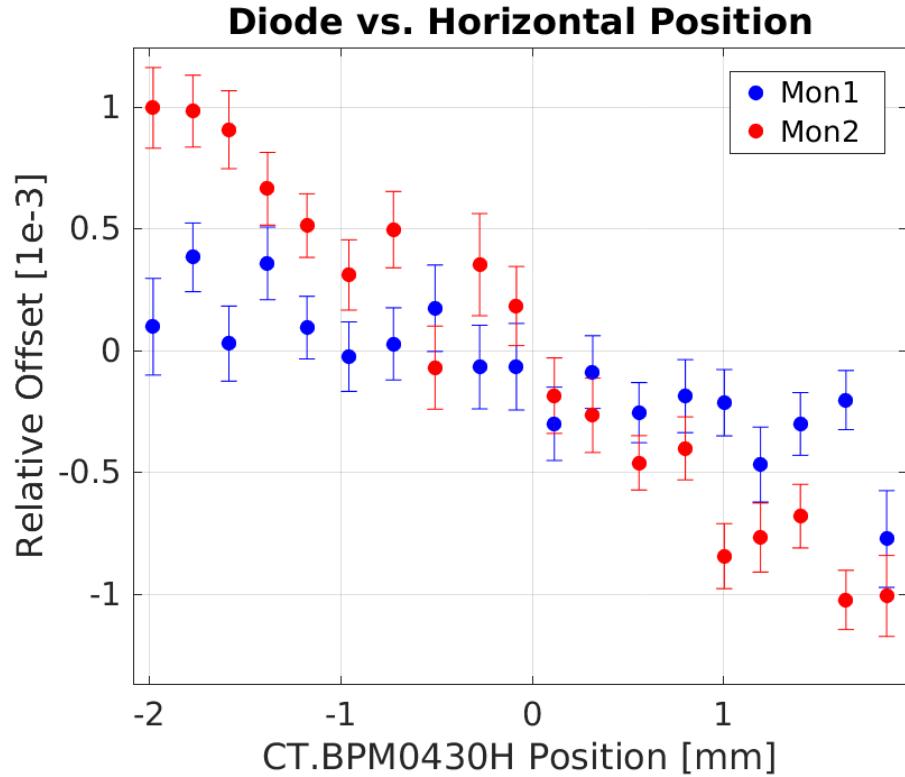


Figure 1.52: Mon 1 and Mon 2 diode dependence on horizontal position during scan.

by:

$$\phi_{M2} - \phi_{M1} = c_{M2}x_{M2} - c_{M1}x_{M1} \quad (1.47)$$

c_{M1} and c_{M2} cannot be determined individually from the scan results alone using this approach, so instead it will be approximated that the strength of the position dependence is the same in Mon 1 and Mon 2. Letting $c_{M1} = c_{M2} = c$ finally gives:

$$\phi_{M2} - \phi_{M1} = c(x_{M2} - x_{M1}) \quad (1.48)$$

$$c = \frac{\phi_{M2} - \phi_{M1}}{x_{M2} - x_{M1}} \quad (1.49)$$

The expressions for x_{M1} and x_{M2} in terms of the BPM position x_{430} derived earlier can then be substituted in to give:

$$c = \frac{\phi_{M2} - \phi_{M1}}{x_{430}(r_{M2} - r_{M1})} \quad (1.50)$$

The gradient of the phase difference versus the position offset in the BPM, $(\phi_{M2} - \phi_{M1}) / x_{430}$, is the only remaining parameter left to calculate in order to estimate c .

Figure 1.53 shows how the difference between the Mon 1 and Mon 2 phase measurement depends on the horizontal position in the BPM during the scan. By removing the actual beam phase drifts the dependence of the phase measurements on the beam position becomes clear. The fitted gradient is $-0.22 \pm 0.01^\circ$ per mm offset in the BPM. Using Equation 1.50 this corresponds to a phase shift of $-1.84 \pm 0.07^\circ$ per mm offset in the phase monitors themselves.

Exactly the same process can be repeated in the vertical plane, and the results of doing this are shown in Figure 1.54. Although the effect is smaller there is still a visible dependence of the phase on the vertical position, in this case with a gradient of $0.06 \pm 0.01^\circ$ per mm offset in the BPM corresponding to $0.53 \pm 0.07^\circ$ per mm vertical offset in the phase monitors.

The position dependence of the measurement appears large when quoted like this but it must be remembered that millimetre scale changes in beam orbit are rare during normal operation. Orbit jitter at CTF3 around the location of the upstream phase monitors is typically at the 0.02 mm level [REF]. Taking the calculated position dependence of Mon 1 and Mon 2 this corresponds to only an additional measured phase jitter of roughly 0.04° , using the larger dependence in the horizontal plane. This is only a small contribution to the overall phase monitor resolution of around 0.13° as seen in Section 1.9. However, it is important to consider that any change in beam setup that alters the trajectory through the monitors will lead to a change in output power and therefore a change in calibration constants. Calibrations are always repeated when the CTF3 setup is changed to take this in to account. Position scans around the region of the downstream phase monitor Mon 3 would be much more difficult to perform and have not yet been attempted. The effect should be of a similar magnitude, although the downstream beam is less stable than upstream so the contribution to measured phase jitter is likely to be slightly larger.

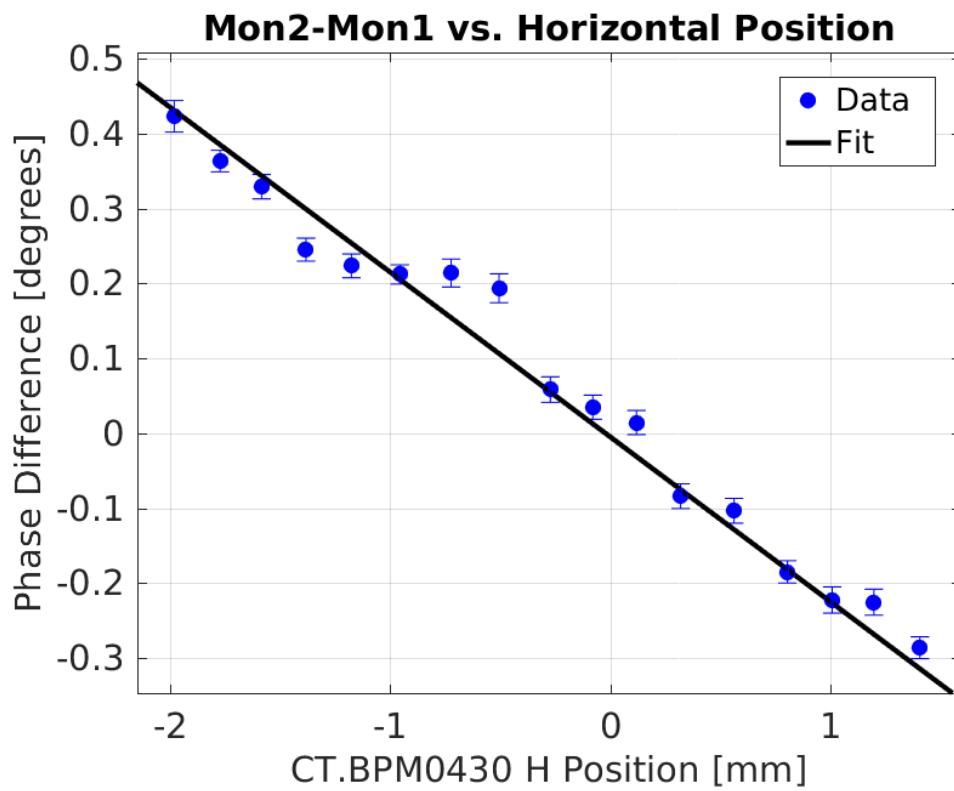


Figure 1.53: Fit to difference between Mon 1 and Mon 2 phase versus horizontal position.

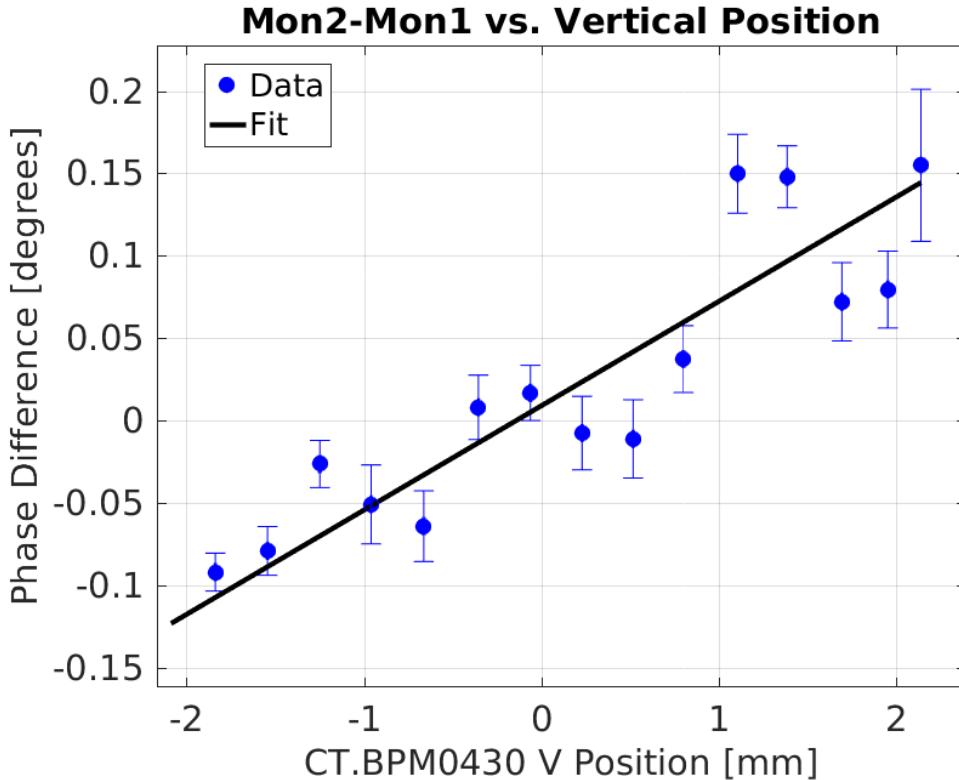


Figure 1.54: Mon 1 and Mon 2 dependence on horizontal position during scan.

Chapter 2

Setup and Commissioning of the PFF System

This is the introductory text. [1]

2.1 Feedforward Controller (FONT5a Board)

This section describes the design, firmware and operational aspects of the FONT5a board, which acts as the PFF controller. Its role is to digitise the signals from the first upstream phase monitor (Mon 1), process them and calculate the appropriate voltage with which to drive the kicker amplifiers in order to correct the phase downstream. In addition it must ensure the timing of the correction output is such that the drive output from the amplifiers reaches the kickers precisely in time with the beam.

The FONT5a board is a custom built digital board designed and constructed by the FONT group at Oxford University [REF]. More details of the design of the board and the internal components can be found in [REF]. It was initially built as the controller for prototypes of an IP (interaction/beam collision point) position feedback for future linear colliders, either ILC or CLIC. Tests of this feedback are ongoing at ATF2, KEK in Japan [REF]. At the heart of the FONT5a board is a Xilinx Virtex-5 field programmable gate array (FPGA) [REF], an integrated circuit with customisable logic that the user can program as desired for his or her application. Exactly the same hardware can therefore be used for the PFF and IP feedback controllers, with different firmware loaded on to the FPGA to take in to account the different signal processing required for the input and output signals in each application.

An annotated picture of the FONT5a board front panel is shown in Figure 2.12. Apart from the FPGA (inside the board and therefore not seen in the figure) the main components of the FONT5a board are nine analogue to digital converters (ADCs) and four digital to analogue converters (DACs). In addition there is a serial RS232 port used to communicate with a LabVIEW data acquisition and control system (DAQ), a JTAG connector used to program the firmware on the FPGA should it need to be changed, and several other inputs



Figure 2.1: racks

and outputs mostly used for the timing and triggering of the board.

The outputs from the phase monitor electronics, mixer and diode signals, are connected to the ADC inputs on the FONT5a board. Usually only the Mon 1 outputs are connected to the FONT5a board, with the diode on ADC 1 and the mixer on ADC 2, although the signals from additional monitors can be connected if needed. The ADCs are 14-bit with an input range of ± 0.5 V. Due to the expected noise on the ADCs the least significant bit is discarded and only the most significant 13 bits are processed by the FPGA [REF]. The processed ADC outputs therefore have a range of ± 4096 values or “counts”, corresponding to 0.12 mV per ADC count. More details on the digitisation of the phase monitor signals were given in Section 1.4.

Each ADC output can have a non-zero mean voltage in its baseline noise. To be able to remove these intrinsic voltage offsets each analogue input is combined with the output from a DAC, labelled “trim DACs” (separate from the DACs used as the PFF correction outputs). By varying the trim DAC voltages it can be ensured that the baseline output of each ADC is 0 V, so that its full ± 0.5 V range can be used for the signal of interest.

For the PFF system the ADCs are usually clocked at a sampling rate of 357 MHz, generated by an external clock generator [REF] and connected to the “FST CLK” input on the FONT5a board. 357 MHz is used for historical reasons, as this is the sampling rate for which experience has been gained for the IP feedback applications. The start of the ADC sampling window is determined by an external 0.8 Hz trigger derived from the CTF3 timing and therefore locked to the beam. The trigger is connected to the “DIG IN B” input on the board, and arrives [TODO: how much] before the beam to take in to account the ADC warmup time.

After being processed on the FPGA the calculated correction outputs are sent to the DAC outputs, which are 14-bit with an output range of ± 2 V to match the required range for the input of the PFF kicker amplifiers. Only DAC 1 and DAC 2 are used for the PFF system, the other two DACs are unused. In addition the FONT5a board generates the trigger for the amplifier, which is sent from the “AUX OUT A” output and must arrive at the amplifier [TODO: how much] before the DAC output signals.

Finally, the FONT5a board is controlled using a LabVIEW data acquisition system (DAQ) documented in [REF], with communication between the board and the DAQ via the serial RS232 port. An example screenshot from the DAQ is shown in Figure 2.3. It provides functionality to change all the setup parameters in the FONT5a firmware for the PFF system setup, view the current ADC inputs and DAC outputs in real time and to save data directly from the FONT5a board. However, as the FONT5a board and DAQ currently run as a standalone system at CTF3, PFF data is usually saved via the CERN control system and SiS digitisers where data from other devices, such as BPMs, can be saved in sync with the phase monitor signals as discussed in Section 1.4. The DAQ runs on a Windows PC next to the racks used for the phase monitor electronics, FONT5a board and amplifier. The PC can be connected to via remote desktop to allow the FONT5a board to be controlled in the CTF3 control room.

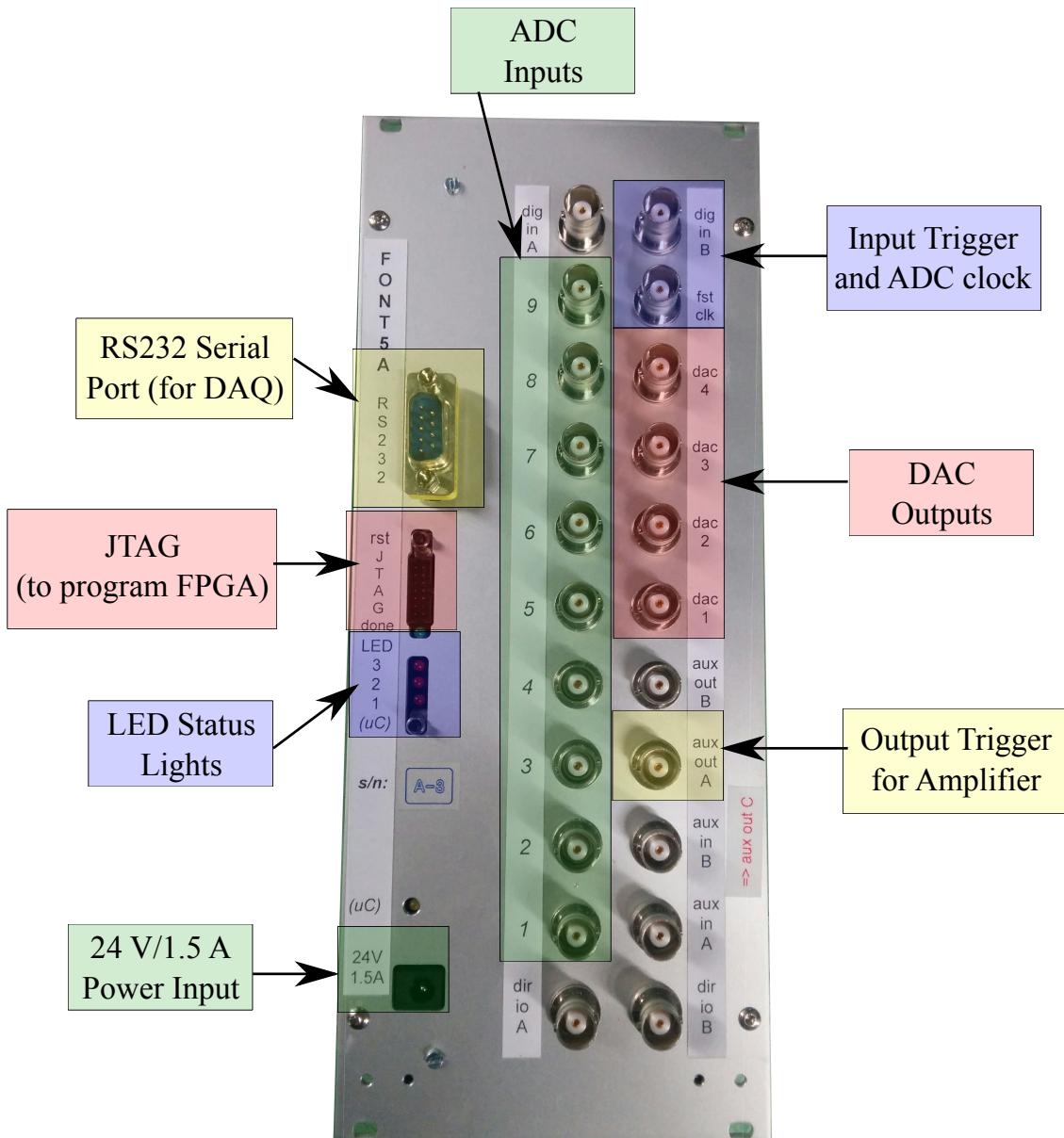


Figure 2.2: Front panel of the FONT5a board. All the connectors relevant to PFF operation are highlighted, the remaining connectors are not used at CTF3. All connectors are BNC apart from the power connector, RS232 serial port used to communicate with the LabVIEW data acquisition system (DAQ) and the JTAG connection used to program the firmware on the FPGA. The use of the ADCs, DACs and timing (trigger and clock) connections is summarised in Figure 2.4.



Figure 2.3: Diode output along the pulse with the IIR filter off and on.

2.1.1 Implementation of PFF Correction

The diagram in Figure 2.4 shows all the connections to and from the FONT5a board that were introduced in the previous section, from the phase monitor and timing inputs on the left side of the diagram to the outputs for the amplifier and DAQ on the right side of the figure. The central portion of the figure shows a simplified version of how the FONT5a firmware calculates and applies the PFF correction. All the parameters shown in blue, and several others not shown in the diagram but described later in this section, must be correctly set (via the DAQ) for operation of the PFF system.

The basic logic of the firmware is as follows. The ADC timing, sampling rate and start time, are determined by the input trigger and external 357 MHz clock. During the set sampling window the ADC outputs are processed, including a number of channel offsets and filters. The processed ADC 2 (Mixer) output is then split into two, to create the two strands that become the DAC 1 and DAC 2 outputs. Note that as the Mixer is used directly (rather than $\arcsin(\text{Mixer})$) this uses the small angle approximation. The effect of this is discussed in Section 2.1.4. If the diode (ADC 1) is being used in the calculation the ADC 2 output is also multiplied by $1/\sqrt{\text{ADC 1}}$, with values taken from a lookup table rather than being calculated directly to save latency [REF]. Prior to being sent to the DACs the two output strands are multiplied by set gain factors and then can be delayed by a set amount of time. The two calculated DAC outputs are then connected to the signal inputs on the amplifiers, where they are amplified and eventually sent to the kickers to deflect the beam and correct the phase. Meanwhile the input trigger for the FONT5a board is used to derive the trigger for the amplifier, with a variable delay that can also be set in the DAQ.

[TODO: latency of calculation (no. clock cycles)]

2.1 Feedforward Controller (FONT5a Board)

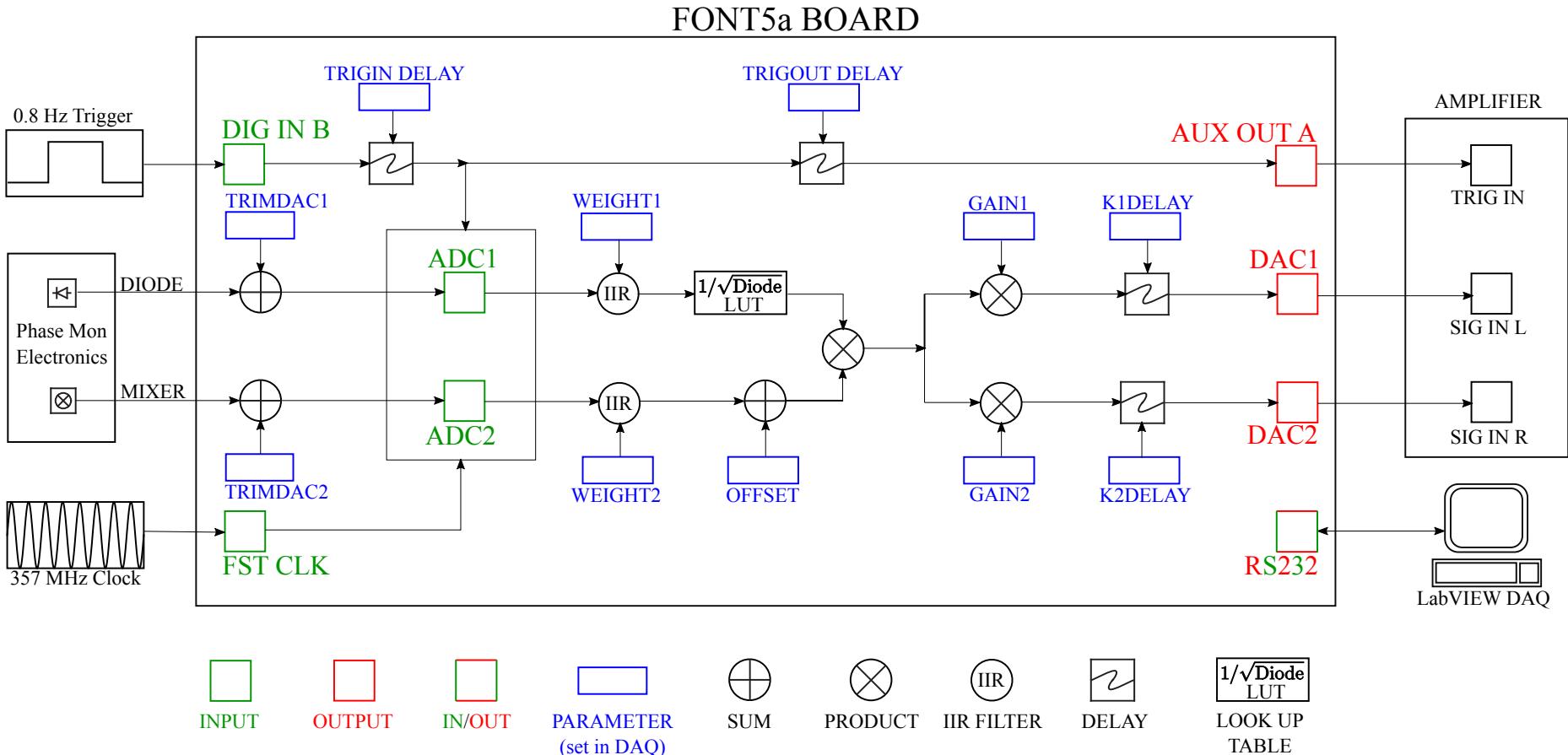


Figure 2.4: Schematic of connections to and outputs from the FONT5a board, as well as the PFF calculation in firmware in the case where the diode is used. If the diode is not used the ADC1 input is not required.

All the parameters and controls that must be adjusted during the PFF system setup, and their respective values where relevant, are listed below for reference. These are only introduced in brief here, but parameters that are either non-trivial to derive or are critical for the PFF performance are described in more detail in later sections and chapters as indicated. The values given are in FONT units as they are set in the DAQ with each parameter expressed by up to a 14 bit number, and the size of each control chosen to give a reasonable degree of flexibility around the expected set point.

[TODO: what do the font values correspond to in actual times etc.?]

Input Timing

The following parameters must be adjusted in order to set the properties of the ADC sampling as desired:

Trig in delay: The Trig in delay allows the start of the ADC sampling window to be delayed with respect to the arrival of the external trigger. Timing of the trigger and correction outputs to the amplifier (Trig out delay and K1/K2 delay) are relative to this delay, therefore changing the Trig in delay value does not effect the synchronisation of the correction output with the beam. The only requirement is to ensure that the full acquired upstream phase monitor signals arrive within the sampling window. A value of 2500 is typically used to achieve this. [TODO: Check value is correct.]

Enabled channels: The FONT5a board has 9 ADCs but only two are usually needed for the PFF system (for the mixer and diode of Mon 1 connected to ADC1 and ADC2, with the other two monitors normally connected to the SiS digitisers, see Section ??). To avoid hitting the limits of the baud rate [TODO: value?] of the RS232 port on the PC the remaining ADC channels can be disabled so their data is not transmitted.

No. samples: The length of the ADC sampling window, in number of samples, can also be varied. Typically 900 samples are used, covering a time window of $2.5 \mu\text{s}$ with the 357 MHz clock. If the signal from more than two ADCs is needed the number of samples can be reduced to avoid hitting the baud rate limit of the RS232 port on the PC, the only requirement is that the time window is long enough to encompass the full $1.1 \mu\text{s}$ beam pulse length.

ADC Signal Processing

The following parameters must be correctly set in order to remove offsets and droop in the ADC outputs:

Trim DACs: As mentioned in Section 2.1 the FONT5a board includes trim DACs in order to remove intrinsic voltage offsets in the output of each ADC. The trim DAC output is added to the ADC inputs, and each trim DAC value must be set correctly in the DAQ. For ADC1 (Diode) and ADC2 (Mixer) the Trim DAC values are 1650 and 1400 counts, respectively.

Filter Weights: IIR filters are implemented in the FONT5a firmware in order to remove droop in the ADC response, see Section 2.1.2. The filter weights for each ADC can be adjusted in the DAQ. The correct values are 50 for ADC1 (Diode) and 56 for ADC2 (Mixer).

Channel Offset: To maximise the effect of the PFF system it is necessary to zero the mean upstream mixer (ADC2) output in the central region of the pulse where the correction is being attempted (the start and end of the pulse can not be fully corrected due to the large phase sag, so the central portion is usually used). Ideally this should be adjusted by varying the Mon1 phase shifter, but this can not be done remotely so the channel offset on the FONT5a board can be used instead to make small adjustments from the control room. The channel offset adds a static offset in counts to the ADC2 output, allowing the mixer output to be zeroed at any point along the pulse. The consequences of using a non-optimal Channel Offset are discussed in Section ???. For large phase offsets giving close to maximum mixer output the phase monitor resolution is degraded (Section ??) and the small angle approximation used in the FONT5a phase reconstruction (Section 2.1.4) becomes invalid, in which case the phase shifter should still be used to zero the phase.

Output Mode

The following parameters control the nature of the DAC output signals:

Feedforward enable: The DAC output can be enabled or disabled, as required.

Interleaved mode: With interleaved mode enabled the DAC outputs from the FONT5a board are only sent for half of the triggers, for example being applied to all the odd pulses but not sent for all the even pulses. This is incredibly useful for interpreting the PFF results, as well as being used for many of the other tests presented in this thesis, as it allows a comparison between beam conditions with and without an applied kick at the same time. In this case the effects of any slow drifts should be equivalent in both the kicked and non-kicked data, thus any differences between the two should be a real effect of the PFF system. Data with the DAC output disabled can also be used to simulate the expected effect of the PFF system in those conditions. All the PFF results in Chapters ?? and ?? use interleaved data.

DAC Output Mode: The DAC output to the amplifier can be sent in two modes — Sample-by-sample or Constant DAC. In Sample-by-sample mode the DAC output is as needed for the PFF system, being shaped along the pulse by the reconstructed phase multiplied by the set gain as shown in Figure 2.4. In Constant DAC output mode a constant output voltage can be sent to the amplifier across the full length of the ADC sampling window (or for a shorter time with an applied gate, see below). The majority of the results presented in the remainder of this chapter use constant DAC outputs for verification of the amplifier, optics, correction range and correction timing.

K1, K2 const DAC: In constant DAC mode the DAC output can be varied between ± 4096 counts, or ± 2 V sent to the amplifier, and can be changed independently for each output.

Gain: In sample-by-sample mode the PFF gain can also be set independently for each

correction output, with each being a 14-bit value (± 8192 units). The conversion between the gain in FONT units and the real applied gain is derived in Section 2.1.1. An applied gain of 624 units corresponds to a real gain of approximately 1 (with a gain of 624 an upstream phase offset of 1 degree corresponds to a downstream phase correction of approximately -1 degrees).

Diode Mode: The FONT5a firmware provides three modes for the treatment of the diode signal on ADC1 — normalisation, gating and unused. With diode normalisation enabled the PFF system reconstructs the phase as originally envisaged using Mixer/sqrt(Diode). Due to the issues with the phase monitor diodes as discussed in Chapter 1 the option to not include the diode in the PFF calculation and only include the mixer was later added, which is now the nominal setup. Rather than leaving the diode completely unused, it is usually used to gate the correction output (see below).

Overflow Mode: The PFF correction output can behave in three ways in the case where the calculated output is outside the maximum range of ± 4096 DAC counts. In the first iteration of the PFF firmware the calculated correction output would overflow, causing sign flips in the output in the regions where the correction range was exceeded [REF]. This behaviour can still be applied in the current firmware if desired. However, in normal operation the output is set to Saturate, so that any calculated values outside ± 4096 DAC counts are sent as the maximum ± 4096 DAC counts or $\pm 2V$ to the amplifier. A final option to provide no output at samples where the calculated output is outside ± 4096 DAC counts, is also provided.

Output Timing

The following parameters control the timing of the DAC output signals:

Trig out enable: The trigger sent to the amplifier can be enabled or disabled as required. Clearly the trigger must be enabled for any correction output to have an effect on the beam (the PFF correction output can be turned on with the amplifier trigger disabled for testing purposes).

Trig out delay: The timing of the trigger sent to the amplifier can be delayed with respect to the start of the ADC sampling window. This must be adjusted so that the arrival of the $1.1 \mu s$ beam pulse at the kickers is aligned with the $1.4 \mu s$ time during which the amplifier is powered and the correction output can be applied [REF]. A value of 110 is typically used. The precise correction timing is set by the K1 and K2 delays below.

K1, K2 delay: The K1 and K2 delay are used to fine tune the timing of the two correction outputs (DAC1/K1 for the first kicker and DAC2/K2 for the second kicker), and can be varied by up to 32 ADC clock cycles (2.8 ns per clock cycle at 357 MHz). The optimal delays are 7 clock cycles for K1 and 7–8 clock cycles for K2. The importance of the correction timing and derivation of these values is presented in Section 2.5.

Gate enable: The correction output can be restricted to a certain sample range by applying a “gate”. The gate can be defined either as a custom sample range picked by the

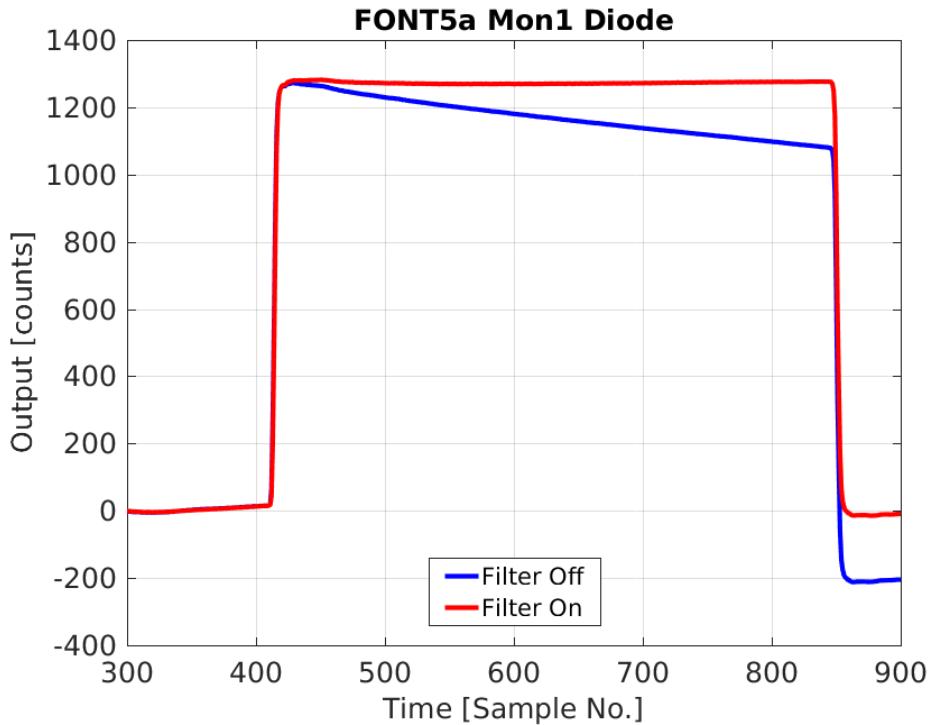


Figure 2.5: Diode output along the pulse with the IIR filter off and on.

user or the diode signal (ADC1) can be used. Diode gating is typically used so that no output is sent to the amplifier outside the time of the beam pulse. Using a custom sample range has been useful for early PFF tests and to apply a constant kick along only part of the beam pulse (this is used in Section 2.5.3, for example).

2.1.2 ADC Droop Correction

Although the FONT5a (and previous FONT5) boards have been used extensively for IP feedback tests by the FONT group prior to its application for the PFF system, it had not been routinely used to process long, microsecond like, pulse lengths such as the CTF3 beam signals. During the first tests of the FONT5 board at CTF3 (prior to the FONT5a board being available) it was immediately apparent that there was a large droop in the measured phase monitor diode outputs using the FONT ADCs. An example of this, taken from the FONT5a board, is shown in Figure 2.5, remembering that as the diodes are highly saturated the response should be close to a perfect square wave. The measured diode output droops by 200 counts (approximately 15%) across the pulse length, with this difference also visible as an offset in the baseline after the pulse.

The droop emerges as a result of the use of AC coupling on the ADC input transformers for electrical isolation. This involves using a capacitor, the current across which is dependent on dV/dt (V being voltage and t time), to remove the DC component (or mean offset) from a signal [REF]. In particular for the diode channel the output is increasingly well described by a DC signal on the flat top as you move away from the leading edge of the pulse, with the capacitor causing droop in the response as a result. There is also a small effect on the mixer

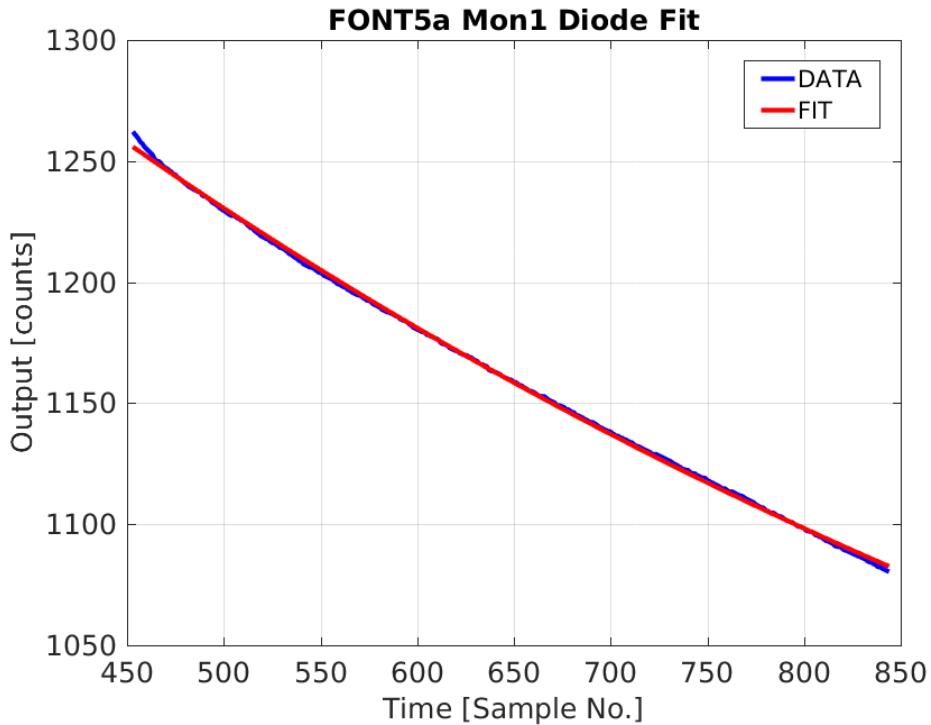


Figure 2.6: Exponential fit to diode droop.

output, as will be seen later. [TODO: Is the effect on the diode and mixer really different? Is this correctly taken in to account by the IIR filter?]

In the simplest case the droop should be well described by an exponential decay of the form $A \exp(-t/\tau)$, where t is the time or sample number along the pulse and τ is the decay time constant. For the FONT5 board this only gave a rough approximation of the true droop characteristics due to non-linear properties of the input transformers. On the updated FONT5a board the transformers were changed to both reduce the magnitude of the droop and give closer to the expected exponential decay [REF]. Figure 2.6 shows an exponential fit to the Mon1 diode output as seen on the FONT5a board (ADC1). Apart from a small deviation at the beginning of the pulse the agreement is excellent, with residuals to the fit of only up to 2 counts compared to a signal magnitude of 1250 counts. For ADC1 the fitted decay time constant is $\tau = 838 \pm 16$ samples, or $2.35 \pm 0.05 \mu\text{s}$ (with one ADC sample every 2.8 ns at 357 MHz). Each ADC on the FONT5a board has slightly different droop characteristics, with the decay time constant for ADC2 being 938 ± 18 samples, for example (calculated with the diode moved on to ADC2).

In the case where the diode is used in the phase reconstruction as originally envisaged the ADC droop would propagate in to the applied correction and create an output to the amplifier that increases with time with respect to the ideal value (as the Mixer is divided by $\text{sqrt}(\text{Diode})$). The effect on the correction is much smaller without diode normalisation but it still slightly distorts the measured Mixer input to ADC2. Therefore, a digital IIR filter has been implemented in the FONT5a board firmware to remove the exponential droop in the ADC outputs [REF]. This works by recursively adding the expected droop to the ADC

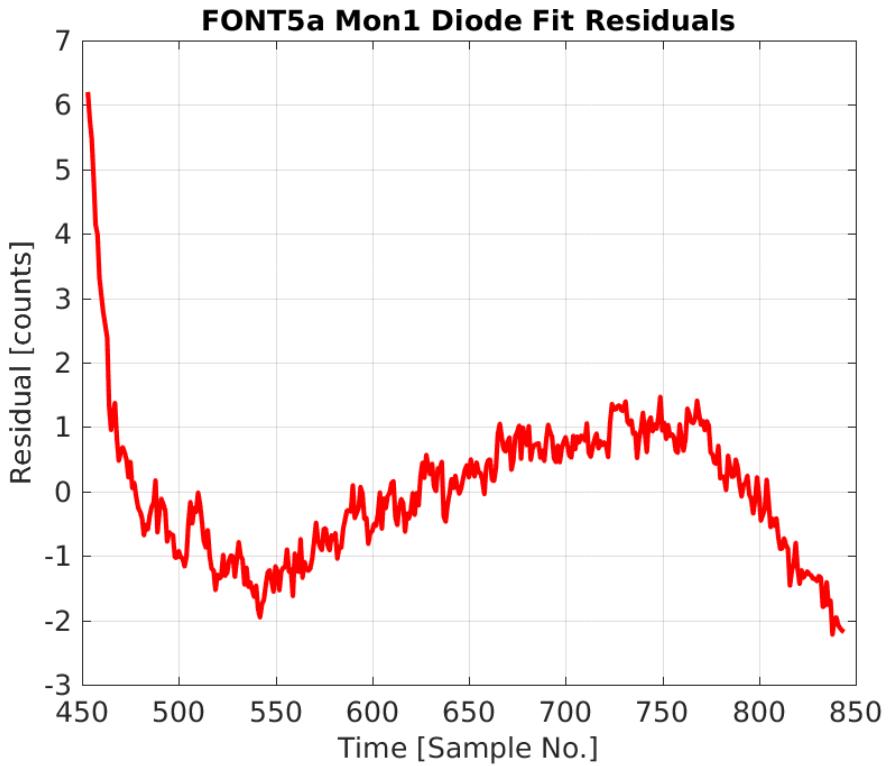


Figure 2.7: Residuals between diode exponential fit and actual diode output.

output based on the known decay constants, so that:

$$y(t) = x(t) + \frac{1}{\tau} \sum_{i=1}^t x(i-1) \quad (2.1)$$

Where $y(t)$ is the filtered ADC output at sample t , $x(t)$ is the original unfiltered output at sample t , and τ is the decay time constant. Rather than being hard-coded in the firmware the applied decay constant in the filter for each ADC is calculated using an 8-bit ± 64 filter weight, which can be changed in the DAQ, which is then divided by a common division factor to get the real applied value of $1/\tau$ [REF]. The optimal filter weights for each ADC in the FONT5a board currently used for PFF operation are shown in Table 2.1, these can be converted in to the true decay constant values using the fitted values for ADC1 and ADC2 quoted above.

With the IIR filters enabled on the FONT5a board the droop on the diode (ADC1) is almost perfectly removed as shown in Figures 2.5 and 2.8, although in the zoomed in figure some slight deviation from flat is visible due to the residuals around the exponential fit seen previously. The effect on the reconstructed phase using only the mixer (ADC2) is shown in Figure 2.9, with a modest adjustment to the overall shape that is most visible at the start and end of the pulse.

ADC	Filter Weight
1 (Mon1 Diode)	50
2 (Mon1 Mixer)	56
3	50
4	53
5	45
6	51
7	48
8	55
9	49

Table 2.1: IIR filter weights for the FONT5a board ADCs.

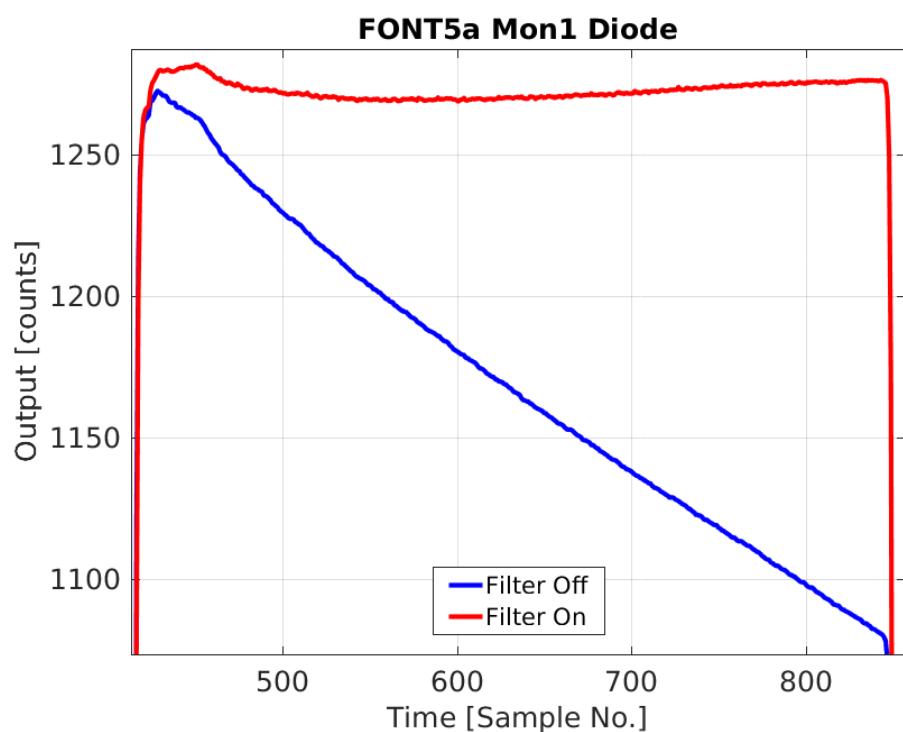


Figure 2.8: Diode output along the pulse with the IIR filter off and on. Zoomed in.

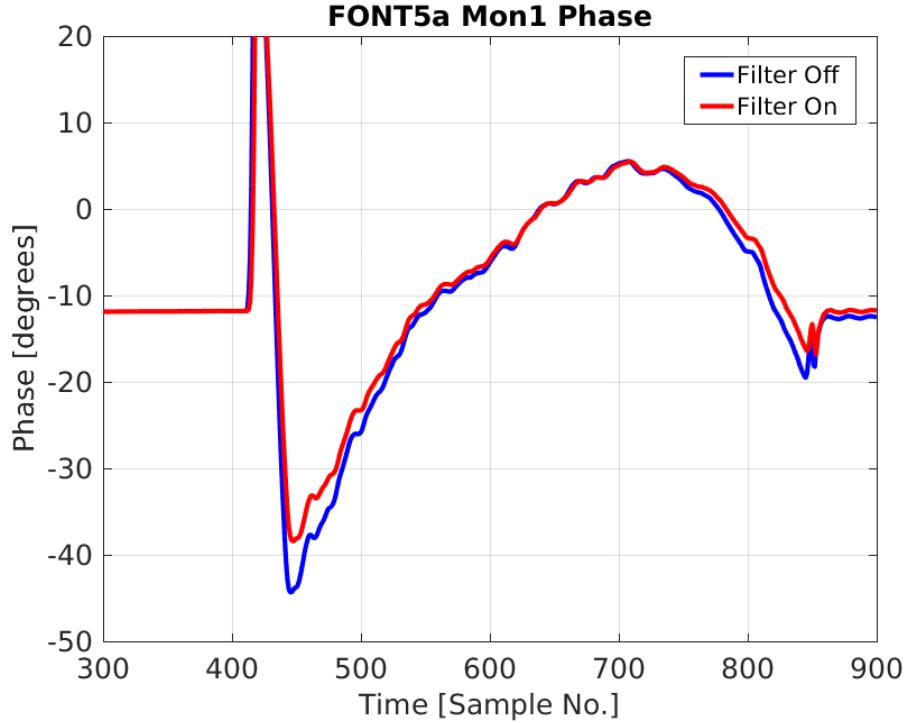


Figure 2.9: Phase along the pulse with the IIR filter off and on.

2.1.3 Gain Calculation

As shown in Section ?? the effect of the PFF system can be modelled by simply subtracting the measured upstream phase, ϕ_u , from the downstream phase, ϕ_d with a gain factor, g :

$$\phi_{PFF} = \phi_d - g\phi_u \quad (2.2)$$

Where ϕ_{PFF} is the corrected downstream phase. The gain set in the FONT5a DAQ is not directly a multiplication factor in terms of the phase, but rather a multiplication in terms of DAC counts and other constants. How the set FONT gain relates to the true gain g is derived in this section.

In the case where diode normalisation is not used, which is the nominal setup, the FONT5a DAC outputs when the PFF system is enabled are given by:

$$\begin{aligned} \text{DAC1} &= \frac{F1}{64} \text{ADC2} \\ \text{DAC2} &= \frac{F2}{64} \text{ADC2} \end{aligned} \quad (2.3)$$

Where DAC1 and DAC2 are the two DAC outputs, in DAC counts, F1 and F2 are the respective gains for each DAC output set in the DAQ, and ADC2 is the Mon1 mixer signal level in ADC counts, which is connected to ADC2 for normal PFF operation. The whole calculation uses 16-bit architecture, with the 3 sub-integer bits discarded when sent to the 13-bit DACs [REF]. The FONT gains F1 and F2 are 14-bit (± 8192) and the common division factor of 1/64 is set by several parameters fixed in the FONT5a firmware in order to give a sensible range of gain values based on the approximate signal levels [REF]. Typically

$F_2 = -F_1$, so that the beam is deflected in opposite directions in each kicker to achieve orbit closure in the chicane. With a maximum FONT gain of 8192 an ADC2 input of 1 ADC count gives an output of 128 DAC counts. If diode normalisation is enabled the expressions above are multiplied by $1/\sqrt{\text{ADC}1}$ (with the Mon1 diode signal connected to ADC1 in normal operation) and different scale factors are used [REF].

To determine the optimal values for F_1 and F_2 given the current beam conditions it is important to know how they translate in to the real applied gain g from Equation 2.2. The real gain g is related to the DAC outputs derived above by:

$$g\phi_u = k\text{DAC} \quad (2.4)$$

Where k is the phase shift, in radians, in the chicane resulting from a DAC output of 1 count. The indices 1 and 2 are dropped from DAC1, DAC2, F_1 and F_2 from this point for simplicity. The upstream phase, also in radians, can then be related to the ADC2 input by:

$$\phi_u \simeq \frac{\text{ADC}2}{A} \quad (2.5)$$

Where A is the calibrated maximum Mon1 mixer amplitude, in ADC counts, determined in the same way as Section 1.7. Note that both this and the direct proportionality with ADC2 in Equations 2.3 assume the small angle approximation $\text{ADC}2 = A \sin \phi_u \simeq A\phi_u$ for small ϕ_u . This is done for latency reasons [REF] and its effect on the accuracy of the applied correction is discussed in the next section.

Combining Equations 2.3, 2.4 and 2.5 gives:

$$\begin{aligned} \frac{g}{A}\text{ADC}2 &= \frac{kF}{64}\text{ADC}2 \\ g &= \frac{kA}{64}F \end{aligned} \quad (2.6)$$

In Section 2.4.1 a phase shift of 3.5° per volt sent to the amplifier is determined. Knowing that 4096 DAC counts corresponds to 2 V sent to the amplifier this value can be converted into $k = 29.8 \mu\text{radians}/\text{DAC count}$. Typical calibrations for Mon1 on the FONT5a board give $A \simeq 3440$ ADC counts (Section 1.7.2). Overall, the real applied gain therefore relates to the set FONT gain in the DAQ via:

$$g \simeq \frac{F}{624} \quad (2.7)$$

The optimal real gain to apply (Section ??) is given by the upstream-downstream phase correlation, ρ , multiplied by downstream-upstream jitter ratio, σ_d/σ_u :

$$g_{\text{opt}} = \frac{\sigma_d}{\sigma_u}\rho \quad (2.8)$$

Therefore the optimal FONT gain to set in the DAQ dependent on the current beam conditions is:

$$F_{\text{opt}} \simeq 624 \frac{\sigma_d}{\sigma_u}\rho \quad (2.9)$$

In good conditions the correlation and jitter ratio are close to one, although the downstream phase jitter can be up to a factor two larger than the upstream jitter at CTF3 thus the applied FONT gains are typically in the range between 625 and 1250.

2.1.4 Effect of Using Small Angle Approximation

As mentioned previously the phase calculation in the PFF algorithm in the FONT5a firmware uses the small-angle approximation, thus differs from the correct full phase reconstruction method used in Chapter 1 as follows:

$$\phi_{\text{FONT}} = \frac{\text{Mixer}}{A} \quad (2.10)$$

$$\phi_{\text{FULL}} = \arcsin\left(\frac{\text{Mixer} - d}{A}\right) \quad (2.11)$$

Where ϕ_{FONT} and ϕ_{FULL} are the upstream phase with the FONT and full phase reconstruction methods respectively, Mixer is the Mon1 mixer signal, A is the Mon1 calibration amplitude and d is the calibration offset needed to take in to account asymmetry in the mixer minimum and maximum output due to cross-talk from the diode (Section ??).

The difference between the measured phase using these two reconstruction methods is plotted in Figure 2.10, versus the phase offset between the beam phase and the electronics LO phase. For small incoming phases (close to zero Mixer output) the only difference between the two methods is a static offset of $-d/A$ in the measured phase, and this holds up to $\pm 10^\circ$ (and is a good approximation up to $\pm 20^\circ$). In this case the corrected downstream phase will contain this constant offset, but the corrected phase jitter, which has been the only focus of the PFF prototype to date, will still be optimal.

With larger offsets between the beam phase and the LO (large Mixer output) the small angle approximation is no longer valid and the difference between the two methods rises to up to 35° . Most importantly the measured phase, and therefore the correction output, is no longer linearly dependent on the incoming beam phase when there is a large offset between the beam and LO phases. In the most extreme case, the measured phase difference between two pulses with a beam-LO phase offset of 80° and 90° would only be 1° with the FONT algorithm instead of the expected 10° , for example. In turn, the difference in the correction applied to the two pulses would only be 1° instead of 10° , degrading the achievable corrected phase jitter.

[TODO: Change legend labels to FONT and FULL, rather than FONT and SiS. And beam-LO rather than Beam-Shifter phase offset]

Figure 2.11 shows a simulation of the theoretical downstream jitter that can be achieved with both phase reconstruction methods with 0.8° initial upstream and downstream phase jitter and an upstream-downstream phase correlation of 97%. These values are chosen to represent the beam conditions that will need to be achieved in order to demonstrate 0.2° phase stability at CTF3. In the $\pm 10^\circ$ region where the small approximation holds there is no degradation in the achievable corrected phase jitter using the simplified method in the PFF algorithm. Outside this region the jitter is degraded, increasing from below 0.2° to 0.3° for a beam-LO phase offset of 50° .

As the correction range of the PFF system is less than $\pm 10^\circ$ (Section 2.4.1) there should be no degradation in the PFF performance resulting from the use of the small angle approximation in the PFF algorithm, providing the LO phase shifter in the phase monitor electronics

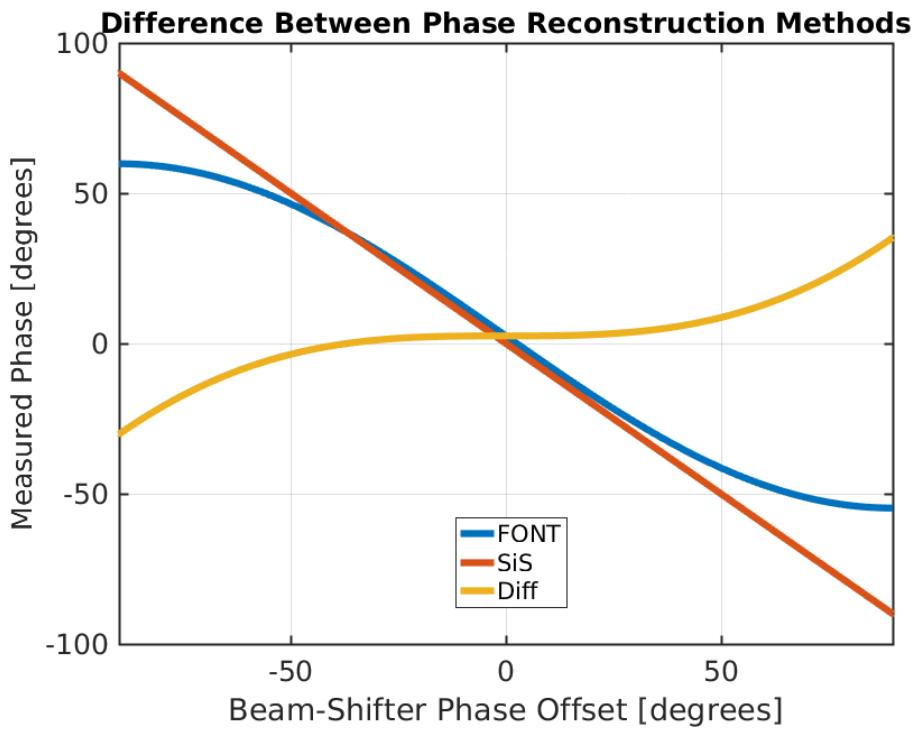


Figure 2.10: Difference between the phase reconstruction method used in the PFF algorithm on the FONT5a board (with the small angle approximation) and the full reconstruction used with data acquired from the SiS digitisers.

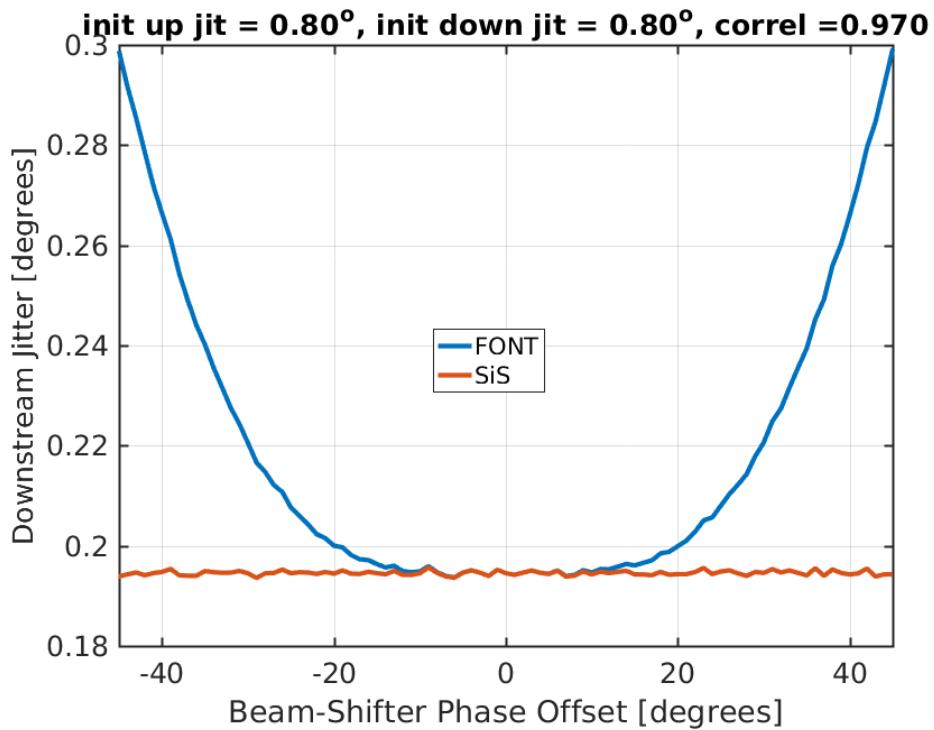


Figure 2.11: Achievable PFF jitter versus phase offset for full phase reconstruction and with the small angle approximation.

has been set correctly. This highlights the importance to adjust the phase shifters to zero the Mixer output not only in order to maximise the phase monitor resolution (Section ??) but also to ensure the correction calculation itself is valid. However, it is perhaps interesting to note that it would not be possible to correct the full CTF3 pulse length to 0.2° jitter with this implementation of the PFF algorithm even if the correction range were large enough to encompass the 40° phase sag.

2.2 Amplifier

The amplifier takes the two DAC signals from the FONT5a board and produces four high voltage outputs from them that are connected to the downstream ends of the kicker strips (two kickers and two strips per kicker gives four connections at the downstream ends in total), creating the potential difference between the kicker strips that deflects the beam in order to correct the phase. The returning signals from the upstream ends of the kicker strips are then terminated back at the amplifier. As the amplifier is installed together with the phase monitor electronics and FONT5a board in the klystron gallery the cables between the amplifier and kickers are long and represent the single largest contribution to the overall system latency, as discussed in Section 2.5.1. This section discusses the design and performance aspects of the amplifier that are relevant to PFF operation.

2.2.1 Design

The amplifier is purpose built for the PFF prototype, also by the FONT group at Oxford University, with further details of its design available in [REF]. An annotated picture of its front panel is shown in Figure 2.12 and a simplified diagram showing the flow of signals between the FONT5a board, amplifier and kickers is shown in Figure 2.13. The amplifier is installed in a standard 3U rack and has a modular design. It consists of five individual modules split between two sides, labelled left and right. The left side of the amplifier, which uses the DAC 1 output, powers the first kicker in the chicane, and the right side of the amplifier, which uses the DAC 2 output, powers the second kicker. Each side of the amplifier contains its own “drive module” and “terminator module”. Finally there is a central “control module” that is common to both sides of the amplifier.

All the outputs from the FONT5a board are connected to the control module, this includes the DAC 1 and DAC 2 outputs as well as the trigger for the amplifier. The required 24 V, 1.1 A power supply is also connected to the control module. The control module then deals with the distribution of power, timing and input signals (derived from the DAC inputs) to the two drive modules. The control panel can therefore include signal processing designed to protect the drive modules. It ensures the maximum signal level sent to the drive modules is at a safe level and limits the rate of large changes in the input drive signal (limits the slew-rate), as well as preventing triggering of the drive modules if a problem is detected, for example.

The amplification of the signals to create the high voltage outputs occurs in the drive

modules. Each drive module takes one input signal but creates two high voltage outputs (A and B) which have equal magnitude but opposite polarity. These are connected to the downstream end of the left and right strips of one of the kickers, to create a potential difference across the kicker strips that is double the voltage of each individual drive module output. The signal amplification consists of low voltage Si FETs (Directed Energy Inc DE150-201N09A [REF]) driving high voltage SiC FETs (Cree C2M01600120D [REF]) and a final output transformer, giving a peak output of around ± 700 V (seen in more detail in Section 2.2.2). The output has a bandwidth of 47 MHz for small signal variations up to 20% of maximum output (around 140 V). The bandwidth for larger variations is slew rate limited, and around 25 MHz for variations up to 50% of the maximum output, for example [REF].

Each drive module requires a ramp up time of $1\ \mu\text{s}$, which defines when the trigger must arrive from the FONT5a board. After this period the drive modules are powered for $1.6\ \mu\text{s}$ with full output across $1.3\ \mu\text{s}$ (slightly longer than needed to correct the full $1.1\ \mu\text{s}$ CTF3 beam pulse length). The control module includes a monitoring output (labelled “ON”) that can be digitised to observe the time period within which the drive modules are on and ready to receive input.

The high voltage signals leaving the upstream ends of the kicker strips are terminated back at the amplifier on the terminator modules. Each module consists of two $50\ \omega$ terminators designed to be able to take the maximum 20 kW output from the drive modules [REF]. Each terminator has a monitoring signal, which gives output at around -40 dB or approximately 1/115 of the input voltage [REF]. These can be used to verify the applied output from the drive modules is as expected, and form the basis of most of the measurements in the remainder of this section as well as the timing checks in Section 2.5.2, for example.

The description of the amplifier here represents the version of the amplifier that was used for the latest PFF tests, and for almost all results in this thesis. A first version of the amplifier, with around half the output voltage at up to ± 350 V was used for early PFF tests. Additional FETs were added in the second version described above to boost the output voltage to ± 700 V. A third version of the amplifier was foreseen but ultimately deemed unnecessary for the application at CTF3. This would have provided a voltage of up to ± 1400 V by combining the output of four individual drive modules [REF].

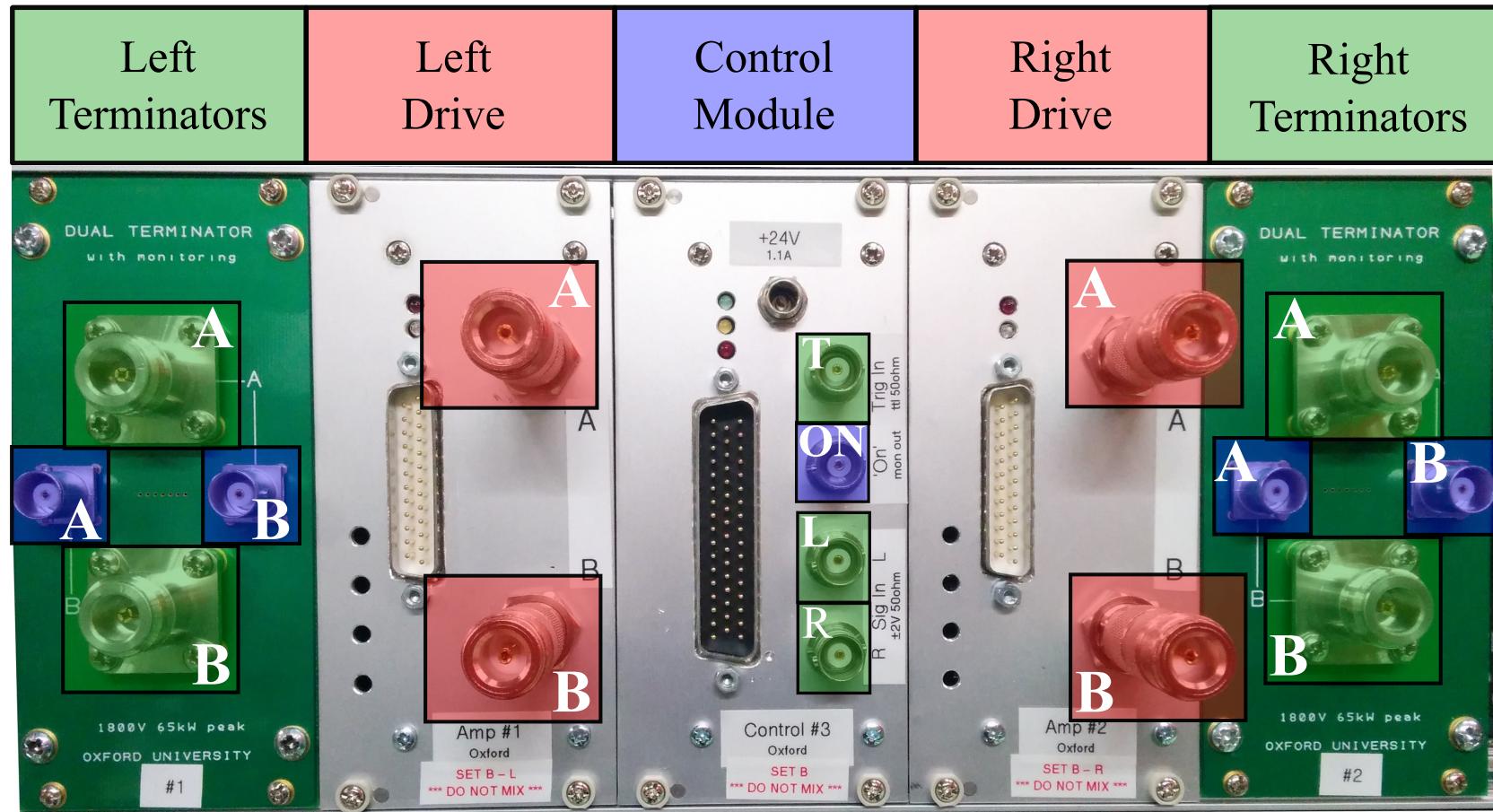


Figure 2.12: Front panel of the amplifier. Inputs to the amplifier are highlighted in green, drive outputs in red and monitoring outputs in blue. Inputs to the control module are the trigger (T) and the two DAC outputs from the FONT5a board used to determine the drive to the left (L) and right (R) sides. Each side of the amplifier has two pairs of drive outputs and terminators, A and B. The signal returning to each of the terminators can be observed on their corresponding monitoring outputs. The monitoring output on the control module (ON) shows the $1.4 \mu\text{s}$ time during which the amplifiers are able to provide their output. Not highlighted in the figure are the 24 V, 1.1 A power connector at the top of the control module, and also the three [TODO: what type?] connectors used to communicate between the control module and drive modules.

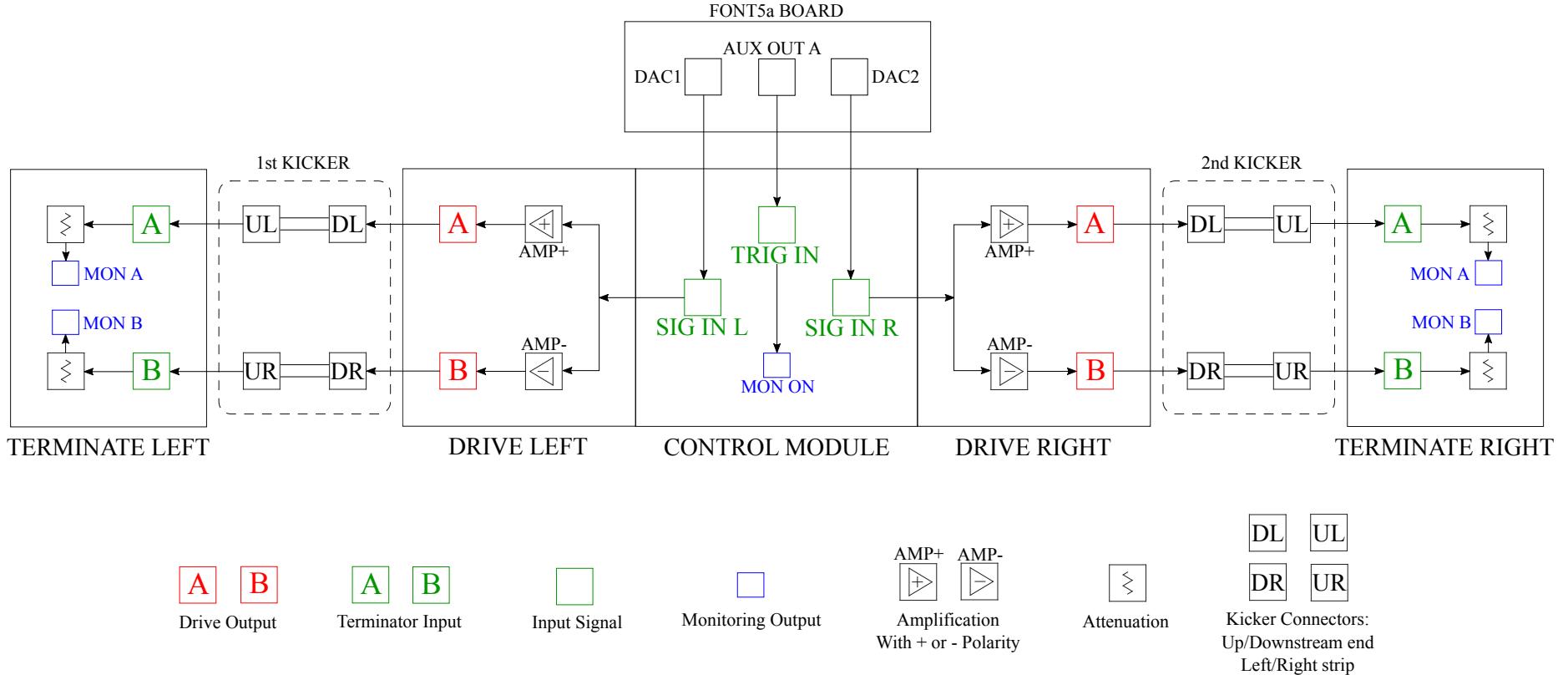


Figure 2.13: Simplified flow diagram showing the connections between the FONT5a board, the amplifier and the kickers. The kickers are inserted between the drive and terminator modules for the purposes of the diagram, but in reality the terminator modules neighbour the drive modules in the same unit as seen in Figure 2.12. Note that the A and B outputs on each side always have opposite polarity, as needed to create a large potential difference between the kicker strips.

2.2.2 Linearity

Figure 2.14 shows the amplifier output, as measured by the monitoring signals, at different constant input voltages sent from the FONT5a board between the minimum of -2V (-4096 DAC counts) and maximum of 2V (+4096 DAC counts). The output voltage from the monitoring signals is converted in to the real amplifier output Voltage using the approximate conversion factor of 115. All four amplifier outputs are shown (one for each strip of the two kickers). The plotted values are means taken across a 480 ns central part of the whole 1400 ns output pulse.

The relative polarity of the four outputs is equivalent to what would be sent to the kickers during PFF operation, with opposite polarity of the L and R amplifier outputs sent to each kicker, so that the beam is kicked in opposite directions by each kicker with the second kicker then closing the orbit bump created by the first. Within each side of the amplifier the A and B outputs (sent to each side of the kicker) also have opposite polarity, necessary to create the potential difference across the strips within each kicker that creates the deflecting field for the beam. The relative polarity of the A and B outputs is fixed in the amplifier design and cannot be controlled via the FONT5a board.

The response of the amplifier is highly linear in the region between ± 1.2 V sent to the amplifier. Outside this range the amplifier clearly begins to enter saturation, in particular above input voltages of ± 1.7 V. The linear fits shown include only the points between ± 1.2 V, excluding the first and last three points in the scan of input voltages, in order to not be biased by the effects of saturation.

Figure 2.15 shows the residuals between the linear fit and the real amplifier output across the full range of input voltages. By looking at the residuals a slight deviation from linearity in the ± 1.2 V range is also visible, although the maximum difference is only 10 V or a 3% relative error. At the maximum input voltage of ± 2 V the difference between the real output and the amplitude expected if the response was linear across the full range rises above 150 V, or a relative error of more than 25%. For example, the RB output at an input voltage of +2 V is 605 V but the fitted response gives 769 V, a difference of 164 V or 27%.

The effects of amplifier saturation are not taken in to account in the PFF algorithm on the FONT5a board, in which the DAC output is linearly dependent on the input phase (voltage from the phase monitor mixer signal) across the full range. The applied correction to the downstream phase will therefore be non-optimal when the DAC output calculated by the PFF algorithm is above an absolute value of 2500 counts (1.2 V sent to the amplifier). To date the non-linearity of the amplifier as it begins to enter saturation has also not been included in the PFF simulations presented in the following chapters. This may partially explain the small discrepancies seen between the simulated and real results in some datasets, so including the effect will be pursued in the future. In addition, it could be foreseen to incorporate the saturation characteristics in to the PFF algorithm on the FONT5a board, so that calculated outputs above 2500 counts are boosted slightly to compensate for the lower than expected amplifier output.

Discrepancies between the four amplifier outputs are also visible in Figure 2.15 and Ta-

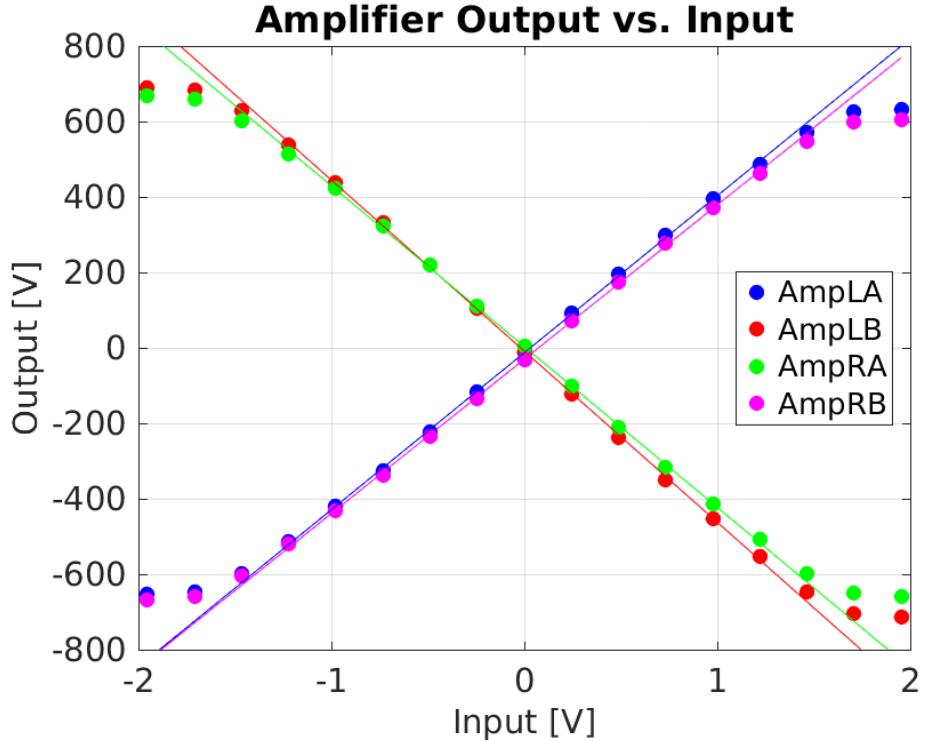


Figure 2.14: Amplifier output vs. input.

ble 2.2, both in terms of gradient and peak output. This can be partially but not completely explained by errors of up to a few percent in the precise calibration of the four monitoring outputs, which do not output exactly 1/115 of the real input voltage [TODO: Ask Colin about errors]. Differences between the A and B outputs sent to each kicker are not an issue for the PFF performance as both are linear (in the ± 1.2 V range) and the kick experienced by the beam in each kicker is proportional to the difference of the two. Therefore, only the calibration between the output from the FONT5a board sent to the amplifier and the resulting phase shift in the TL2 chicane is affected. However, disparity between the potential difference across each kicker (LA-LB and RA-RB), so that the deflection of the beam in each kicker is different, leads to the orbit bump created by the PFF system not being closed in the chicane, degrading the horizontal beam stability downstream. The fitted potential difference at 1 V input is 869 V for the left amplifier (LA-LB, sent to the first kicker) and 835 V for the right amplifier (RA-RB, sent to the second kicker), a difference of 4%. This can be compensated in the PFF setup on the FONT5a board by using a different gain for each correction output, so that the voltage sent to the right amplifier is higher but the resulting output voltage sent to both kickers is the same. Orbit closure is discussed further in Section 2.4.4.

2.2.3 Shape

In the previous section the linearity of the mean output was considered but the performance of the PFF correction is clearly also sensitive to any variations in output voltage along the amplifier output pulse. Figures 2.16 and 2.17 show the full 1.4 μ s amplifier output pulse

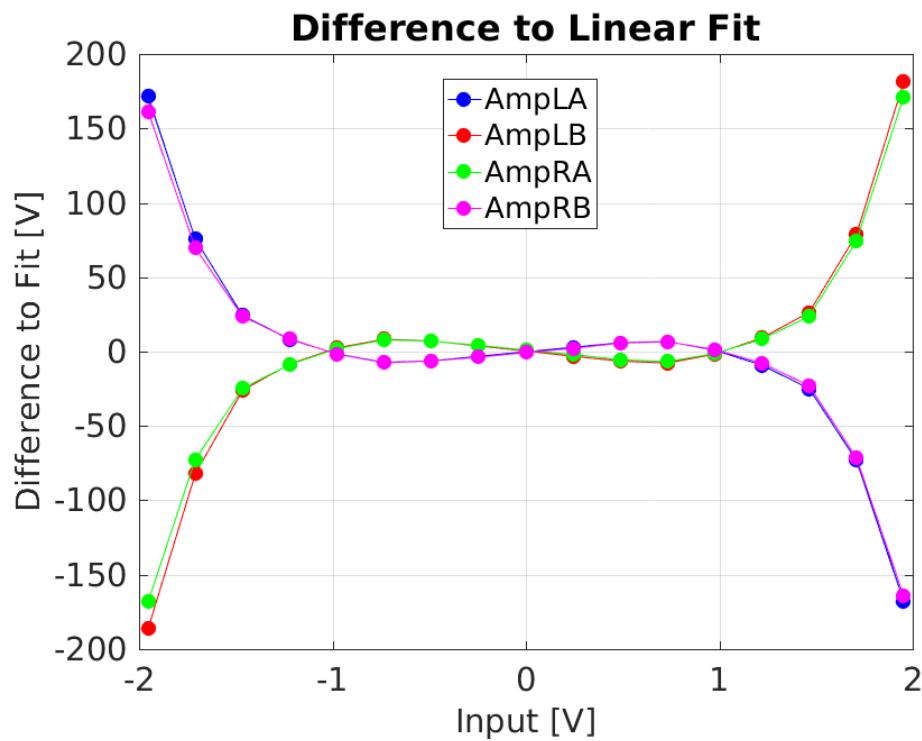


Figure 2.15: Residual between amplifier output and linear fit.

Amplifier Port	Output at +1 V Input
LA	+416 ± 3 V
LB	-453 ± 3 V
RA	-426 ± 3 V
RB	+409 ± 3 V

Table 2.2: Feedforward results using combined data from 20th November 2015.

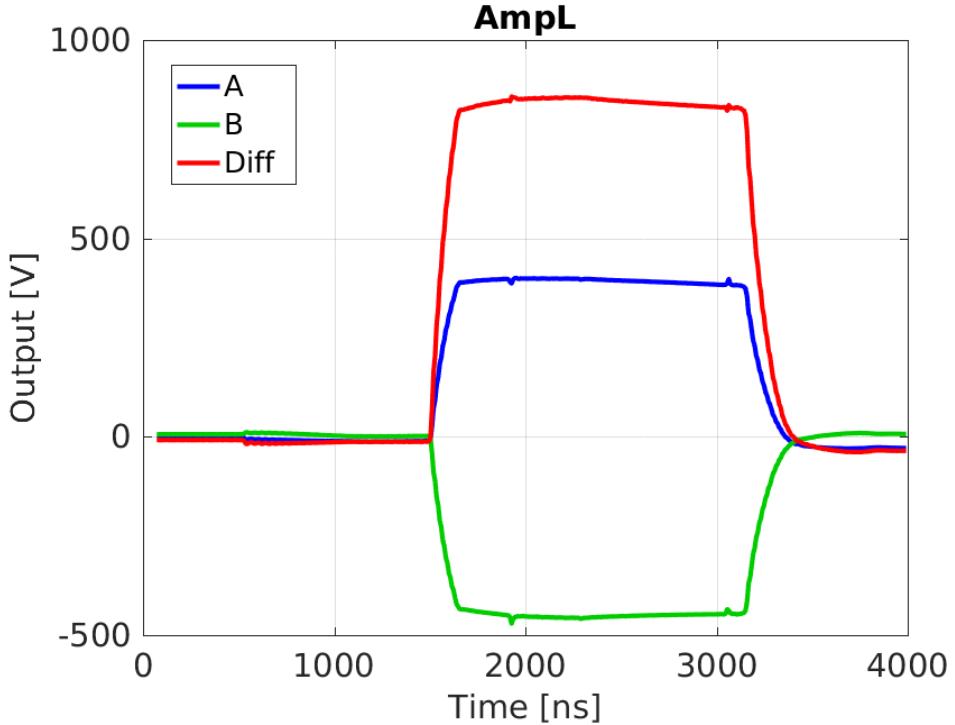


Figure 2.16: Amp L along pulse at 1 V input

at a constant +1 V input sent to the left amplifier and a constant -1 V input sent to the right amplifier respectively. Spikes in the signal just prior to 2000 ns and after 3000 ns on the time axis as seen in the plots are beam pickup induced by the beam passing through the kickers. These are therefore not a property of the amplifier performance and are excluded from the analysis in this section. However, the beam pickup is used later in Section 2.5.2 for the purposes of optimising the correction timing.

For each side of the amplifier both the A and B outputs are plotted as well as the difference of the two, which is the relevant quantity in terms of the kick received by the beam as it traverses the kickers. In the ideal case the potential difference should be flat along the full pulse length. However, for both the left and right side variations in the difference are visible, with an initial increase in output across the first 500 ns of the pulse followed by a droop in response across the second half of the pulse. Although not shown here, the shape of the variations along the pulse is consistent across the full range of output voltages, and scale in magnitude with the output voltage. Figure 2.18 shows the peak-to-peak and mean deviation of the output voltage along the pulse across the full range of input voltages. The peak-to-peak deviation refers to the difference between the minimum and maximum output along the pulse, whilst the mean deviation is the average absolute difference between the mean output and the output at each sample point. For a constant input voltage the output voltage along the pulse varies by up to 88 V peak-to-peak (mean 12 V) for the left amplifier or 93 V peak-to-peak (mean 14 V) for the right amplifier. As a relative difference, this corresponds to approximately a 6 % peak-to-peak, or 1 % mean, variation along the pulse.

The PFF algorithm on the FONT5a board uses a single gain value across the whole pulse length for each correction output, thus making the approximation that the amplifier

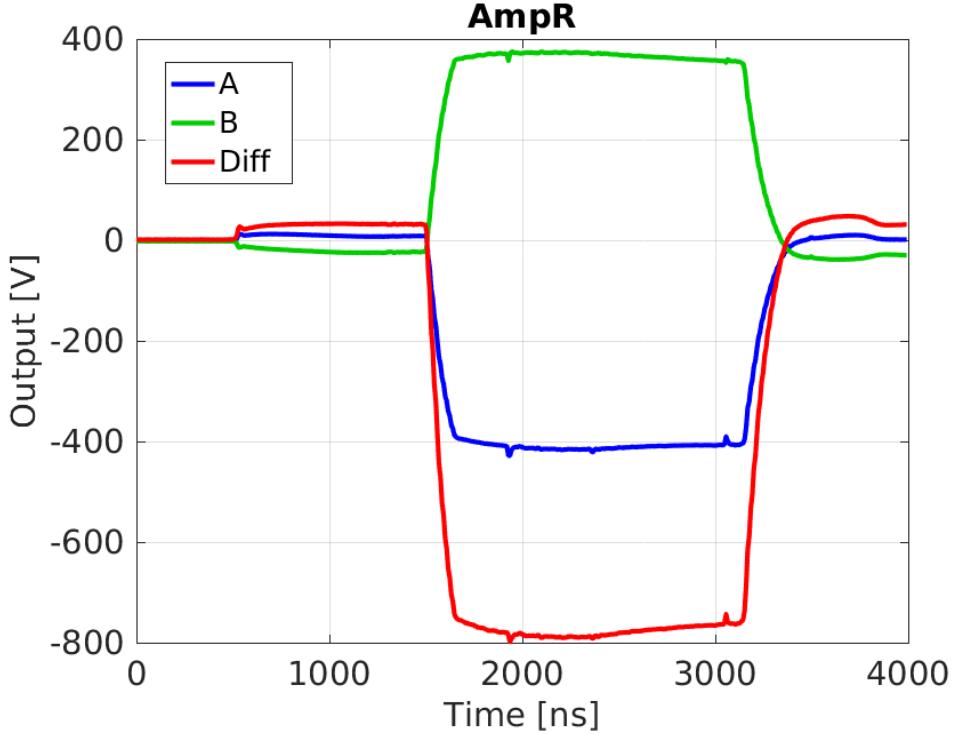


Figure 2.17: Amp R along pulse at 1 V input

response is flat along the pulse. The variations along the amplifier pulse therefore directly translate in to discrepancies between the intended phase shift as calculated and the real phase shift experienced by the beam. As the region of interest for the correction is a few hundred nanoseconds about the central part of the pulse, as opposed to the full pulse length, the 1 % mean variation is more indicative of the resulting error than the 6 % peak-to-peak variation. With a correction range (Section 2.4.1) of $\pm 6^\circ$, the effects of the non-flat amplifier output should be below 0.06° and not measurable considering the phase monitor resolution of 0.14° . Nevertheless, it could be foreseen to implement a droop correction in the PFF algorithm on the FONT5a board, taking the variations in the amplifier output along the pulse in to account.

As for the mean output voltage, the second way variations in the amplifier output along the pulse can impact the PFF performance is via the orbit closure in the chicane. For this the relevant quantity is the sum of the potential difference sent to each kicker, or $(LA - LB) + (RA - RB)$. To ensure orbit closure this quantity, named the residual kick here, should be zero across the whole pulse length for all input voltages. Figure 2.19 shows the residual kick along the pulse for all the input voltages in the scan. Clearly they are not all centred around zero, but this is expected due to the differences in the mean output voltage of the four amplifier outputs seen in the previous section. As already stated, the overall mean offset can be removed by using a different gain for the two correction outputs. However, any variations along the pulse cannot be compensated for in the PFF algorithm. The magnitude of the effect is summarised in Figure 2.20, showing the peak-to-peak and average deviation of the residual kick from flat. The overall residual kick is very flat and effect is smaller than any of those previously shown — only up to 2 V on the mean or 21 V

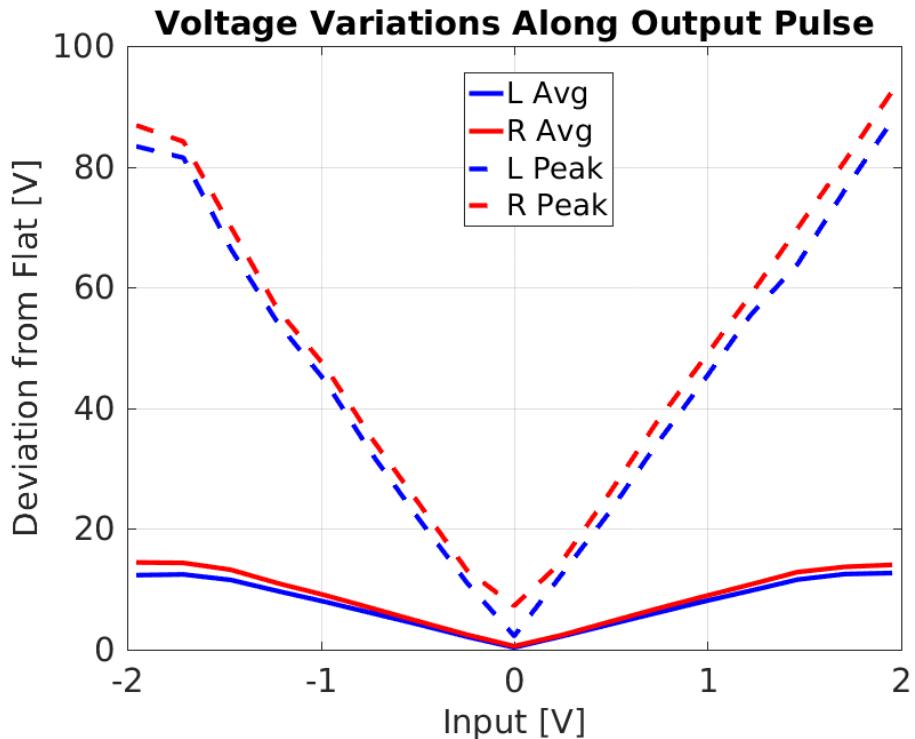


Figure 2.18: Flatness of potential difference sent to kickers.

peak-to-peak. Whether this has any measurable effect on the orbit closure is discussed in Section 2.4.4.

2.3 Data Acquisition and Signal Processing

2.3.1 SiS Digitiser Setup

(already discussed in ph mon chapter)

2.3.2 Acquisition Tools

2.3.3 Monitoring Tools

Online display

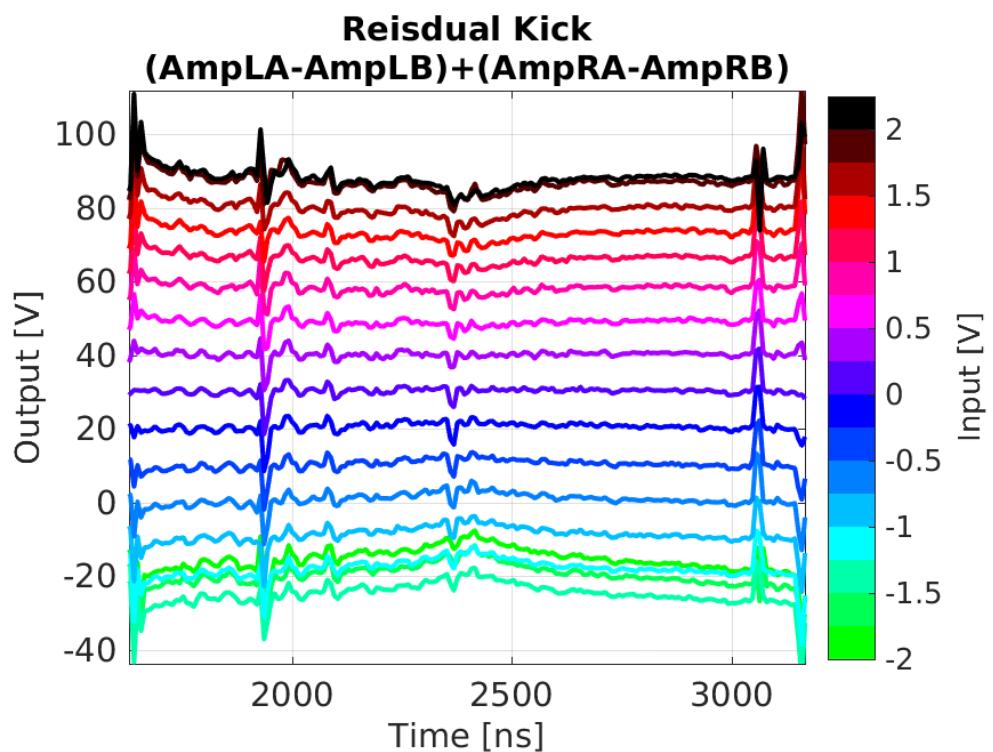


Figure 2.19: Residual kick along pulse.

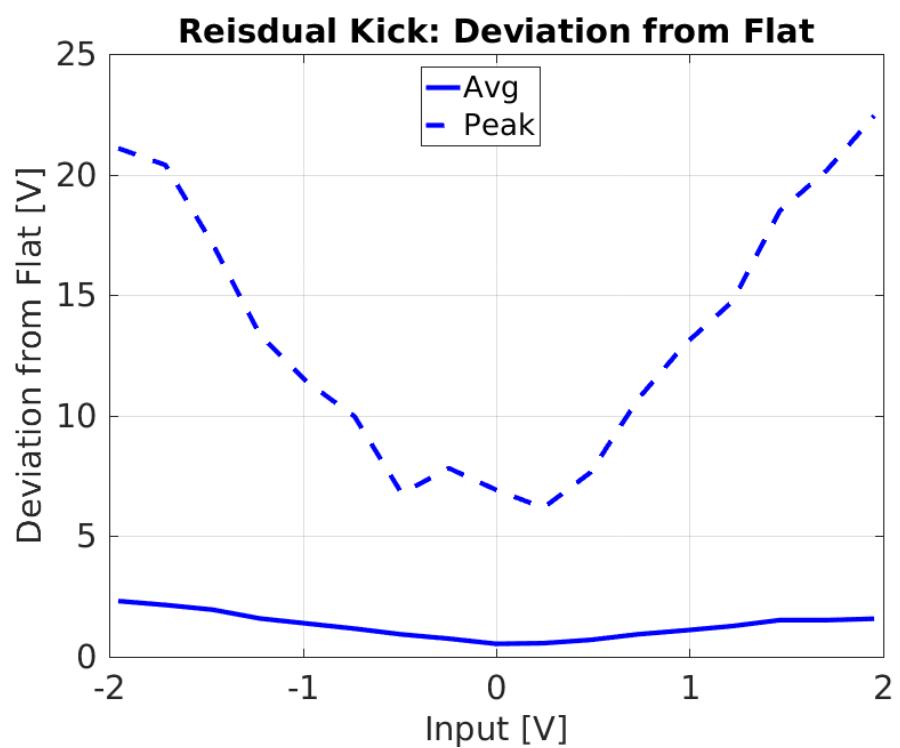


Figure 2.20: Residual kick along pulse: deviation from flat.

	Phase Shift at +1 V Input	Max Phase Shift
Data	$3.5 \pm 0.1^\circ$	$5.5 \pm 0.3^\circ$
Model	3.6°	5.6°

Table 2.3: Phase shift at +1 volt input to the amplifier.

2.3.4 Time Alignment of Signals

2.3.5 Definition of Zero Phase

2.4 Kicker and Optics Performance Verification

2.4.1 Correction Range

Knowledge of the correction range of the PFF system, or more specifically the relationship between the voltage sent to the amplifier and the phase shift in the chicane, is critical for the PFF setup. The first checks of the ability to shift the phase in the TL2 chicane using the new phase feedforward optics were performed with magnetic correctors prior to the PFF amplifier being available (these correctors can be used to implement a secondary “Slow Correction” to complement the PFF system, as discussed in Section ??). Aside from their use for the PFF correction, these tests and the clear variation with beam phase versus voltage sent to the PFF kickers shown in this section are already a significant achievement and a verification of the extensive work to improve the MADX model of TL2 presented in Chapter ??.

Figure 2.21 shows the mean phase shift after the chicane (in the downstream phase monitor) across the full ± 2 V input range of the amplifier. Constant DAC outputs from the FONT5a board were sent to the amplifier in 17 steps between -4096 counts (-2 V) and +4096 counts (+2 V). In order to reduce the sensitivity to any drifts in the beam phase between data points the scan was taken in interleaved mode, alternating between pulses with no drive sent to the amplifier and a constant non-zero DAC output. The phase plotted in Figure 2.21 is therefore the difference between 50 kicked beam pulses and 50 “nominal” pulses taken at the same time for each amplifier input voltage.

At the maximum amplifier input voltage of 2 V the phase after the chicane is shifted by $5.5 \pm 0.3^\circ$. The fitted phase shift per Volt sent to the amplifier is $3.5 \pm 0.1^\circ$ in the ± 1.2 V linear range of the amplifier (excluding the first and last three points, blue “FIT” line in Figure 2.21). This fitted gradient is required and was previously introduced for the conversion between the PFF gain in the units on the FONT5a board and the real applied gain in Section 2.1.1. In Section 2.1.1 it was quoted in terms of the phase shift in radians per DAC count output from the FONT5a board, rather than degrees per Volt as shown here. The value of $30\mu\text{rad}/\text{count}$ is easily derived using the conversion factors between degrees and radians and knowing that a DAC output of 4096 counts corresponds to 2 V sent to the amplifier. [TODO: Calculated factor is 29.827 microradians/count here. One I actually used for gain conversion, simulations etc. was 26.18 (used full range rather than linear range)]

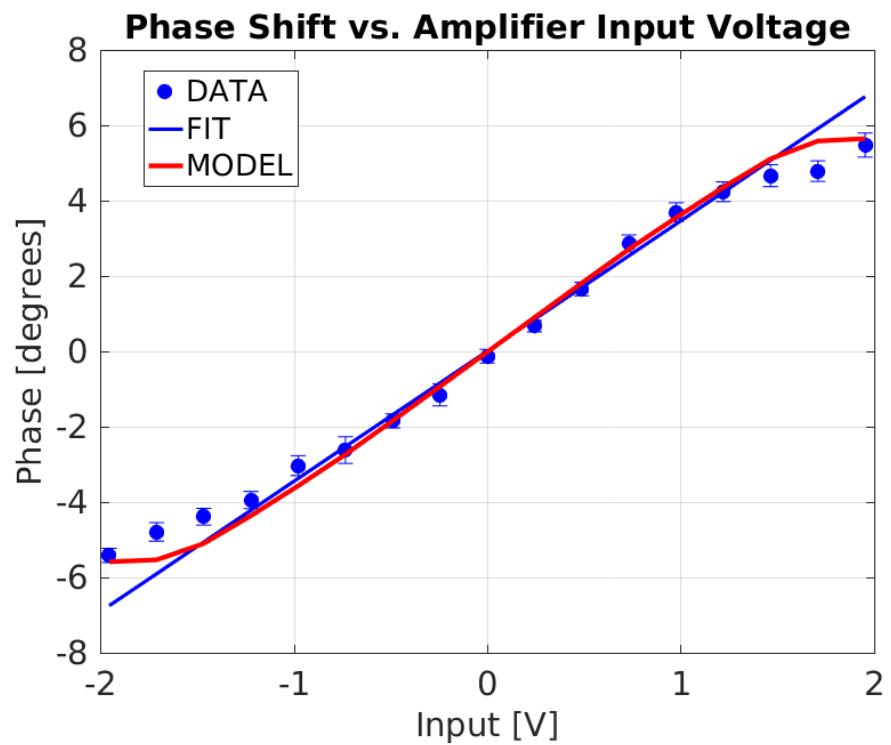


Figure 2.21: Phase shift versus amplifier input voltage.

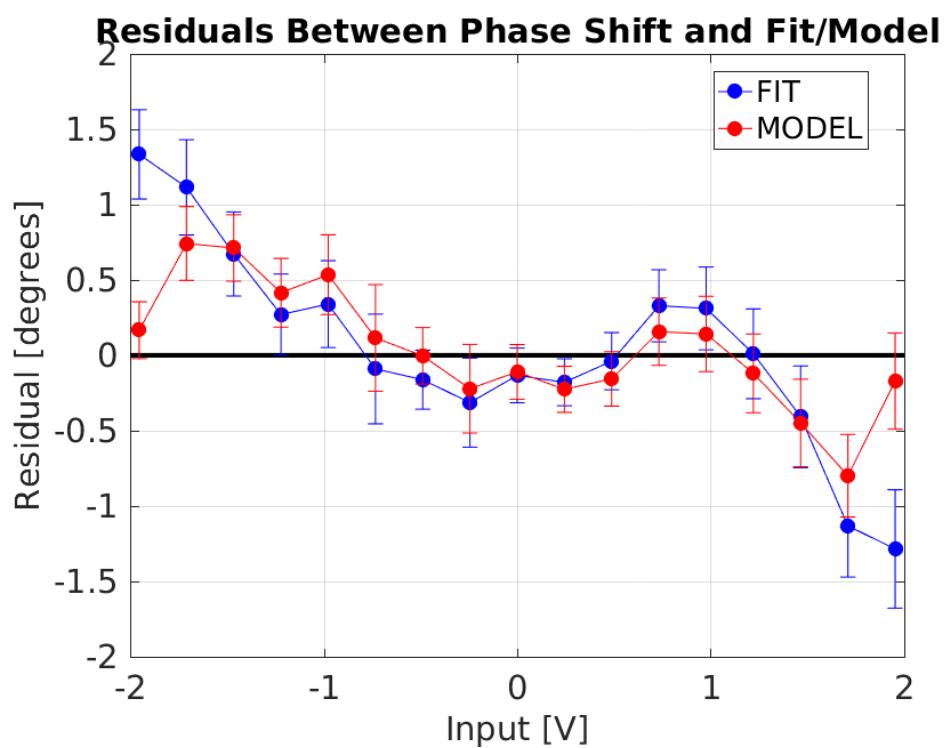


Figure 2.22: Phase shift versus amplifier input voltage.

Given knowledge of the amplifier output characteristics (Section 2.2.2), the kicker specifications (Section ??) and the chicane optics (Section ??) the real phase shift seen in the scan can be compared to the expected phase shift based on the system parameters. The predicted phase shift, $\Delta\phi$, in degrees is given by:

$$\Delta\phi = V_{amp}[V_{font}] \cdot K \cdot R_{52} \cdot \frac{360}{\lambda_{12\text{GHz}}} \quad (2.12)$$

Where $V_{amp}[V_{font}]$ is the amplifier output Voltage at an input voltage of V_{font} sent from the FONT5a board, K is the angular deflection of the beam per Volt applied to each kicker strip, R_{52} is the R_{52} value between the kickers in the PFF optics and $\frac{360}{\lambda_{12\text{GHz}}}$ converts the calculated orbit length difference in to an equivalent 12 GHz phase using the 12 GHz wavelength $\lambda_{12\text{GHz}}$. The value of most of these parameters has already been derived in the sections previously mentioned. They are:

$$\begin{aligned} V_{amp}[1 \text{ V}] &= 435 \text{ V} \\ K &= 0.8 \text{ } \mu\text{rad/V} \\ R_{52} &= -0.7 \text{ m} \\ \lambda_{12\text{GHz}} &= 2.5 \text{ cm} \end{aligned}$$

The value of $V_{amp}[1 \text{ V}]$ is given as a representative value in the linear range of the amplifier but the real amplifier output at all input voltages is used in the predictions to include the effects of saturation in the calculated phase shift values. Also, the output sent to the first kicker (from the left side of the amplifier) is used as this is most relevant for the phase shift in the chicane (the orbit should be closed after the second kicker with no further phase shift in the chicane after that point). The value of K is derived from the kicker design, in which 1.4 kV applied to each strip gives a 1 mrad kick for a 150 MeV beam [TODO: REF]. The actual CTF3 beam energy at this time was approximately 135 MeV (calculated based on the dipole currents used in the machine setup), so the value of K above is scaled by a factor 150/135.

In Figure 2.21 the red line “MODEL” shows the predicted phase shifts using Equation 2.4.1. Table 2.3 compares the fitted gradients and maximum phase shift for the model and real data. The overall agreement between the two is good, with the residuals between both the model and the data, as well as the linear fit to the data and the data, generally consistent with zero within error bars in the $\pm 1.2 \text{ V}$ linear range of the amplifier as shown in Figure 2.22.

Outside the linear range some discrepancies appear, although at the maximum $\pm 2 \text{ V}$ output the agreement is good so the effect is largest where the amplifier is entering saturation but before hard saturation is reached. However, most amplifier effects can be excluded as the analysis in this section uses the same dataset that was used to characterise the amplifier performance in Section 2.2. This could hint at possible remaining higher order errors in the TL2 chicane optics, or unexpected behaviour from the kickers or amplifier. Although subtracting alternating, interleaved pulses should remove the sensitivity to drifts in the machine it is possible that some residual effect remains. To determine whether the discrepancies are reproducible further scans of this type will need to be completed in the

future. The residuals between between the data and the linear fit between ± 1.2 V would also be of significance for the PFF correction should they not converge to zero with additional measurements, as they are of similar magnitude to the 0.2° downstream jitter target.

However, the overall conclusion is as expected — the phase shift in the chicane linearly depends on the amplifier input in the ± 1.2 V (± 2500 DAC counts) region thus a close to optimal correction can be applied in this range, corresponding to a $\pm 4.2 \pm 0.1^\circ$ phase shift. However, when the calculated optimal correction is between an absolute input voltage of 1.2 V and 2.0 V, 2500 to 4096 DAC counts, or $\pm 4.2 \pm 0.1^\circ$ to $\pm 7.0 \pm 0.2^\circ$, the actual phase shift in the chicane is lower, only up to $\pm 5.5 \pm 0.3^\circ$, due to the amplifier entering saturation (and possibly other effects to be determined). Any calculated correction outside $\pm 5.5 \pm 0.3^\circ$ receives a static phase shift of $\pm 5.5 \pm 0.3^\circ$ in the chicane. In the limit where all pulses are outside this range the PFF system can only induce a static shift in the mean phase and makes no improvement to the phase jitter. Understanding the impact of the limited correction range on the PFF results was particularly critical for interpreting the early correction attempts with the first version of the amplifier, giving approximately half the ranges shown in this section. This is discussed using simulations of the PFF system in Chapters ?? and ??.

<http://accelconf.web.cern.ch/accelconf/ipac2011/papers/tupc007.pdf> 1.4 kV to each strip
 $= 1$ mrad kick at 150 MeV 1.26 kV to each strip $= 1$ mrad kick at 135 MeV

2.4.2 Variations Along Pulse

[TODO: In this section I intended to check the stability of the constant kick along the pulse, as I did for the "Shape" section with the amplifier above. The results from the constant kick data do not look good, though - the errors are quite large and there are some nasty oscillations along the pulse, such as in the example Figure 2.23. With the phase stability downstream a much longer scan would probably be needed to draw conclusions here, though even on longer time scales I think it needs to be checked that the difference between odd and even pulses converges to zero. As it is I would probably choose to skip this section, or possibly just show one of the better plots.]

2.4.3 Shape

[TODO: The purpose of this section is to compare the shape of the given kick to the upstream phase - i.e. compare the upstream phase to the amplifier monitoring output and the difference in the downstream phase with PFF off and on. Again here my first attempts produced results that were not as I'd like, without particularly good agreement between the difference in the downstream phase and the upstream phase shape. Looks kind of like the two are rotated with respect to each other. More analysis needed here to check more thoroughly. I think this section should definitely be included, but I need either an explanation for the differences or to find datasets where the agreement is much better.]

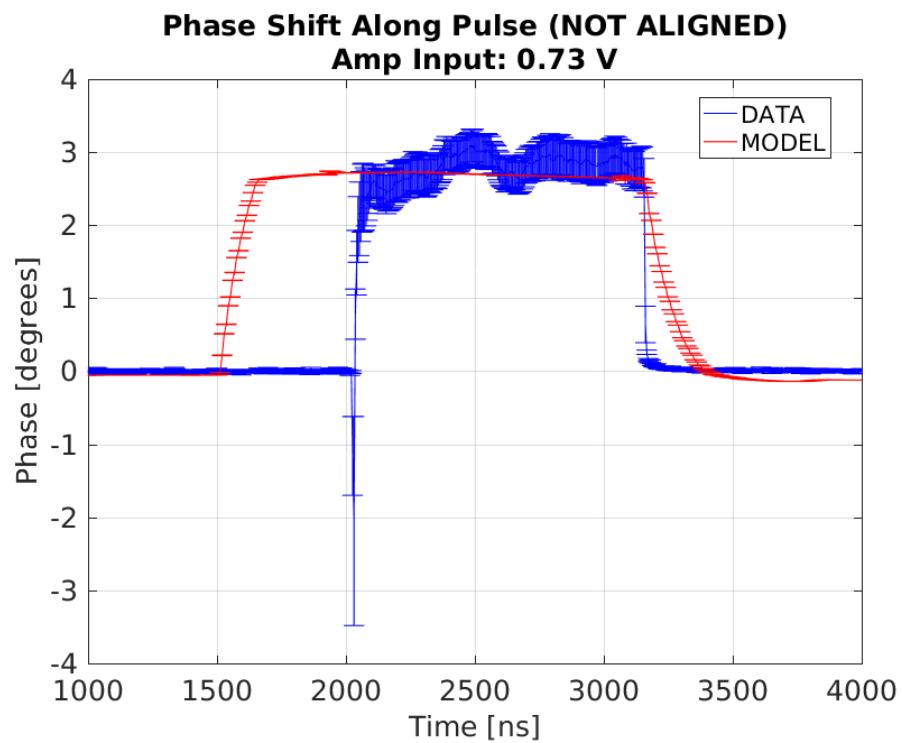


Figure 2.23: Traces relative timing scan.

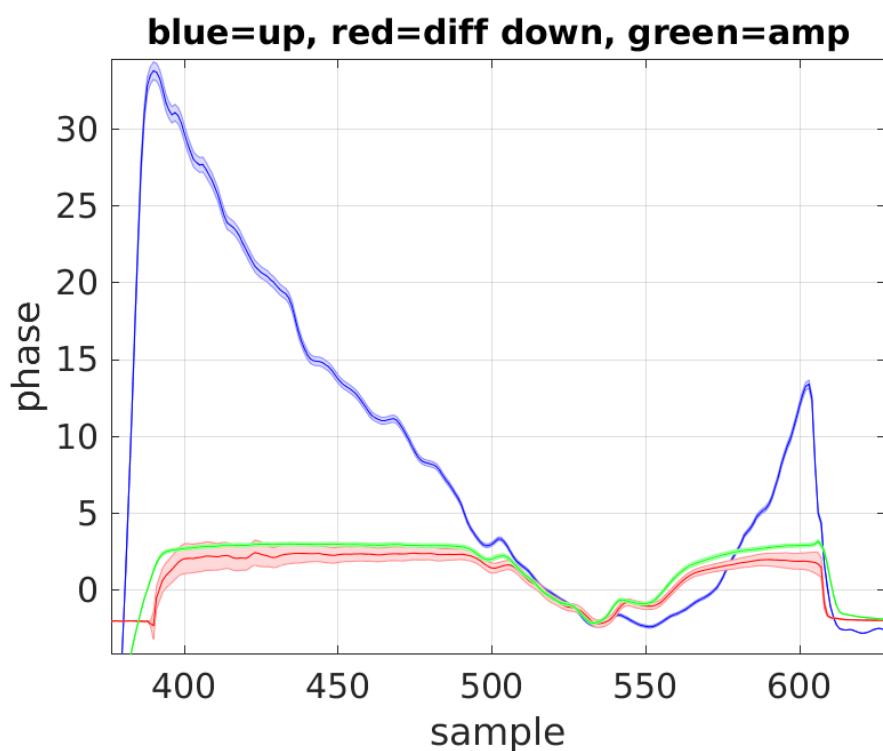


Figure 2.24: Traces relative timing scan.

2.4.4 Orbit Closure

At CLIC the PFF system must not degrade the transverse beam stability. This means for any voltage sent to the kickers the horizontal beam orbit after the PFF chicane must be unchanged, or closed, despite the different orbits inside the chicane. As such, the PFF optics for the TL2 chicane at CTF3 is also designed to give a closed kick, as presented in Section ???. However, up until now the main focus during PFF operation has been the primary goal of reducing the downstream phase jitter and ensuring good beam transmission to the downstream phase monitor. As a result orbit closure after the TL2 chicane has not yet been strictly enforced during PFF operation as will be seen in this section, but the current status is shown here as an additional cross-check of the PFF optics and to highlight where improvements are needed for future tests.

Using the same constant kick data as Section 2.4.1 Figure 2.25 shows mean the horizontal orbit before, inside and after the TL2 chicane across the full ± 2 V range of inputs sent to the amplifier. The vertical black lines on the plot mark the approximate location of the entry to the chicane (index CC.500) and the exit of the chicane (index CC.800), with the two kickers being located at CC.480 and CC.780. Two BPMs before and after the chicane, as well as the four inside the chicane, are included. The plotted positions are the difference between the kicked and nominal (non-kicked) orbit at each BPM, thus removing any misalignment in the BPM centres. Before the chicane and the first kickers there is no significant effect on the orbit as expected. Inside the chicane the PFF system induces an orbit offset of up to 1.4 ± 0.1 mm. After the chicane, in BPMs CC.845 and CC.930, the orbit should return to zero in the ideal case. However, a clear residual offset can be seen, up to 0.5 ± 0.1 mm in CC.930.

During this scan the input sent to both sides of the amplifier was the same magnitude. However, in Section 2.2.2 it was seen that the right side of the amplifier, sent to the second kicker, gave 4% lower output than the left side. This could explain why the orbit after the chicane was not closed during this scan, and during PFF operation which has typically used equal gain for both correction outputs to date. Figure 2.26 shows the expected orbit in the TL2 chicane in the case where both kickers are driven with the same voltage (“nominal optics”) and with the 2nd driven with a 4% lower voltage (“real amplifier ratio”).¹ The full MADX orbit propagated through all elements is shown, with the eight real measured BPM offsets also included at their respective positions. Each BPM point represents the gradient of a linear fit using the variation with input voltage seen previously in Figure 2.25. Before and inside the chicane the agreement between the BPM data and the model is excellent. As seen before, the BPM orbit is not closed after the chicane, unlike the nominal optics. If the actual kicker voltage ratio is taken in to account the MADX orbit after the chicane is not closed either, but the offset has opposite polarity to the real data in the last BPM.

The true explanation for the non-closed orbit is that the quadrupole strengths used in the machine setup are not exactly nominal. Although every effort has been made to keep the TL2 optics as close to nominal as possible, particularly inside the chicane, it is an

¹The term “nominal optics” is used in this section to refer to the nominal PFF optics, not the nominal optics created in Chapter ?? to use when the PFF system is not under operation.

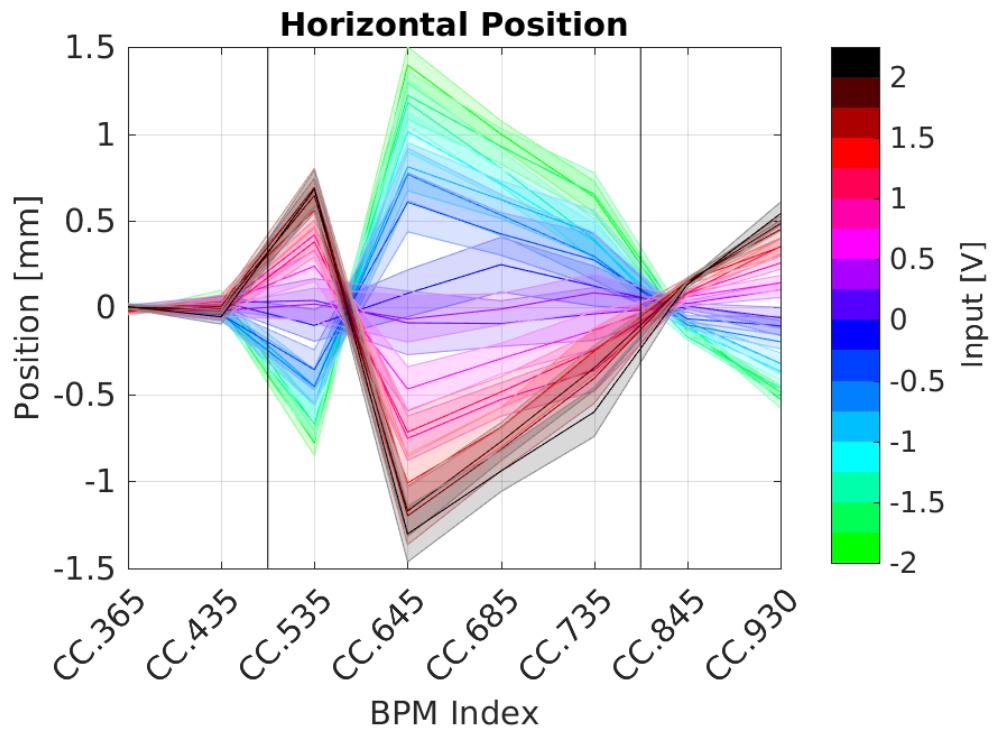


Figure 2.25: Horizontal orbit offset in and around the TL2 chicane at different input voltages sent to the amplifier.

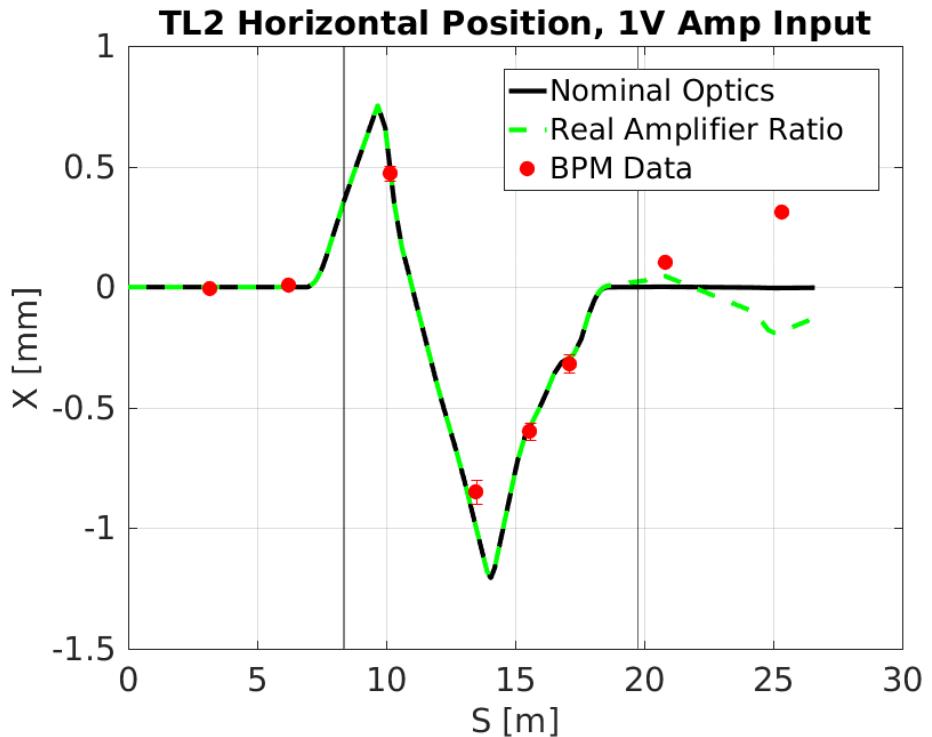


Figure 2.26: Orbit in the TL2 chicane at 1 V amplifier input for the BPM data, nominal model and model taking in to account the difference in amplifier output voltage to each kicker.

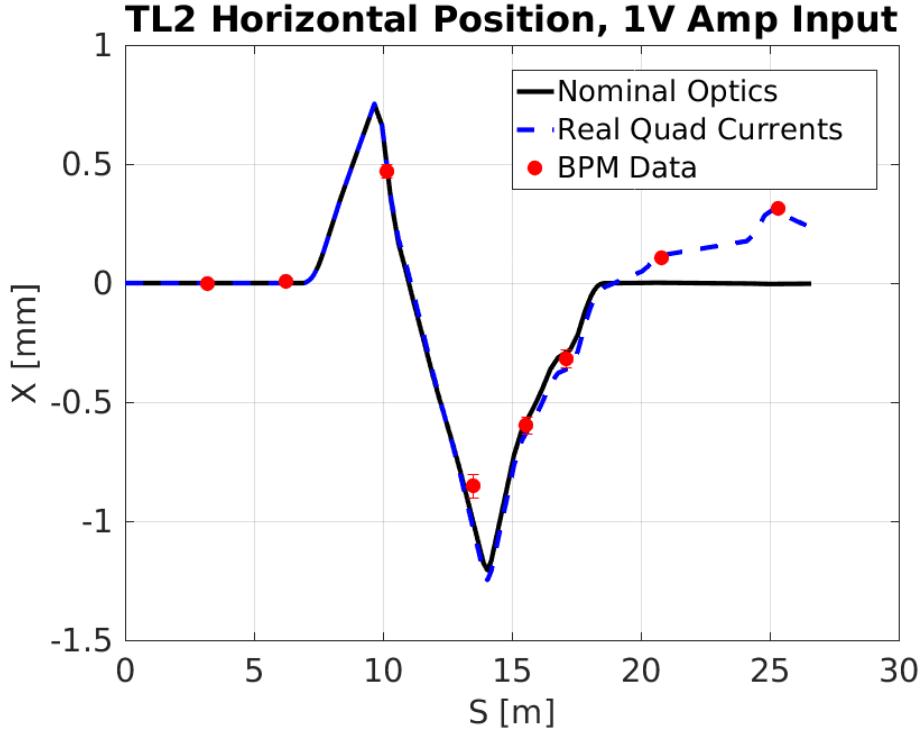


Figure 2.27: Orbit in the TL2 chicane at 1 V amplifier input for the BPM data, nominal model and model taking in to account the quadrupole currents in the real machine setup.

extremely sensitive area for the setup of CTF3 and beam transport in to the CLEX area downstream of TL2 (including the location of the downstream phase monitor in the TBL line) is always difficult. Minor modifications have therefore been necessary in order to achieve full beam transmission to the downstream area, both for PFF and other experiments at CTF3. The largest changes have been made to the four quadrupoles following the chicane but one quadrupole inside the chicane, CC.IQFL0730 (just prior to the 2nd kicker) has a set value 10% lower than the nominal optics, as well as differences up to 2% in the other quadrupoles. Using the real quadrupole strengths used in the machine gives the result shown in Figure 2.27. In this case the agreement between the model and the data is also extremely good after the chicane. It may still be possible to compensate for these differences by outputting different voltages to each kicker and this will be investigated. Alternatively, a completely nominal optics can be set in the chicane purely for the purposes of verifying orbit closure, reverting back to non-nominal optics and closure if needed to achieve good beam transmission for normal PFF operation.

[TODO: Not enough detail r.e. why beam transport there is difficult etc.?]

[TODO: Do have data with different ratios of kicker strengths. Can analyse to see effect on closure. Considering quad currents don't think it adds anything to discussion here, though.]

[Comment for Piotr: With these quad currents also expect to see some dispersion leaking out of the chicane. Up to 0.3 m in girder 9.]

2.5 Correction Output Timing

All the results based on the amplifier outputs and kicked beam presented so far have used a constant output voltage sent from the FONT5a board across the full $1.4 \mu\text{s}$ time window that the amplifier is powered for. As the $1.4 \mu\text{s}$ amplifier output sent to the kickers is much longer than the $1.1 \mu\text{s}$ CTF3 beam pulse it is easy to ensure that the full length of the pulse experiences the constant kick with this setup. However, for operation of the PFF system precise control of the correction output timing becomes critical. In order to remove phase variations along the pulse with the PFF system the output correction signal, shaped by the upstream phase, must arrive at the kickers exactly in sync with the beam. Any timing misalignment between the beam and correction signal arrival will result in residual oscillations along the pulse in the downstream phase, even in the case where the upstream-downstream phase propagation is perfect. Approximating the phase sag along the pulse to be quadratic, $\phi_u(t) \sim \phi_d(t) \sim t^2$, a misaligned correction would yield a corrected downstream phase with a linear increase in phase along the pulse with time, $\phi_{PFF}(t) \sim \phi_d(t) - \phi_u(t + \delta) \sim -2\delta t - \delta^2$, for example, where ϕ_{PFF} is the corrected phase, ϕ_d the uncorrected downstream phase, ϕ_u the upstream phase, t the time and δ the time misalignment in the applied correction. Also, the effect is particularly significant for any higher frequency variations in phase along the pulse. If a 40 ns oscillation is present in the upstream phase but the correction is applied with a 50 ns delay, for example, a second 40 ns oscillation with opposite sign would be introduced to the “corrected” downstream phase at a later time with no change to the initial oscillation. Although the effects are most visible along the pulse, any timing delay will also degrade the achievable mean phase jitter. This section gives an overview of the main methods that have been used to ensure that the correction output to the two kickers arrives in time with the beam.

2.5.1 Kicker Cable Lengths

The cables carrying the correction signal between the PFF amplifier and the kickers in the TL2 chicane are the single largest contributor to the overall system latency. They must be routed from the PFF electronics racks (in the klystron gallery, one floor and directly above the location of the upstream phase monitors), down in to the machine hall and across the width of the CTF3 facility to the TL2 chicane. The initial kicker cables installation used pre-existing cable trays and gave a signal transit time of 260 ns, with a signal speed of 0.66 c and approximate lengths of 50 m. This is more than two thirds the overall PFF latency budget, which must be lower than the 380 ns beam time of flight between the upstream phase monitor and the first kicker. Considering the latencies of the various pieces of hardware in the PFF system chain as well as the cables between the upstream phase monitors and the PFF electronics (Section ??), the overall PFF system latency would have been in excess of the 380 ns beam time of flight with this setup. By re-routing the cables on to a dedicated pathway and trimming any remaining slack it was possible to reduce the cable lengths by up to 90 ns, bringing the system within the latency budget as will be seen in the following sections. Precise measurements of the cable lengths with this setup are presented in this section, as well as their significance beyond ensuring the system is within the latency

requirements.

With two kickers, two strips per kicker and two ends of each strip a total of eight cables are needed. The drive from the amplifier is sent to the downstream end of each kicker strip, traverses the kicker, and is then terminated back at the amplifier after leaving the upstream end. Drive is sent to the downstream end of each kicker (meaning it propagates through the kicker in the opposite direction to the beam) so that the electric and magnetic fields between the strips are in the same direction, as discussed in Section ???. Rather than being connected directly to the amplifier, the eight kicker cables are connected to a patch panel below the amplifier in the PFF electronics racks. Eight additional cables, around 70 cm in length, are used to connect the amplifier outputs to the patch panel. This is in order to create a tidier cabling setup in the rack as well as making changes to the amplifier cabling easier, when necessary. [TODO: Picture]. The kicker cables are of type [TODO: REF] with HN-type connectors and the patch panel cables of type [TODO: REF] with N-type connectors to match the amplifier.

The length of the eight kicker cables and eight patch panel cables has been measured using time domain reflectometry (TDR) on a network analyser [TODO: REF?]. The network analyser is used to send a short pulse down the cable, with one end of the cable connected to the network analyser and the other end disconnected so it is not correctly terminated. As the signal reaches the (non-terminated) end of the cable the discontinuity in impedance creates a reflected signal that propagates back to the network analyser. The time difference between when the signal was output and when the reflected signal arrives back at the network analyser therefore corresponds to double the one-way signal transit time in the cable. [TODO: Example TDR plot?]

Table 2.4 shows the patch panel cable lengths and Table 2.5 the kicker cable lengths that were determined with this method. Quoted errors of ± 0.05 ns are estimated based on the sampling rate of the measurement. The amplifier port, patch panel port and kicker strip that the cables are connected to are also shown in the table, as well as their corresponding CTF3 identifying number for reference. For the amplifier port labels the three letters correspond to:

- Whether the cable is connected to the **L**evelt or **R**ight side of the amplifier.
- Whether the cable is connected to the amplifier **A** or **B** outputs on that side.
- Whether the cable is connected to the amplifier **D**rive or **T**erminator.

And for the kicker strip labels the three letters correspond to:

- Whether the cable is connected to the first (**1**) or second (**2**) kicker.
- Whether the cable is connected to the **U**pstream or **D**ownstream end of the kicker strip.
- Whether the cable is connected to the **L**evelt or **R**ight kicker strip, as viewed looking at the upstream end of the kicker.

Label	Length	Amplifier Port	Patch Panel Port
2907701B	2.99 ± 0.05 ns	LAT	1
2907703B	3.03 ± 0.05 ns	LBT	2
2907700B	3.03 ± 0.05 ns	LAD	3
2907702B	3.01 ± 0.05 ns	LBD	4
2907838B	3.03 ± 0.05 ns	RAD	5
2907740B	3.05 ± 0.05 ns	RBD	6
2907739B	3.03 ± 0.05 ns	RAT	7
2907741B	3.03 ± 0.05 ns	RBT	8

Table 2.4: Lengths of cables between the amplifier and the patch panel.

Label	Length	Patch Panel Port	Kicker Strip
2907701A	171.28 ± 0.05 ns	1	1UL
2907703A	171.30 ± 0.05 ns	2	1UR
2907700A	171.29 ± 0.05 ns	3	1DL
2907702A	171.30 ± 0.05 ns	4	1DR
2907838A	205.45 ± 0.05 ns	5	2DL
2907740A	205.62 ± 0.05 ns	6	2DR
2907739A	205.15 ± 0.05 ns	7	2UL
2907741A	204.49 ± 0.05 ns	8	2UR

Table 2.5: Lengths of cables between the patch panel and the kickers.

Finally, the patch panel connectors are simply labelled from 1 to 8 from left to right, as viewed from the front of the rack. All of the cable connections between the amplifier, patch panel and kickers are shown in Figure 2.28.

The patch panel cables all have lengths of around 3 ns, with the lengths of each matched to within the measurement error. After the re-routing and shortening of the kicker cables the cables connected to the first kicker have a length of around 170 ns, whilst the cables for the downstream kicker are longer at around 205 ns. For the downstream kicker the latency requirements are slightly relaxed due to the additional 36 ns beam time of flight between the kickers. Rather than also shortening the downstream kicker cables as much as possible some additional slack was left so that the difference in lengths is similar to the difference in the beam time of flight between the two. This means the two correction outputs (one for each kicker) can be sent from the FONT5a board at, or close to, the same time as discussed in Section 2.5.3.

Although all the upstream kicker cables are matched within the measurement error there are some differences in the downstream kicker cable lengths, with cable 2907741A more than 1 ns shorter than cable 2907740A, for example. If there is a difference between the lengths of the cables connected to the downstream left and downstream right strips of a kicker (the driven end) there will be a time offset in the voltage applied to each side of the kicker, which would degrade the quality of the PFF correction. However, there is no need for the cables connected to the upstream ends of the kickers to be of matched lengths,

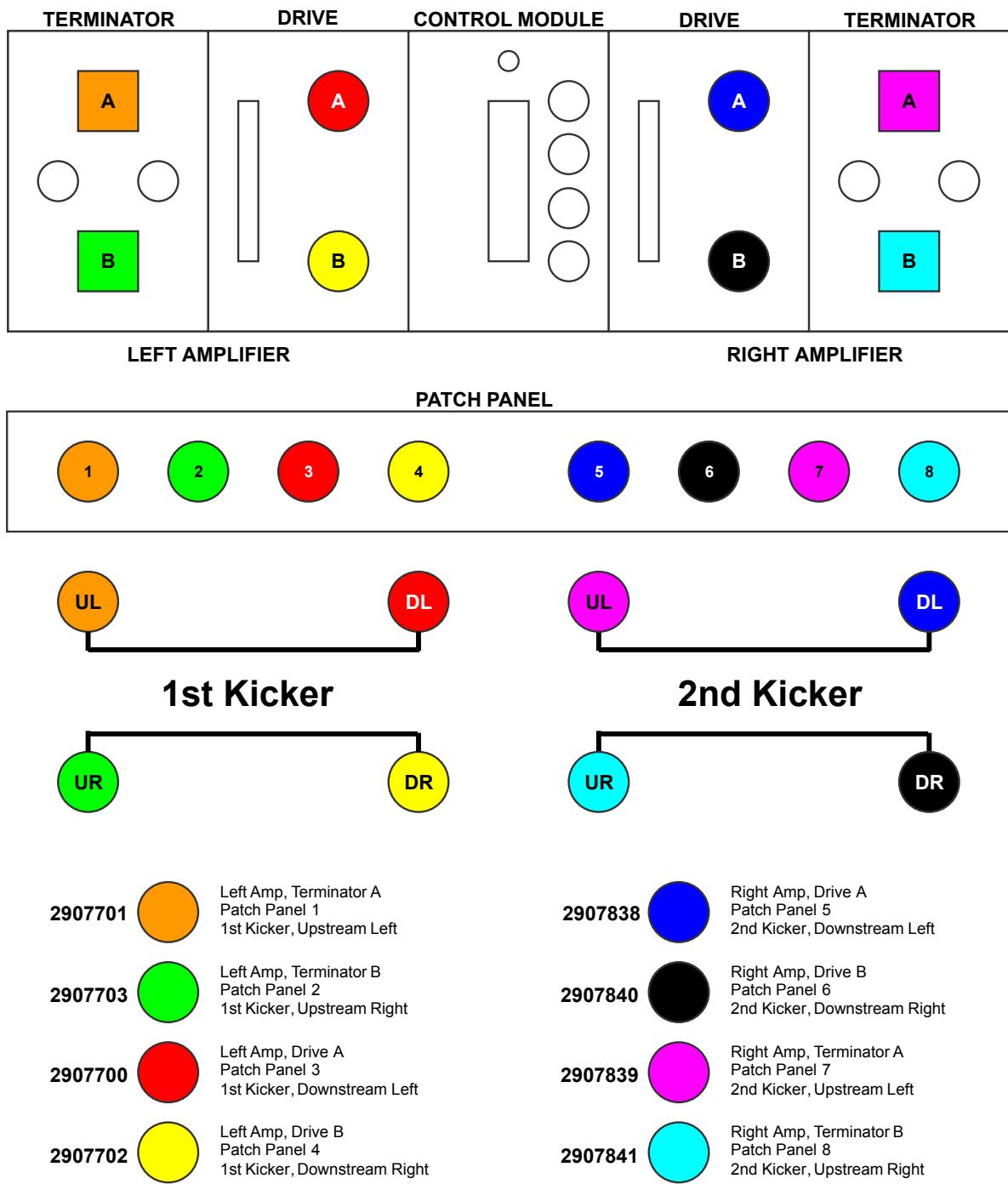


Figure 2.28: Cabling setup for cables between the amplifier and kickers.

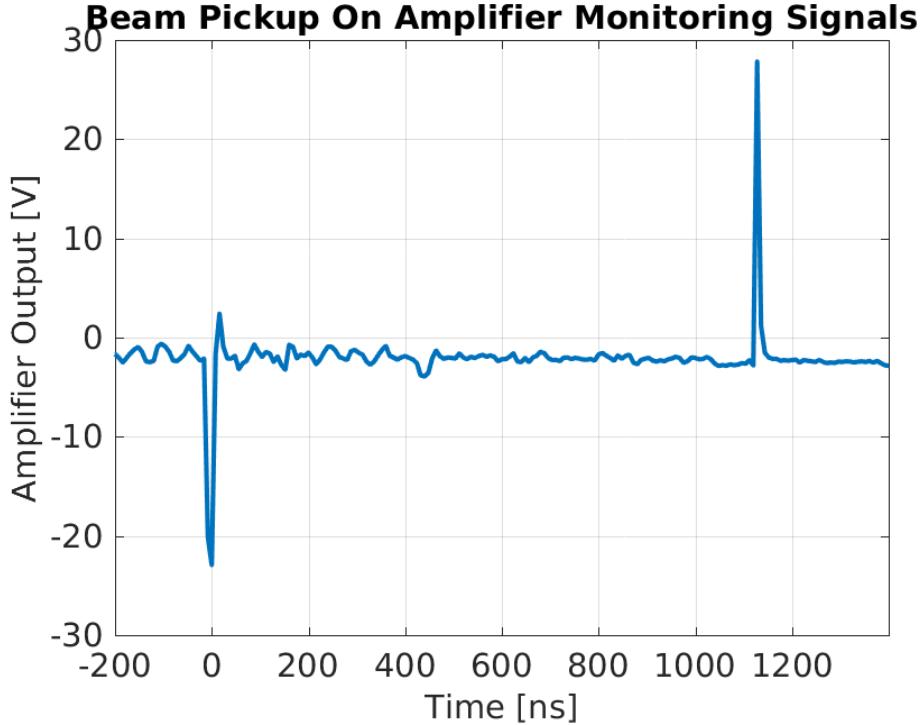


Figure 2.29: Beam pickup on kicker strips as seen on amplifier monitoring signals.

the only requirement is that they are terminated correctly at the amplifier. The shorter 2907741A cable is therefore connected to the upstream end of the second kicker, and the cables 2907838A and 2907740A, with lengths matched to within 200 ps, are used to carry the amplifier output to the downstream end of the strips.

[TODO: Tolerances for cable length matching?]

2.5.2 Absolute Timing

Using Beam Pickup

[TODO: Kicker pick-up theory. In particular, is time between pickup exactly the beam pulse length or is it longer by double the kicker length?]

Figure 2.29 shows the beam pickup at the start and end of the pulse from the PFF kickers at CTF3, as seen on one of the amplifier monitoring outputs (each of the four amplifier monitoring outputs, one for the upstream end of each strip prior to the signal being terminated at the amplifier, gives a similar response). The separation of the peaks in the beam pickup is $1.1 \mu\text{s}$, thus the same as the CTF3 pulse length as expected. By comparing the timing of these peaks with respect to the start and end of the amplifier output pulse, using the same amplifier monitoring signal, it is possible to ensure that the correction output arrives in sync with the beam.

An example of this is shown in Figure 2.30. A constant DAC output is sent from the FONT5a board to the amplifier and both this output pulse and the beam pickup, at samples

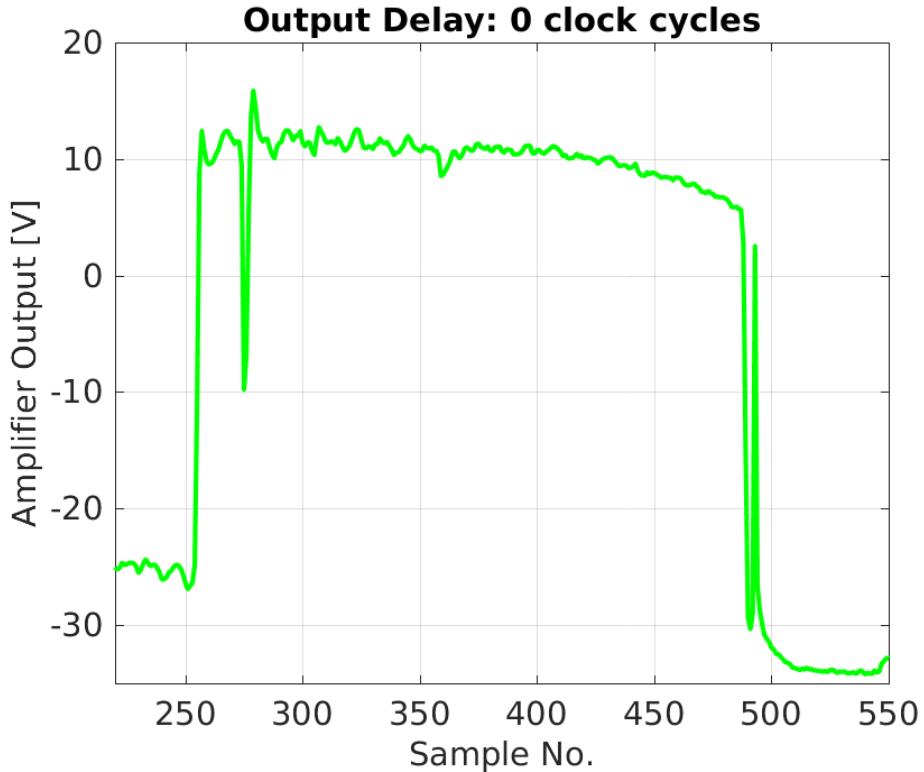


Figure 2.30: Output delay of 0 clock cycles. Full pulse.

275 and 493, are visible in the figure. Importantly, the DAC output is gated using the upstream phase monitor diode signal (in other words, the constant DAC output is only sent during the time when the diode is non-zero) and this has two consequences. Firstly, the amplifier output pulse has the same length as the beam pulse in the upstream phase monitor. Secondly, the timing of the output is identical to what it would be in normal PFF operation. In the case of Figure 2.30 the drive to the amplifier is sent as quickly as possible after the arrival of the upstream diode signal at the FONT5a board. It can be seen that the amplifier pulse arrives before the beam pickup, thus with the PFF system setup this way the correction would be applied slightly early. This result therefore proves that the PFF system just meets the latency requirements, with the overall time needed to transport and process all the relevant signals a few tens of nanoseconds less than the 380 ns time of flight of the beam between the upstream phase monitor and the first kicker. However, what is also clear in the figure is that the time offset between the start of the amplifier pulse and the first beam pickup spike is much larger than the time difference between the end of the amplifier pulse and the second beam pickup spike. This is due to the energy transient across the first 100 ns of the CTF3 beam pulse which is present in the upstream phase monitor but is then lost prior to the TL2 chicane, predominantly in TL1. As a result the downstream beam pulse is shorter than the upstream beam pulse which defines the length of the correction output. Therefore, in order to align the correction output with the beam the signals from the end of the amplifier and beam pulses must be used, not the start.

The firmware for the FONT5a board includes an output delay parameter that can be used to fine-tune the timing of the correction output sent to the amplifier. This can be done

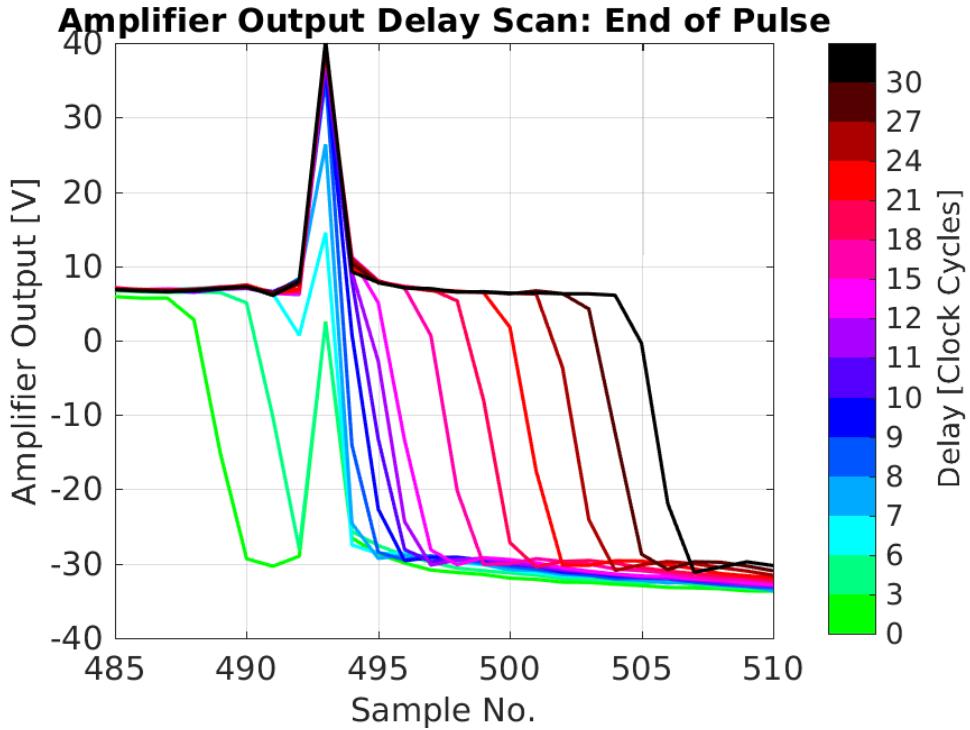


Figure 2.31: Output delay scan, end of pulse.

independently for each of the two correction outputs so that it can be ensured the correction arrives in sync with the beam in each kicker individually (the relative timing of the two kickers is discussed in the next section). The delay can be varied between 0 and 31 clock cycles in integer steps, with one clock cycle corresponding to one period of the 357 MHz ADC clock frequency, or 2.8 ns. A delay of up to 86.8 ns can therefore be added to the correction outputs. Figure 2.31 shows the effect of varying the output delay across the full range of possible values, zoomed in on the end of the pulse. For all output delays the beam pickup remains at sample 493, as expected. Meanwhile, the end of the amplifier pulse is moved from before the beam pickup (output too early) to after the beam pickup (output too late). To achieve the optimal correction timing the end of the amplifier pulse must be aligned with the beam pickup and this is achieved with a delay of 7 clock cycles, or 19.6 ns, as shown in Figures 2.32 and 2.33. This delay has been used for the latest PFF runs presented in Chapter ???. Due to ambiguity in which point along the falling edge of the amplifier pulse the beam pickup should be aligned to there may be a remaining error of up to 3 clock cycles in the exact alignment, and this can only be verified by beam based measurements (not using the amplifier monitoring outputs).

Using BPMs

This section presents one way in which the correction output timing can be determined using a combination of the phase monitor measurements and a BPM signal downstream of the TL2 chicane. The results shown here were performed with the first, lower power version of the amplifier and the FONT5 rather than the later FONT5a board, and because of this

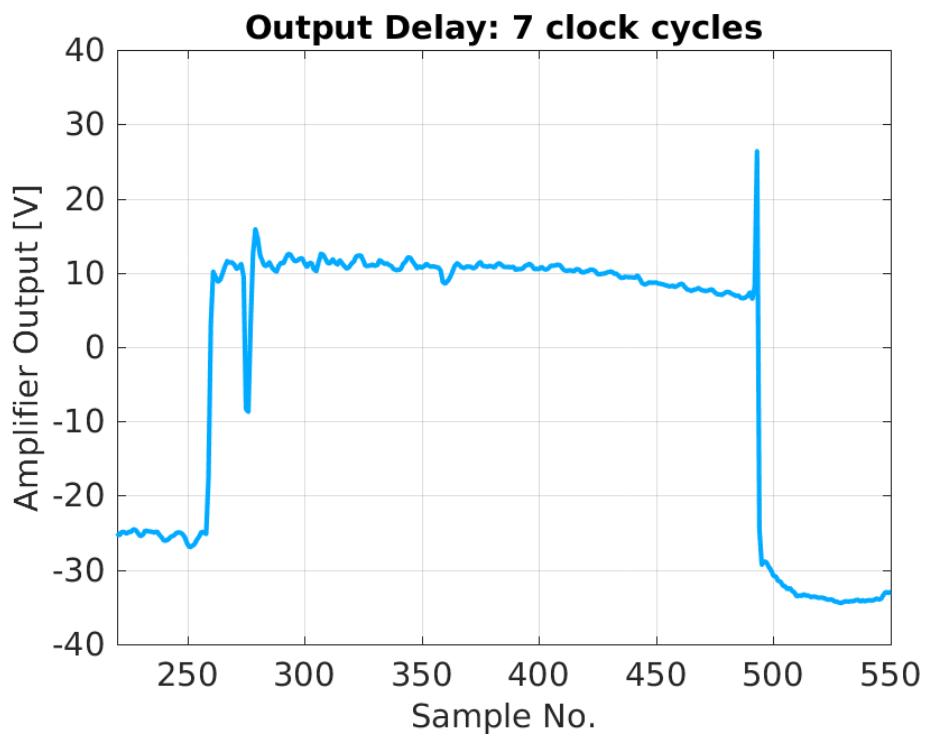


Figure 2.32: Output delay of 7 clock cycles. Full pulse.

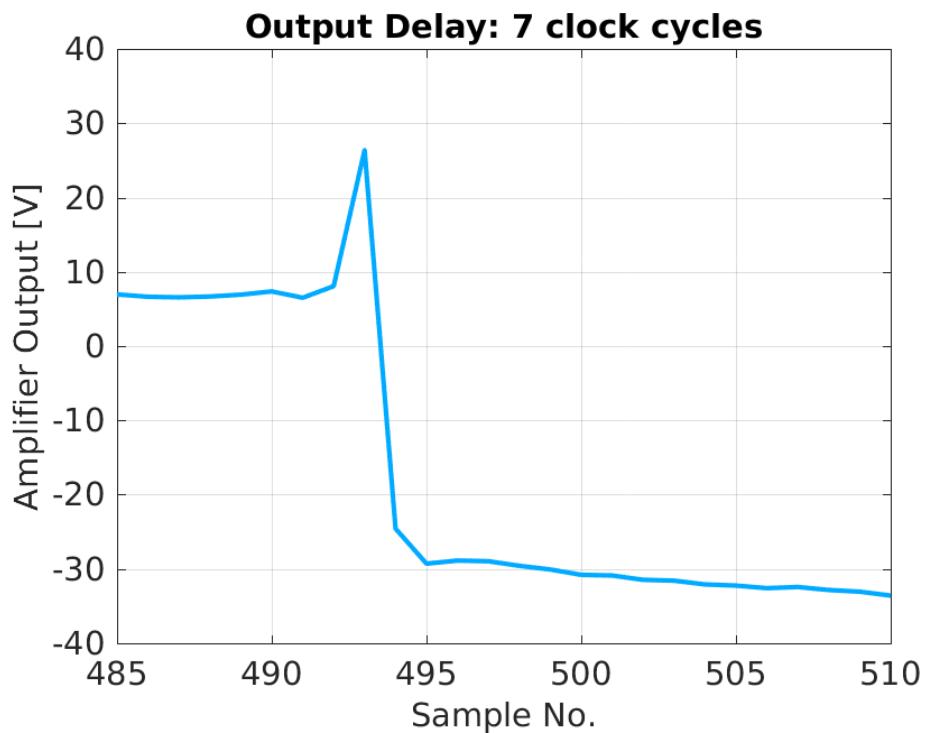


Figure 2.33: Output delay of 7 clock cycles. End of pulse.

the optimal output delay calculated here does not agree with the value of 7 clock cycles from the beam pickup based measurement above. The newer hardware has the same latency as the previous versions, thus the difference does not come from hardware changes but rather associated changes to cabling between the phase monitor electronics, FONT5a board and amplifier. The measurement will be repeated in the future to verify that both methods give consistent results when the same hardware and cabling setup is used.

The FONT5 (and FONT5a) board firmware provides the functionality to be able to change the gain of each PFF correction output independently. This means it is possible to apply the correction to only one kicker, or to kick the beam in the same direction in each kicker (i.e. to use the same sign for the gain in each kicker, rather than gains with equal magnitude but opposite sign). In both of these cases the kicked PFF orbit in the chicane is not closed, thus the horizontal position along the beam pulse in a BPM after the chicane depends on the shape and timing of the applied correction.²

Figure 2.34 compares the upstream phase, downstream phase and horizontal position (in a BPM after the TL2 chicane) along the pulse in the case where the PFF correction is applied with gains set to kick the beam in the same direction in each kicker, and with no output delay applied in the FONT5 board. The data is taken in interleaved mode, with the plotted phases shown using the PFF off data and the BPM trace being the difference between the PFF on and PFF off data. Each signal is scaled and sign flipped where necessary to give variations along the pulse with the same magnitude and sign, in arbitrary units. The BPM and phase monitor signals are acquired with the same sampling frequency of 192 MHz, with each aligned so that the end of the pulse is at the same sample number.

By taking the difference of the PFF off and PFF on data in the BPM any residual orbit variations along the pulse not related to the PFF system are removed, thus the remaining shape should match that of the PFF correction output, which in turn is linked to the upstream phase. The downstream phase should also have the same shape as the upstream phase with the PFF system off, within the limits of the upstream-downstream phase correlation achieved at this time. During this measurement many oscillations along the upstream phase were present, which usually are not desired but for this measurement are perfect points of reference to check the time alignment of the signals. As expected the overall shape of the residual horizontal position in the BPM along the pulse and the two phase signals is very similar. The largest feature in the upstream phase that is present in all three signals occurs at sample 671 in the upstream phase, with the location of the peak of this oscillation in the phase signals and the BPM marked by vertical black lines in the figure. The peak as seen in the BPM signal is clearly before the peak in the phase monitor signals thus in this case the correction was applied early, with a measured offset of -36 ns between the peaks.

This measurement was repeated with four different correction output delays applied in the FONT5 board, at delays of 0, 10, 20 and 30 clock cycles (0 to 84 ns), which includes points where the correction is applied both early and late. Fitting the measured time offset between the peaks in the BPM and the phase in the same way as before yields an optimal

²In Section 2.4.4 it was shown that the corrected orbit is not perfectly closed in normal PFF operation either. However, in this case no attempt at orbit closure is made so the measured effect seen in the BPMs is much larger.

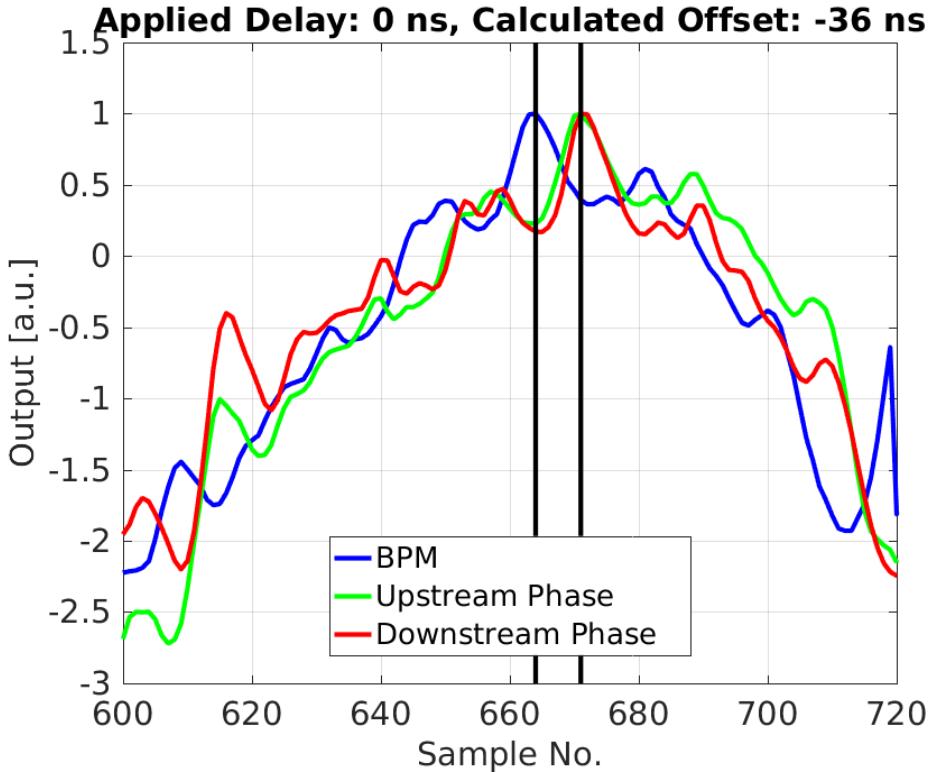


Figure 2.34: Kick output with no delay as seen on BPM and phase signals.

correction output delay to apply of 39 ± 7 ns (Figure 2.35), or 14 ± 3 clock cycles. Applying this delay in data analysis gives the result shown in Figure 2.36, in which the similarity of the three signals becomes clear.

2.5.3 Relative Kicker Timing

For the phase correction the absolute output timing sent to the first kicker, as derived above, is the most critical as this defines the alignment of the applied phase shift in the chicane with the beam. The second kicker's main purpose is then to close the kick created by the first, ensuring the orbit after the chicane is closed (with the caveats already mentioned in Section 2.4.4). For the purposes of orbit closure it is also important to ensure that the correction arrives at the second kicker in time with the beam. As discussed in Section 2.5.1 the beam time of flight between the kickers is about 36 ns, thus the correction must arrive at the second kicker 36 ns later than the first kicker. Most of this difference should be accounted for by the longer cable lengths for the second kicker, but the precise relative timing is checked here. In this context the relative timing means the additional output delay that must be applied to the FONT5a correction output for the second kicker with respect to the first in order to ensure the correction is aligned in time with the beam in both kickers.

Figure 2.37 shows a simulated example of the expected effect of kicking the beam with a relative time offset in each kicker, in this case with the output to the second kicker arriving later than the first kicker (with respect to the beam pulse). The kickers are driven with

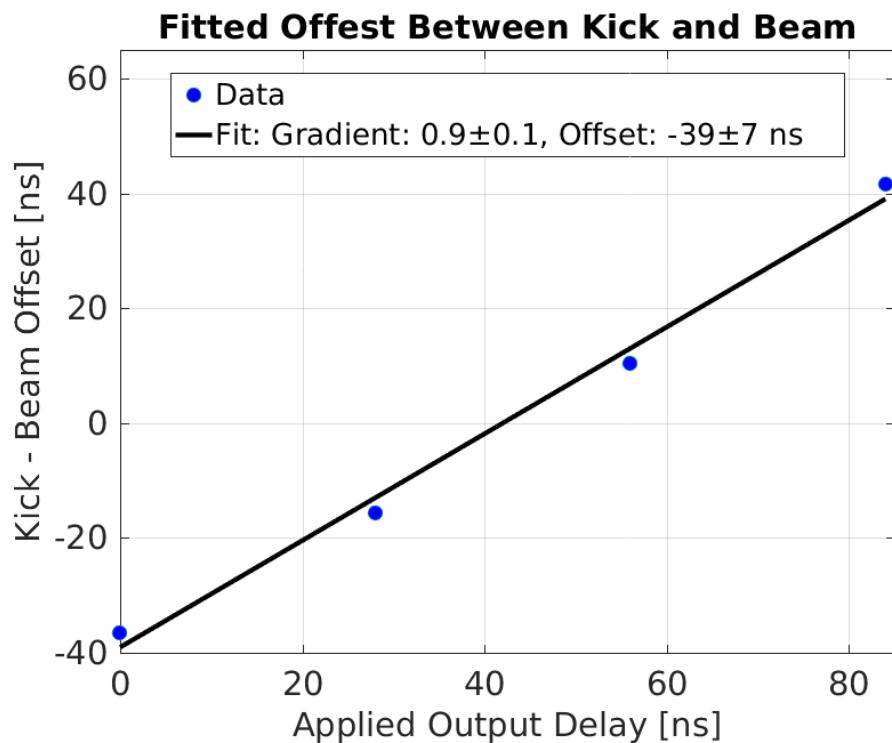


Figure 2.35: Fit time offset between kick and beam at different output delays.

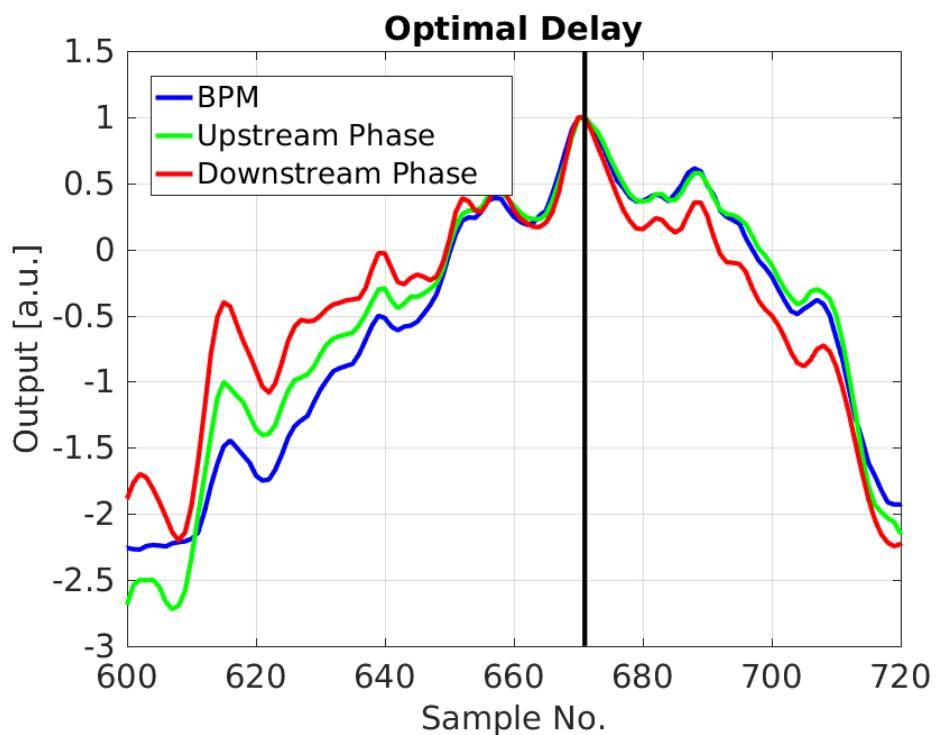


Figure 2.36: Alignment between BPMs and phase signals with optimal delay applied in analysis.

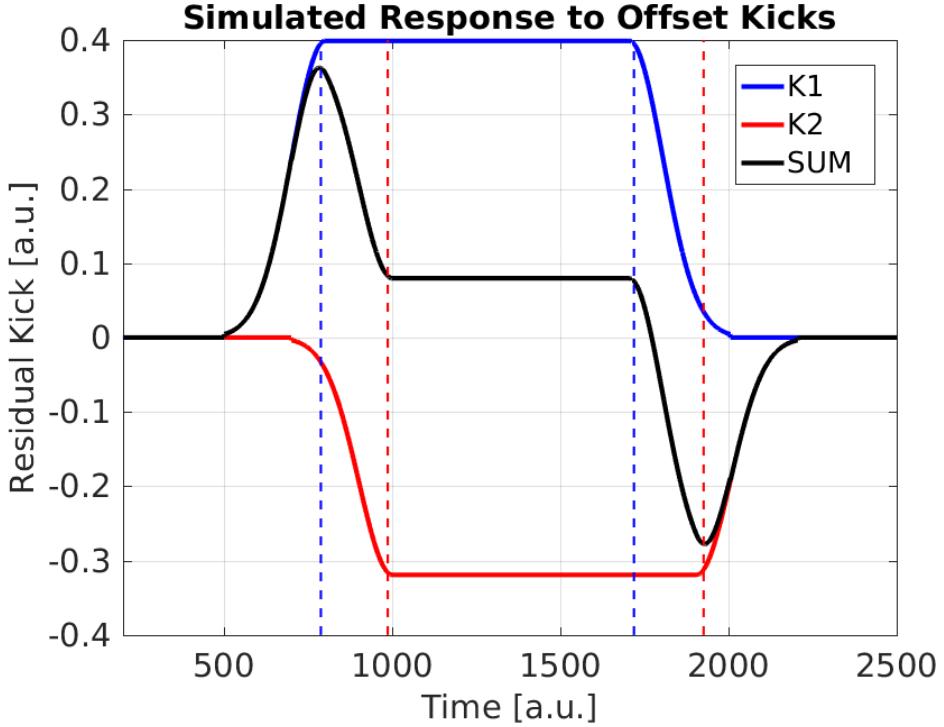


Figure 2.37: Simulated response to offset kicks.

opposite polarity in the same way as the PFF system, and the first kicker is shown with a larger output than the second. The total kick received in the chicane is given by the sum of the two, shown in black. In the ideal case the total/residual kick in the chicane should be zero so that the orbit is closed after the chicane. However, with a timing offset between the two kickers there are large peaks in the residual kick at the start and end of the pulse, where only one of the two kickers receives its full drive. Due to the different amplitude of the two kickers the residual kick is also non-zero in the central part of the pulse. With well-aligned timing the residual kick would be constant along the full pulse length, or zero across the full pulse length if the kicks had matched amplitudes.

By varying the relative timing of the two correction outputs on the FONT5a board (K1 and K2 delay) and using a BPM after the TL2 chicane to measure the size of the peaks at the start and end of the pulse resulting from the offset kicks (in the same way as Figure 2.37) the optimal relative delay can be determined. The optimal relative delay is the point that minimises the size of the peaks on the rising/falling edge of the pulse, with the peak magnitude approximately linearly dependent on the delay. Figure 2.38 shows the result of doing this, using a constant DAC output from the FONT5a board applied across a 168 ns portion of the pulse. The horizontal position in a BPM after the TL2 chicane is plotted for relative K2 delays ranging between -10 (K1 output delayed with respect to K2) to +10 (K2 output delayed with respect to K1) clock cycles. Aside from the asymmetry between the size of the peaks at the start and end of the pulse the result is as expected from the example previously discussed. [TODO: Why asymmetry? Differences in output along pulse?]. Note the non-zero position offset in the central part of the pulse. Based on the orbit closure results in Section 2.4.4 this is predominantly due to optics differences leading to a

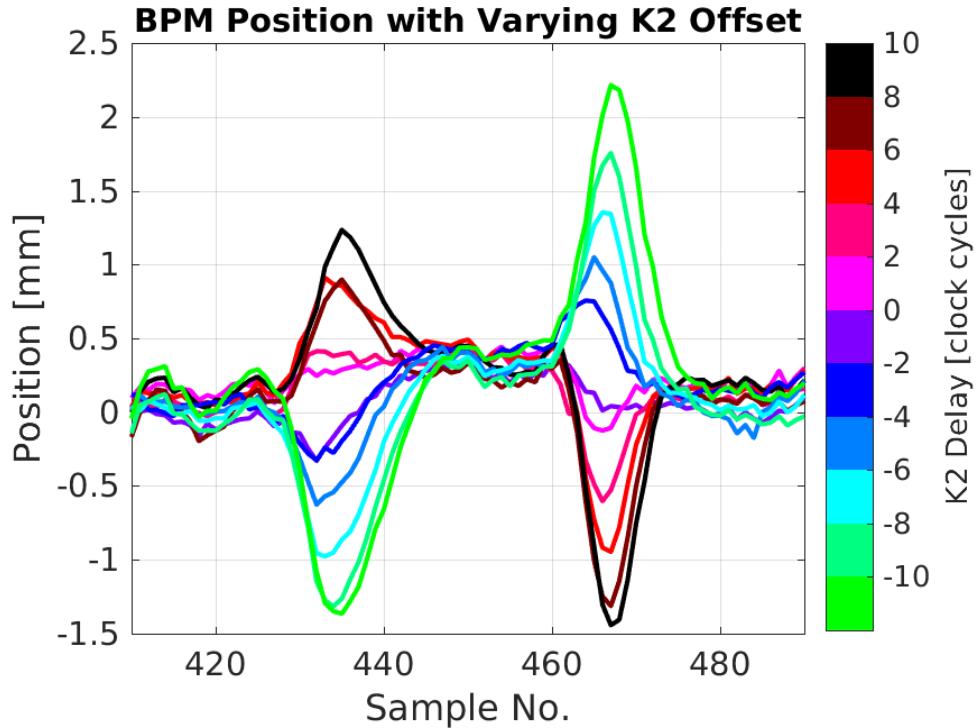


Figure 2.38: Measured BPM offset for different relative kick delays.

non-closed orbit, rather than the small difference in amplifier output voltage to each kicker.

Figure 2.39 then shows the peak beam offset in the BPM versus the relative K2 delay using the falling edge of the pulse. The peak beam offset is defined as the difference between the maximum and minimum beam position after the chicane between sample 458 and 477 (as seen in Figure 2.38 [TODO: Add vertical lines to show ranges?]). As the K2 delay approaches the optimal value the difference in beam position in this range converges to the 0.3 mm offset in the flat central part of the kicked pulse. The point of intersection between the two linear fits shown (one for the points with a positive peak position and the other for points with a negative peak) gives the optimal relative K2 offset to be 0.1 ± 0.5 clock cycles. Repeating the procedure for the peaks at the rising edge of the pulse gives a result of 1.9 ± 2.0 clock cycles, and the two results combine to give an optimal value of 0.5 ± 0.6 clock cycles.

Relative K2 delays of both 0 and 1 clock cycles have been used during PFF operation, with no measurable difference in the PFF results between the two to date although this will have to be verified with further orbit closure tests. Adding the absolute delay of 7 clock cycles derived in Section 2.5.2, the final delays to apply in the FONT5a board are:

- **K1 delay:** 7 clock cycles.
- **K2 delay:** 7 or 8 clock cycles.

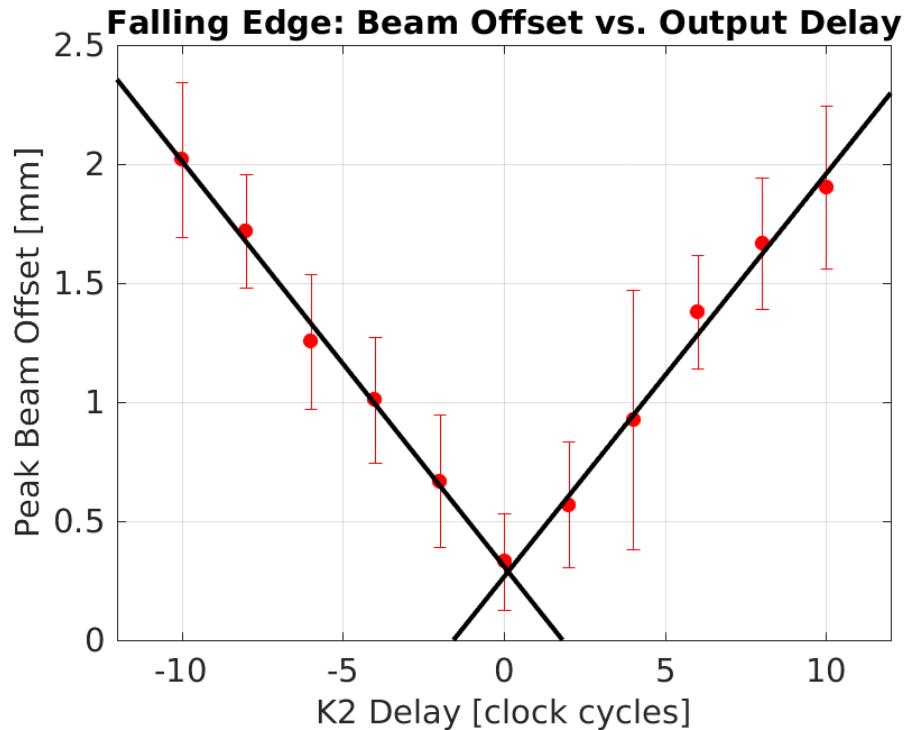


Figure 2.39: Fitted peak BPM offset vs. relative kick delay.

2.6 Early Phase Feedforward Attempts and Simulations

This is the introductory text.

2.6.1 Gain Scans

2.6.2 Effect of Limited Correction Range

Bibliography

- [1] Dummy One & Dummy Two. *Phys. Journal*, **1**, 1 (2002) 1–5. hep-ph/0000000.
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