

Development of a beam-based phase feed-forward
demonstration at the CLIC Test Facility (CTF3).

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Abstract

This is the abstract TeX for the thesis and the stand-alone abstract.

Dedication.

Acknowledgements

Acknowledgements.

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Glossary

Item1 Description.

Item2 Description.

Item3 Description.

Chapter 1

Setup and Commissioning of the PFF System

This is the introductory text.

1.1 Feedforward Controller (FONT5a Board)

1.1.1 Cabling Setup

1.1.2 Implementation of PFF Algorithm in Firmware

Not using arcsin in phase reconstruction - effect

Gain conversion factor

1.1.3 DAQ and Setup Parameters

gain

filter weights

timing delays

saturate rather than overflow output

Interleaved mode

1.1.4 ADC Droop Correction

The droop in the response of the FONT5 ADCs, as most clearly seen in the output of the diode channel in Figure 1.1 (although it also effects the mixer channel), is not an issue for the work the FONT group does at ATF2 where the signals are well approximated by

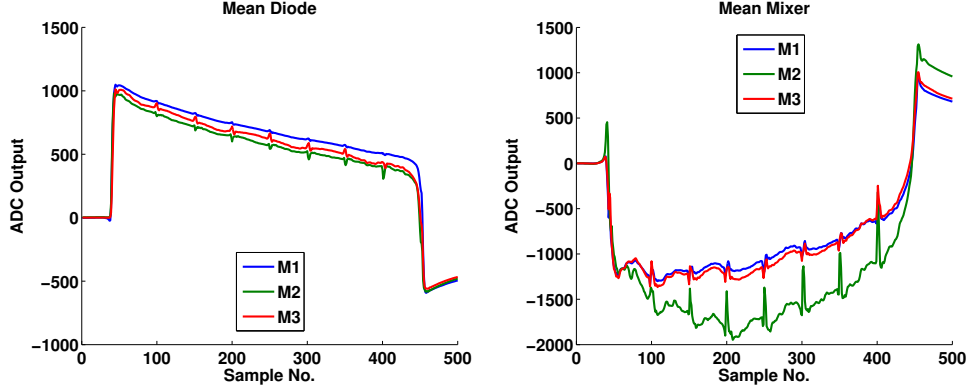


Figure 1.1: Mean diode and mixer output with no filter.

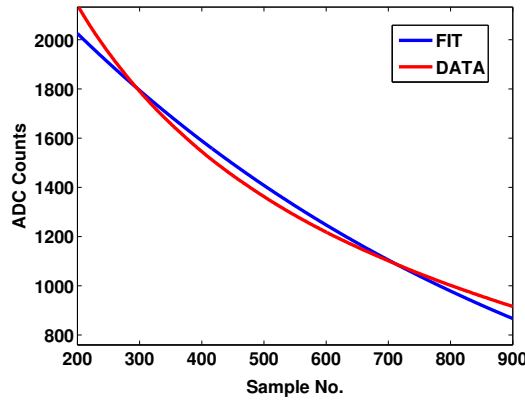


Figure 1.2: Attempted exponential fit to the ADC droop.

delta functions separated by ~ 100 ns. Although the droop has been seen previously, its significance for the continuous microsecond length pulse at CTF3 had not been considered because of this.

The droop emerges as a result of the use of AC coupling on the ADC input transformers for electrical isolation. This involves using a capacitor, the current across which is dependent on dV/dt (V being voltage and t time), to remove the DC component from a signal. In particular for the diode channel, which should be a square wave, the output is increasingly well described by a DC signal on the flat top as you move away from the leading edge of the pulse, with the capacitor causing droop in the response as a result.

In the simplest case the droop should be well described by an exponential decay of the form $A \exp(-t/T)$. The droop makes it difficult to perform calibrations and measurements on the data and one way in which it could be removed in offline analysis is by determining the decay constants, T , for each of the ADCs on the FONT5 board. To avoid the influence of beam effects tests were done in Oxford using a generated $10 \mu\text{s}$ DC pulse.

Unfortunately, as can be seen in Figure 1.2 which shows an example of an exponential fit for one ADC, although the fits return good R^2 values it is clear that the slope of the exponential curve is not a good match for the slope of the data. This is perhaps not unexpected as the ferrite cores used in the transformers have many non-linear properties. In fact, by

using a fit with two exponential terms it is possible to obtain a perfect match to the data but at this point the complexity of the fit would make any attempt to remove the droop in real beam data in this way spurious.

Instead, changes will be made to the currently in development FONT5a board hardware and firmware to greatly reduce the scale of the droop. Different transformers will be used to reduce the droop rate by up to a factor of fifty and in addition digital filtering will be implemented in firmware to smooth out and reduce the remaining droop component even further. It is expected that after these changes the droop will be small enough to not have a detrimental effect on the performance of the phase feedforward system.

1.2 Amplifier

1.2.1 Introduction

Amplifier versions:

First version (nov 2014) 350 V (check)

2nd version (jul 2015) 650 V - double FETs

3rd version: 1200 V with combiner module (?) not pursued

1.2.2 Installation

Amplifier inputs:

Trigger from FONT5a board

DAC1 and DAC2 from FONT5a board

Amplifier outputs:

4 drive signals - one for each strip. Sent to downstream end of kicker (why?)

4 terminators

Amplifier on time monitoring

Monitoring of each amplifier output

1.2.3 Linearity

Figure 1.4 shows the amplifier output, as measured by the monitoring signals, at different constant input voltages sent from the FONT5a board between the minimum of -2V (-4096 DAC counts) and maximum of 2V (+4096 DAC counts) [TODO: One of these 4095 not 4096?]. The output voltage from the monitoring signals is converted in to the real amplifier

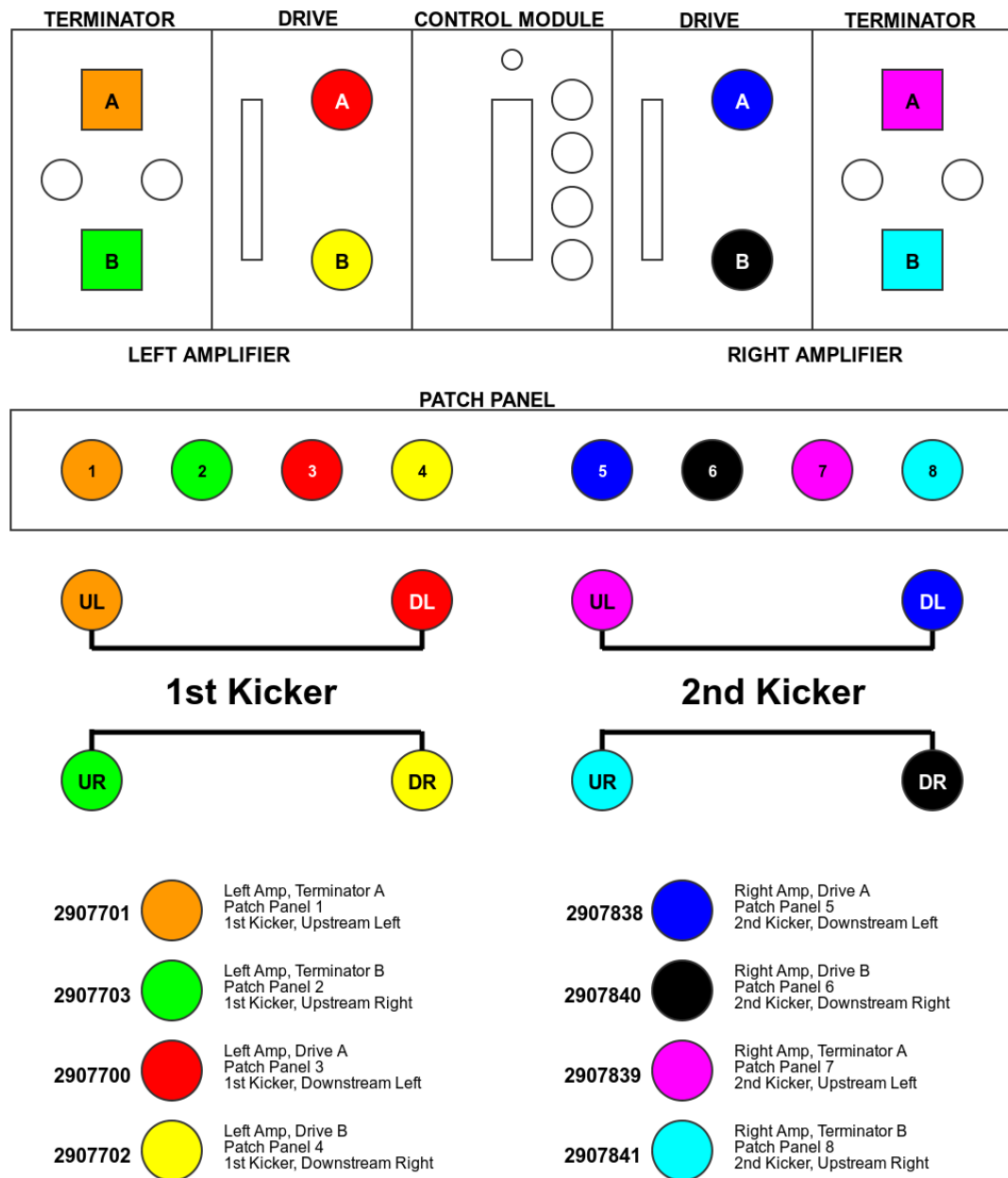


Figure 1.3: Cabling setup for cables between the amplifier and kickers.

Amplifier Port	Output at +1 V Input
LA	$+416 \pm 3$ V
LB	-453 ± 3 V
RA	-426 ± 3 V
RB	$+409 \pm 3$ V

Table 1.1: Feedforward results using combined data from 20th November 2015.

output Voltage using the approximate conversion factor of 115. All four amplifier outputs are shown (one for each strip of the two kickers). The plotted values are means taken across a 480 ns central part of the whole 1400 ns [TODO: Check - looks more like 1500 ns in data] output pulse.

The relative polarity of the four outputs is equivalent to what would be sent to the kickers during PFF operation, with opposite polarity of the L and R amplifier outputs sent to each kicker, so that the beam is kicked in opposite directions by each kicker with the second kicker then closing the orbit bump created by the first. Within each side of the amplifier the A and B outputs (sent to each side of the kicker) also have opposite polarity, necessary to create the potential difference across the strips within each kicker that creates the deflecting field for the beam. The relative polarity of the A and B outputs is fixed in the amplifier design and can not be controlled via the FONT5a board.

The response of the amplifier is highly linear in the region between ± 1.2 V sent to the amplifier. Outside this range the amplifier clearly begins to enter saturation, in particular above input voltages of ± 1.7 V. The linear fits shown include only the points between ± 1.2 V, excluding the first and last three points in the scan of input voltages, in order to not be biased by the effects of saturation.

Figure 1.5 shows the residuals between the linear fit and the real amplifier output across the full range of input voltages. By looking at the residuals a slight deviation from linearity in the ± 1.2 V range is also visible, although this the maximum difference is only 10 V or a 3% relative error. At the maximum input voltage of ± 2 V the difference between the real output and the amplitude expected if the response was linear across the full range rises above 150 V, or a relative error of more than 25%. For example, the RB output at an input voltage of +2 V is 605 V but the fitted response gives 769 V, a difference of 164 V or 27%.

The effects of amplifier saturation are not taken in to account in the PFF algorithm on the FONT5a board, in which the DAC output is linearly dependent on the input phase (voltage from the phase monitor mixer signal) across the full range. The applied correction to the downstream phase will therefore be non-optimal when the DAC output calculated by the PFF algorithm is above an absolute value of 2500 counts (1.2 V sent to the amplifier). [TODO: Calculate how significant later?]

Differences in the gradient and peak output - real or just monitoring calibration? If real effect on PFF - difference between kickers means non-closed orbit. Difference between strips just changes phase vs. input voltage, no issue as long as linear.

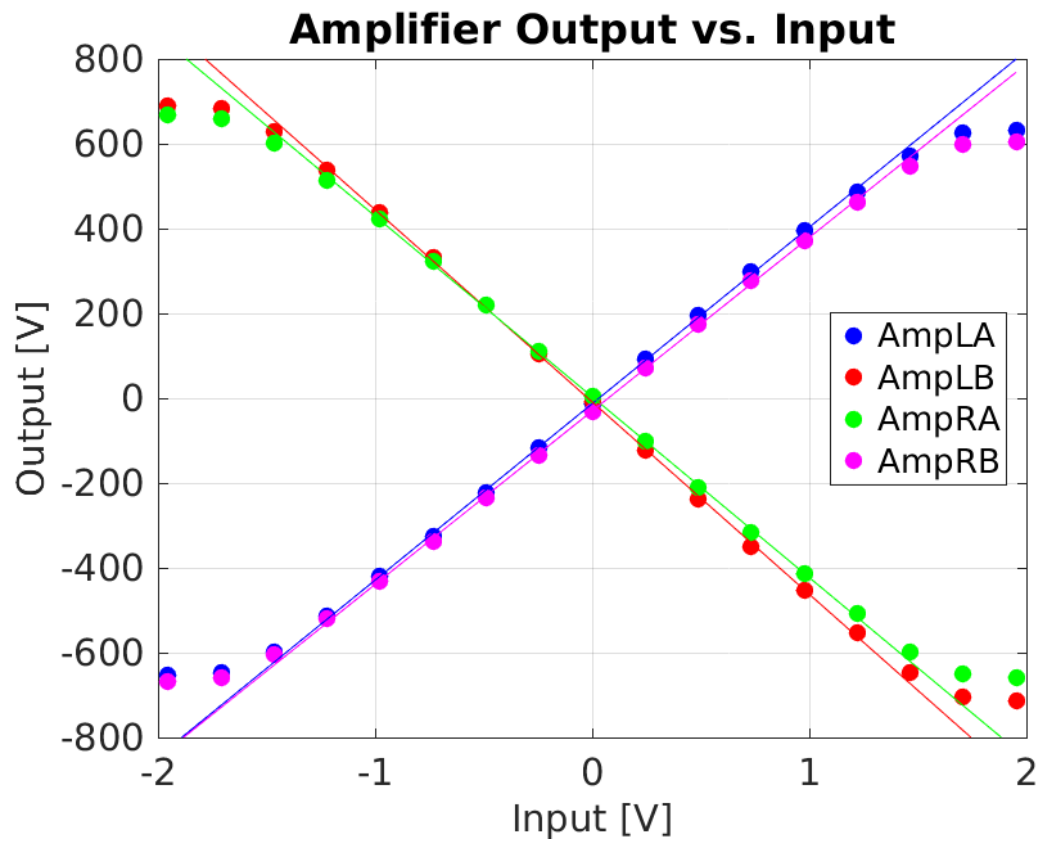


Figure 1.4: Amplifier output vs. input.

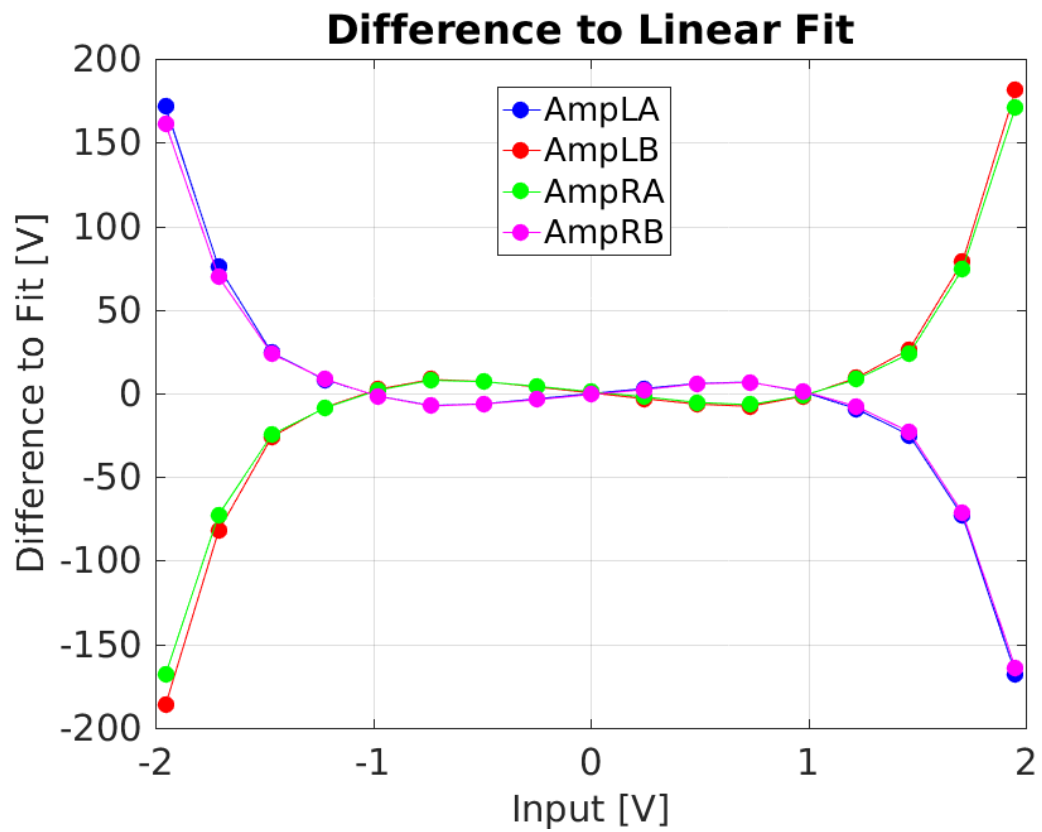


Figure 1.5: Residual between amplifier output and linear fit.

<http://accelconf.web.cern.ch/accelconf/ipac2011/papers/tupc007.pdf> 1.4 kV to each strip
= 1 mrad kick at 150 MeV 1.26 kV to each strip = 1 mrad kick at 135 MeV

1.2.4 Shape

1.2.5 Bandwidth

1.3 Data Acquisition and Signal Processing

1.3.1 SiS Digitiser Setup

(already discussed in ph mon chapter)

1.3.2 Acquisition Tools

1.3.3 Monitoring Tools

Online display

1.3.4 Time Alignment of Signals

1.3.5 Definition of Zero Phase

1.4 Kicker and Optics Performance Verification

1.4.1 Correction Range

Scan and comparison to expectation from optics.

Effect on correction.

Optics: 0.7m R52 - 10 degrees for 1mrad kick

1.4.2 Linearity

1.4.3 Orbit Closure

1.4.4 Shape

Shape of FF kick on BPMs vs. shape of upstream phase

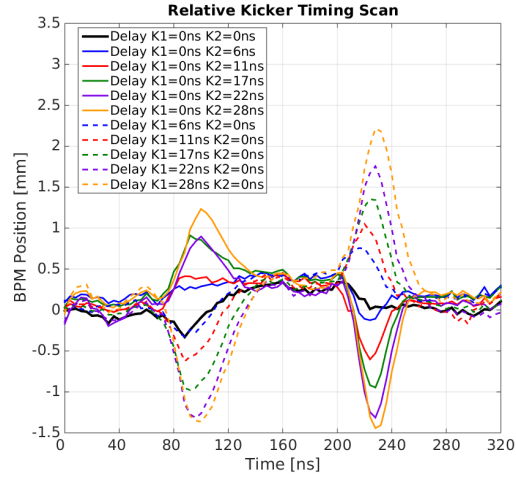


Figure 1.6: Traces relative timing scan.

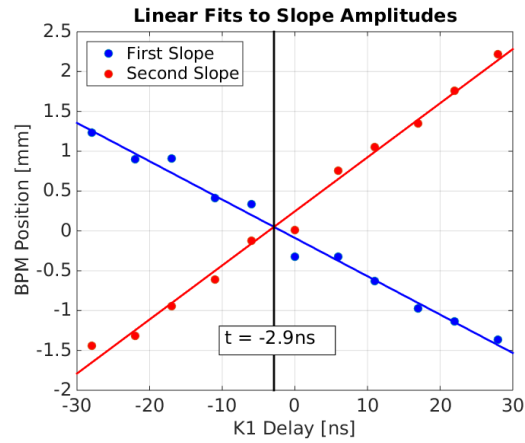


Figure 1.7: Relative timing scan - fit to rising/falling edge.

1.5 Correction Output Timing

1.5.1 Latency

1.5.2 Absolute Timing

Using Beam Pickup

Using BPMs

1.5.3 Relative Kicker Timing