EE-245, Digital Systems
Pin Assignments for DE-10 Lite

Table 3-3 Pin Assignment of Push-buttons

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY0	PIN_B8	Push-button[0]	3.3 V SCHMITT TRIGGER"
KEY1	PIN_A7	Push-button[1]	3.3 V SCHMITT TRIGGER"

Table 3-4 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTL

Table 3-5 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTL

7-Segment Displays:

6 digits with 7 segments and one decimal point on each display. Segments are assigned as shown below. Pin assignments for each segment on each digit follow.

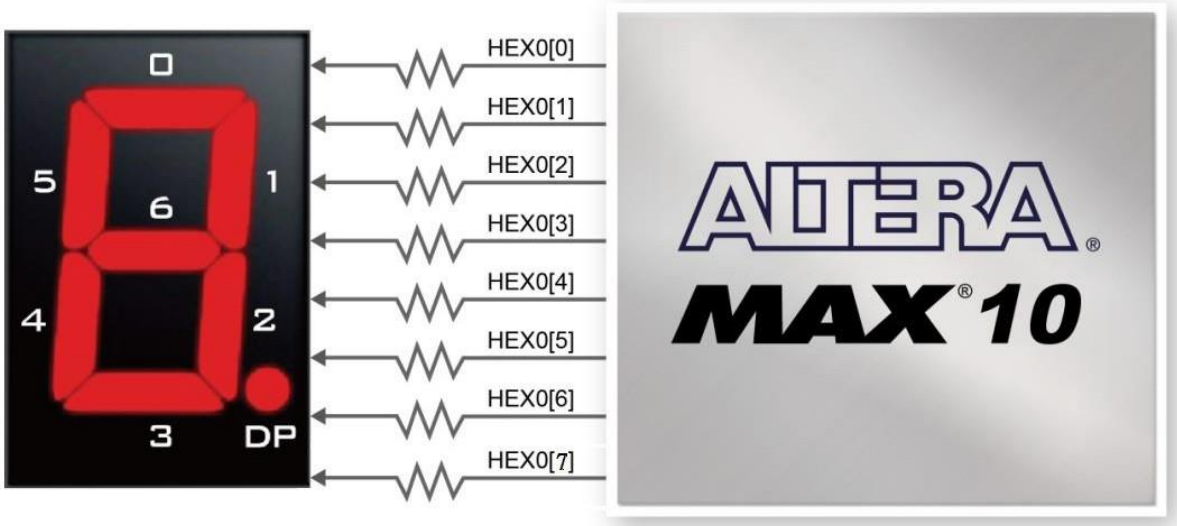

Figure 3-17 Connections between the 7-segment display HEX0 and the MAX 10 FPGA

Table 3-6 Pin Assignment of 7-segment Displays

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX00	PIN_C14	Seven Segment Digit 0[0]	3.3-V LVTTL
HEX01	PIN_E15	Seven Segment Digit 0[1]	3.3-V LVTTL
HEX02	PIN_C15	Seven Segment Digit 0[2]	3.3-V LVTTL
HEX03	PIN_C16	Seven Segment Digit 0[3]	3.3-V LVTTL
HEX04	PIN_E16	Seven Segment Digit 0[4]	3.3-V LVTTL
HEX05	PIN_D17	Seven Segment Digit 0[5]	3.3-V LVTTL
HEX06	PIN_C17	Seven Segment Digit 0[6]	3.3-V LVTTL
HEX07	PIN_D15	Seven Segment Digit 0[7], DP	3.3-V LVTTL
HEX10	PIN_C18	Seven Segment Digit 1[0]	3.3-V LVTTL
HEX11	PIN_D18	Seven Segment Digit 1[1]	3.3-V LVTTL
HEX12	PIN_E18	Seven Segment Digit 1[2]	3.3-V LVTTL

Table 3-6, Pin Assignment of 7-segment Displays (cont.)

HEX13	PIN_B16	Seven Segment Digit 1[3]	3.3-V LVTTL
HEX14	PIN_A17	Seven Segment Digit 1[4]	3.3-V LVTTL
HEX15	PIN_A18	Seven Segment Digit 1[5]	3.3-V LVTTL
HEX16	PIN_B17	Seven Segment Digit 1[6]	3.3-V LVTTL
HEX17	PIN_A16	Seven Segment Digit 1[7] , DP	3.3-V LVTTL
HEX20	PIN_B20	Seven Segment Digit 2[0]	3.3-V LVTTL
HEX21	PIN_A20	Seven Segment Digit 2[1]	3.3-V LVTTL
HEX22	PIN_B19	Seven Segment Digit 2[2]	3.3-V LVTTL
HEX23	PIN_A21	Seven Segment Digit 2[3]	3.3-V LVTTL
HEX24	PIN_B21	Seven Segment Digit 2[4]	3.3-V LVTTL
HEX25	PIN_C22	Seven Segment Digit 2[5]	3.3-V LVTTL
HEX26	PIN_B22	Seven Segment Digit 2[6]	3.3-V LVTTL
HEX27	PIN_A19	Seven Segment Digit 2[7] , DP	3.3-V LVTTL
HEX30	PIN_F21	Seven Segment Digit 3[0]	3.3-V LVTTL
HEX31	PIN_E22	Seven Segment Digit 3[1]	3.3-V LVTTL
HEX32	PIN_E21	Seven Segment Digit 3[2]	3.3-V LVTTL
HEX33	PIN_C19	Seven Segment Digit 3[3]	3.3-V LVTTL
HEX34	PIN_C20	Seven Segment Digit 3[4]	3.3-V LVTTL
HEX35	PIN_D19	Seven Segment Digit 3[5]	3.3-V LVTTL
HEX36	PIN_E17	Seven Segment Digit 3[6]	3.3-V LVTTL
HEX37	PIN_D22	Seven Segment Digit 3[7] , DP	3.3-V LVTTL
HEX40	PIN_F18	Seven Segment Digit 4[0]	3.3-V LVTTL
HEX41	PIN_E20	Seven Segment Digit 4[1]	3.3-V LVTTL
HEX42	PIN_E19	Seven Segment Digit 4[2]	3.3-V LVTTL
HEX43	PIN_J18	Seven Segment Digit 4[3]	3.3-V LVTTL
HEX44	PIN_H19	Seven Segment Digit 4[4]	3.3-V LVTTL
HEX45	PIN_F19	Seven Segment Digit 4[5]	3.3-V LVTTL
HEX46	PIN_F20	Seven Segment Digit 4[6]	3.3-V LVTTL
HEX47	PIN_F17	Seven Segment Digit 4[7] , DP	3.3-V LVTTL
HEX50	PIN_J20	Seven Segment Digit 5[0]	3.3-V LVTTL
HEX51	PIN_K20	Seven Segment Digit 5[1]	3.3-V LVTTL
HEX52	PIN_L18	Seven Segment Digit 5[2]	3.3-V LVTTL
HEX53	PIN_N18	Seven Segment Digit 5[3]	3.3-V LVTTL
HEX54	PIN_M20	Seven Segment Digit 5[4]	3.3-V LVTTL
HEX55	PIN_N19	Seven Segment Digit 5[5]	3.3-V LVTTL
HEX56	PIN_N20	Seven Segment Digit 5[6]	3.3-V LVTTL
HEX57	PIN_L19	Seven Segment Digit 5[7] , DP	3.3-V LVTTL

Table 3-7 Show all Pin Assignment of Expansion Headers

Signal Name	FPGA Pin No.	Description	I/O Standard
GPIO_0	PIN_V10	GPIO Connection [0]	3.3-V LVTTL
GPIO_1	PIN_W10	GPIO Connection [1]	3.3-V LVTTL
GPIO_2	PIN_V9	GPIO Connection [2]	3.3-V LVTTL
GPIO_3	PIN_W9	GPIO Connection [3]	3.3-V LVTTL
GPIO_4	PIN_V8	GPIO Connection [4]	3.3-V LVTTL
GPIO_5	PIN_W8	GPIO Connection [5]	3.3-V LVTTL
GPIO_6	PIN_V7	GPIO Connection [6]	3.3-V LVTTL
GPIO_7	PIN_W7	GPIO Connection [7]	3.3-V LVTTL
GPIO_8	PIN_W6	GPIO Connection [8]	3.3-V LVTTL
GPIO_9	PIN_V5	GPIO Connection [9]	3.3-V LVTTL
GPIO_10	PIN_W5	GPIO Connection [10]	3.3-V LVTTL
GPIO_11	PIN_AA15	GPIO Connection [11]	3.3-V LVTTL
GPIO_12	PIN_AA14	GPIO Connection [12]	3.3-V LVTTL
GPIO_13	PIN_W13	GPIO Connection [13]	3.3-V LVTTL
GPIO_14	PIN_W12	GPIO Connection [14]	3.3-V LVTTL
GPIO_15	PIN_AB13	GPIO Connection [15]	3.3-V LVTTL
GPIO_16	PIN_AB12	GPIO Connection [16]	3.3-V LVTTL
GPIO_17	PIN_Y11	GPIO Connection [17]	3.3-V LVTTL
GPIO_18	PIN_AB11	GPIO Connection [18]	3.3-V LVTTL
GPIO_19	PIN_W11	GPIO Connection [19]	3.3-V LVTTL
GPIO_20	PIN_AB10	GPIO Connection [20]	3.3-V LVTTL
GPIO_21	PIN_AA10	GPIO Connection [21]	3.3-V LVTTL
GPIO_22	PIN_AA9	GPIO Connection [22]	3.3-V LVTTL
GPIO_23	PIN_Y8	GPIO Connection [23]	3.3-V LVTTL
GPIO_24	PIN_AA8	GPIO Connection [24]	3.3-V LVTTL
GPIO_25	PIN_Y7	GPIO Connection [25]	3.3-V LVTTL
GPIO_26	PIN_AA7	GPIO Connection [26]	3.3-V LVTTL
GPIO_27	PIN_Y6	GPIO Connection [27]	3.3-V LVTTL
GPIO_28	PIN_AA6	GPIO Connection [28]	3.3-V LVTTL
GPIO_29	PIN_Y5	GPIO Connection [29]	3.3-V LVTTL
GPIO_30	PIN_AA5	GPIO Connection [30]	3.3-V LVTTL
GPIO_31	PIN_Y4	GPIO Connection [31]	3.3-V LVTTL
GPIO_32	PIN_AB3	GPIO Connection [32]	3.3-V LVTTL
GPIO_33	PIN_Y3	GPIO Connection [33]	3.3-V LVTTL
GPIO_34	PIN_AB2	GPIO Connection [34]	3.3-V LVTTL
GPIO_35	PIN_AA2	GPIO Connection [35]	3.3-V LVTTL

Table 3-8 Pin Assignments for Arduino Uno Expansion Header connector

Schematic Signal Name	FPGA Pin No.	Description	Specific features For Arduino	I/O Standard
Arduino_IO0	PIN_AB5	Arduino IO0	RXD	3.3-V LVTTL
Arduino_IO1	PIN_AB6	Arduino IO1	TXD	3.3-V LVTTL
Arduino_IO2	PIN_AB7	Arduino IO2		3.3-V LVTTL
Arduino_IO3	PIN_AB8	Arduino IO3		3.3-V LVTTL
Arduino_IO4	PIN_AB9	Arduino IO4		3.3-V LVTTL
Arduino_IO5	PIN_Y10	Arduino IO5		3.3-V LVTTL
Arduino_IO6	PIN_AA11	Arduino IO6		3.3-V LVTTL
Arduino_IO7	PIN_AA12	Arduino IO7		3.3-V LVTTL
Arduino_IO8	PIN_AB17	Arduino IO8		3.3-V LVTTL
Arduino_IO9	PIN_AA17	Arduino IO9		3.3-V LVTTL
Arduino_IO10	PIN_AB19	Arduino IO10	SS	3.3-V LVTTL
Arduino_IO11	PIN_AA19	Arduino IO11	MOSI	3.3-V LVTTL
Arduino_IO12	PIN_Y19	Arduino IO12	MISO	3.3-V LVTTL
Arduino_IO13	PIN_AB20	Arduino IO13	SCK	3.3-V LVTTL
Arduino_IO14	PIN_AB21	Arduino IO14	SDA	3.3-V LVTTL
Arduino_IO15	PIN_AA20	Arduino IO15	SCL	3.3-V LVTTL
ARDUINO_RESET_N	PIN_F16	Reset signal, low active.		3.3 V SCHMITT TRIGGER"

Table 3-11 Pin Assignment of VGA

Signal Name	FPGA Pin No.	Description	I/O Standard
VGA_R0	PIN_AA1	VGA Red[0]	3.3-V LVTTL
VGA_R1	PIN_V1	VGA Red[1]	3.3-V LVTTL
VGA_R2	PIN_Y2	VGA Red[2]	3.3-V LVTTL
VGA_R3	PIN_Y1	VGA Red[3]	3.3-V LVTTL
VGA_G0	PIN_W1	VGA Green[0]	3.3-V LVTTL
VGA_G1	PIN_T2	VGA Green[1]	3.3-V LVTTL
VGA_G2	PIN_R2	VGA Green[2]	3.3-V LVTTL
VGA_G3	PIN_R1	VGA Green[3]	3.3-V LVTTL
VGA_B0	PIN_P1	VGA Blue[0]	3.3-V LVTTL
VGA_B1	PIN_T1	VGA Blue[1]	3.3-V LVTTL
VGA_B2	PIN_P4	VGA Blue[2]	3.3-V LVTTL
VGA_B3	PIN_N2	VGA Blue[3]	3.3-V LVTTL
VGA_HS	PIN_N3	VGA Horizontal sync	3.3-V LVTTL
VGA_VS	PIN_N1	VGA Vertical sync	3.3-V LVTTL

Table 3-12 Pin Assignment of SDRAM

Signal Name	FPGA Pin No.	Description	I/O Standard
DRAM_ADDR0	PIN_U17	SDRAM Address[0]	3.3-V LVTTL
DRAM_ADDR1	PIN_W19	SDRAM Address[1]	3.3-V LVTTL
DRAM_ADDR2	PIN_V18	SDRAM Address[2]	3.3-V LVTTL
DRAM_ADDR3	PIN_U18	SDRAM Address[3]	3.3-V LVTTL
DRAM_ADDR4	PIN_U19	SDRAM Address[4]	3.3-V LVTTL
DRAM_ADDR5	PIN_T18	SDRAM Address[5]	3.3-V LVTTL
DRAM_ADDR6	PIN_T19	SDRAM Address[6]	3.3-V LVTTL
DRAM_ADDR7	PIN_R18	SDRAM Address[7]	3.3-V LVTTL
DRAM_ADDR8	PIN_P18	SDRAM Address[8]	3.3-V LVTTL
DRAM_ADDR9	PIN_P19	SDRAM Address[9]	3.3-V LVTTL
DRAM_ADDR10	PIN_T20	SDRAM Address[10]	3.3-V LVTTL
DRAM_ADDR11	PIN_P20	SDRAM Address[11]	3.3-V LVTTL
DRAM_ADDR12	PIN_R20	SDRAM Address[12]	3.3-V LVTTL
DRAM_DQ0	PIN_Y21	SDRAM Data[0]	3.3-V LVTTL
DRAM_DQ1	PIN_Y20	SDRAM Data[1]	3.3-V LVTTL
DRAM_DQ2	PIN_AA22	SDRAM Data[2]	3.3-V LVTTL
DRAM_DQ3	PIN_AA21	SDRAM Data[3]	3.3-V LVTTL
DRAM_DQ4	PIN_Y22	SDRAM Data[4]	3.3-V LVTTL
DRAM_DQ5	PIN_W22	SDRAM Data[5]	3.3-V LVTTL
DRAM_DQ6	PIN_W20	SDRAM Data[6]	3.3-V LVTTL
DRAM_DQ7	PIN_V21	SDRAM Data[7]	3.3-V LVTTL
DRAM_DQ8	PIN_P21	SDRAM Data[8]	3.3-V LVTTL
DRAM_DQ9	PIN_J22	SDRAM Data[9]	3.3-V LVTTL
DRAM_DQ10	PIN_H21	SDRAM Data[10]	3.3-V LVTTL
DRAM_DQ11	PIN_H22	SDRAM Data[11]	3.3-V LVTTL
DRAM_DQ12	PIN_G22	SDRAM Data[12]	3.3-V LVTTL
DRAM_DQ13	PIN_G20	SDRAM Data[13]	3.3-V LVTTL
DRAM_DQ14	PIN_G19	SDRAM Data[14]	3.3-V LVTTL
DRAM_DQ15	PIN_F22	SDRAM Data[15]	3.3-V LVTTL
DRAM_BA0	PIN_T21	SDRAM Bank Address[0]	3.3-V LVTTL
DRAM_BA1	PIN_T22	SDRAM Bank Address[1]	3.3-V LVTTL
DRAM_LDQM	PIN_V22	SDRAM byte Data Mask[0]	3.3-V LVTTL
DRAM_UDQM	PIN_J21	SDRAM byte Data Mask[1]	3.3-V LVTTL
DRAM_RAS_N	PIN_U22	SDRAM Row Address Strobe	3.3-V LVTTL
DRAM_CAS_N	PIN_U21	SDRAM Column Address Strobe	3.3-V LVTTL
DRAM_CKE	PIN_N22	SDRAM Clock Enable	3.3-V LVTTL
DRAM_CLK	PIN_L14	SDRAM Clock	3.3-V LVTTL
DRAM_WE_N	PIN_V20	SDRAM Write Enable	3.3-V LVTTL
DRAM_CS_N	PIN_U20	SDRAM Chip Select	3.3-V LVTTL

Table 3-13 Pin Assignment of Accelerometer Sensor

Signal Name	FPGA Pin No.	Description	I/O Standard
GSENSOR_SDI	PIN_V11	I2C serial data SPI serial data input (SPI 4-wire) SPI serial data input and output (SPI 3-wire)	3.3-V LVTTL
GSENSOR_SDO	PIN_V12	SPI serial data output (SPI 4-wire) Alternate I2C address select	3.3-V LVTTL
GSENSOR_CS_n	PIN_AB16	I2C/SPI mode selection: 1: SPI idle mode / I2C communication enabled 0: SPI communication mode / I2C disabled SPI Chip Select	3.3-V LVTTL
GSENSOR_SCLK	PIN_AB15	I2C serial clock SPI serial clock (3- and 4-wire)	3.3-V LVTTL
GSENSOR_INT1	PIN_Y14	Interrupt pin 1	3.3-V LVTTL
GSENSOR_INT2	PIN_Y13	Interrupt pin 2	3.3-V LVTTL