838L - Milestone 1

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1 Literature Review

2 Alterations to the Proposal

Rather than leveraging the CIRCT framework, we now plan on having our compiler emit Calyx IR. This IR will then be lowered into Verilog, which we can show as a timing simulation and potentially deploy to an FPGA. We decided to use Calyx as it has a more mature build system, and is not as experimental/development focused as CIRCT is right now.

3 Concrete Steps

So far, we have built sample circuits with Calyx IR, including a 4 bit adder circuit. We have simulated this circuit using Icarus, and are able to view the timing simulations in GTKWave.