ELEC 5200/ELEC 6200 Computer Architecture and Design
Class Test 2, Solution, March 29, 2019 **Total 60 points**
Broun 235, 11:00-11:50AM

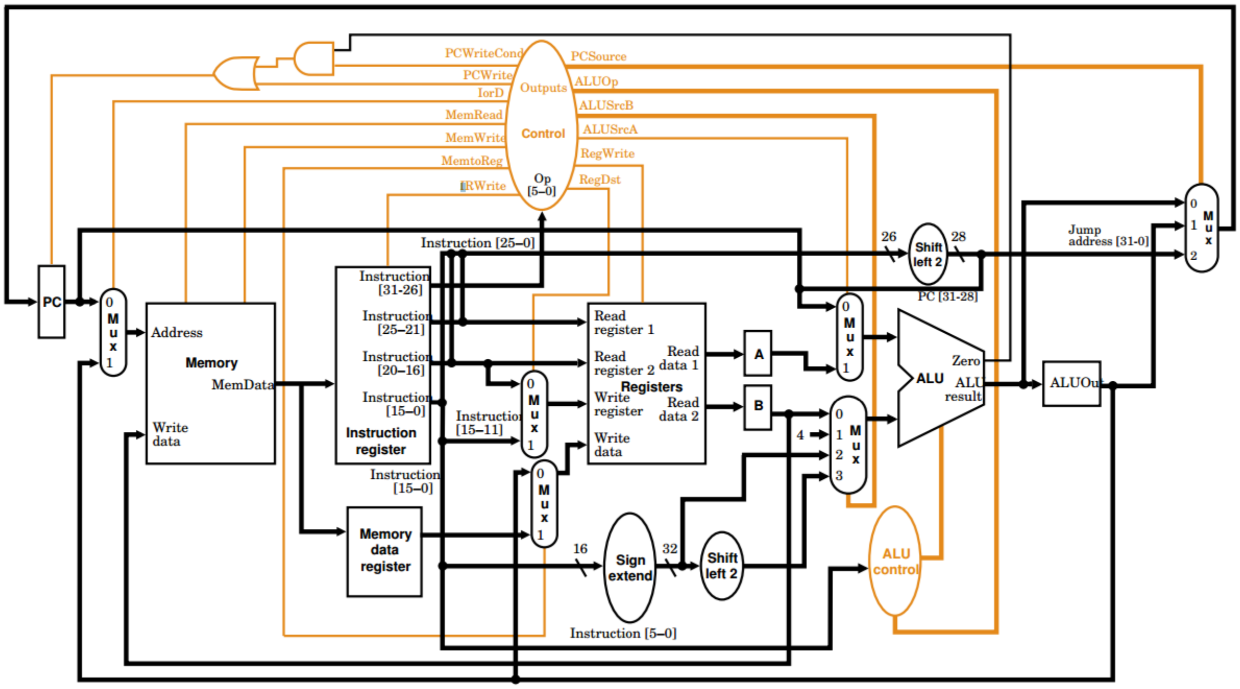
Instructions: Attempt all problems. Write your answers in the provided space. Be sure to review your answers before turning them in. Thank you and good luck!

1. What is the ideal CPI of a single cycle processor? A pipelined processor? Why is one design desirable over the other? (2 points)

Answer:

The ideal CPI for both designs is 1. They both complete an instruction in (approximately) one cycle on average, but the cycle time for a pipelined processor is generally shorter. Thus the pipelined design can complete more instructions per second compared to the single cycle design.

For questions 2 through 4 use the multi-cycle datapath diagram provided below:



2. List the 5 execution steps AND provide a brief explanation as to what happens in each step. (5 points)

Answer:

Step 1: Instruction Fetch – The instruction is read from memory and stored in the instruction register. The PC value is also incremented by one instruction and stored in preparation for the next instruction fetch.

Step 2: Instruction Decode – The opcode is sent to the control unit where the control signals necessary for the rest of the instruction steps are generated. Register operands are fetched and the branch target address is also calculated during this stage.

Step 3: Instruction Execution – The is the primary stage where the ALU is used. R-type instructions use the ALU to generate arithmetic results, Load/Store word instructions use the ALU for memory address calculations. Branch instructions use the ALU for operand comparison, while Jump instructions simply write the PC with the jump target address.

Step 4: Memory Access – Load and Store word instructions access memory.

Step 5: Write Back – Results from R-type (ALU) instructions and Load word instructions are written to the destination register in the register file.

3. The RTL for Step 1 is:

```
IR = Memory[PC];
PC = PC + 4;
```

Fill in the values that are required for the following control signals: (4 points)

Answer:

ALUSrcA = **0**   ALUSrcB = **01**

PCSource = **00**   IorD = **0**

4. For a single cycle processor X assume the following:

200 ps for memory operations
100 ps for ALU operations
50 ps for register file access

(disregard the delay for all other datapath components such as multiplexors and control unit)

If both a single cycle datapath X and the multi-cycle datapath Y (as shown above) are running the same benchmark consisting of the following instruction mix:

20% lw, 10% sw, 11% branch, 3% jump, 56% ALU instr

Calculate (show your work):

(a) The cycle time for each processor. (5 points)

Answer:

For the single cycle processor the cycle time is determined by the longest instruction, which is lw.

The cycle time of lw contains the delay of the following units:
lw := IF + REG READ + ALU + MEM + REG WRITE
= 200ps + 50ps + 100ps + 200ps + 50ps = 600ps

For the multicycle datapath the cycle time is determined by the individual step with the longest delay. The steps where memory is accessed (instruction fetch or data read/write) result in the longest delay. Therefore, the cycle time for the multicycle datapath is 200ps.

(b) The average instruction execution time for each processor. (4 points)

Answer:

To find the average instruction execution time we must first find CPI and then multiply if by the clock cycle.

$\text{CPI}_{\text{SINGLE}}$ for any single cycle processor is 1. Therefore the average instruction execution time for the single cycle processor is:

$T_{\text{EX-SINGLE}}$ = 600ps * 1 = 600ps

The CPI for the multicycle datapath can be calculated using the benchmark instruction mix along with the number of cycles required for each instruction type.

Recall that: lw = 5 cycles, sw & ALU = 4 cycles, jump & branch = 3 cycles

$\text{CPI}_{\text{MULTI}}$ = 0.20*5 + 0.10*4 + 0.11*3 + 0.03*3 + 0.56*4 = 4.06

The average instruction execution time for the multicycle processor is:
$T_{\text{EX-MULTI}}$ = 200ps * 4.06 = 812ps

(c) The performance ratio (using results from part b) for the datapaths. (2 points)

Answer:

The performance ratio of single cycle to multicycle is:

$$\frac{T_{EX-SINGLE}}{T_{EX-MULTI}} = \frac{600\ ps}{812\ ps} = 0.7389$$

5. Consider the MIPS pipelined architecture studied in class. How is a stall/bubble implemented in hardware? (give specific signals/signal groups and their required values). (6 points)

Answer:

- **All control signal outputs in the decode stage are forced to 0.** In class this was implemented by the hazard detection unit controlling a mux input which either selected the control signals generated from the control unit or all 0s.
- **Prevent the PC from changing.** In class this was implemented by the hazard detection unit generating a PCWrite signal with a value of 0.
- **Prevent the IF/ID pipeline register from changing.** In class this was implemented by the hazard detection unit generating an $\text{IF/ID}_{\text{Write}}$ signal which is deasserted (assumed to be a value of 0).

6. Draw a pipeline diagram for the code below, assuming the MIPS pipeline that we used in class. Show stalls and/or forwarding where needed. (5 points)

```
add $s1, $s3, $s4
lw $v0, 0($s1)
sub $v0, $v0, $s1
```

Answer:

CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8	CC9	CC10	Instr
FE	ID	EX	MEM	WB						add $s1, $s3, $s4
	FE	ID	EX	MEM	WB					lw $v0, 0($s1)
		FE	ID	BUB	BUB	BUB				sub $v0, $v0, $s0 / bubble
				ID	EX	MEM	WB			sub $v0, $v0, $s0

7. Consider a processor with a 7-stage pipeline. Assume that branches are resolved in the sixth stage. Assume that 20% of instructions are branches.

(a) How many instructions of wasted work are there per branch misprediction on this machine? (1 point)

Answer:

5 instructions are wasted.

(b) Assume ***N*** instructions are on the correct path of a program and assume a branch predictor accuracy of ***A***. Write the equation for the number of instructions that are fetched on this machine in terms of ***N*** and ***A***. (5 points. Please show your work for full credit.)

Answer:

Note that if you assumed the wrong number of instructions in Part (a), you will only be marked wrong for this in Part (a). You can still get full credit on this part.

Correct path instructions = N

Incorrect path instructions = N(0.2)(1 - A)5 = N(1 - A)

Total fetched instructions = Correct path instructions + Incorrect path instructions
=N + N(1 - A)
= N(2 - A)

8. Describe the two types of **locality** exhibited in memory accesses. (2 points)

Answer:

Temporal locality – Memory addresses accessed are likely to be accessed again soon. (ie locality in time)

Spatial locality – Items located at addresses near an item recently accessed are likely to also be accessed soon. (ie locality in address space)

9. How many transistors in an SRAM cell? How many in a DRAM cell? Why is this relevant? (3 points)

Answer:

An SRAM cell has **6 transistors** while a DRAM cell has **1 transistor** (and a capacitor). We can therefore fit **more bits of DRAM in a given chip area** than bits of SRAM. However, SRAM is faster than DRAM (due to the necessity of DRAM refresh) and therefore tradeoffs are required in memory system design.

10. Consider a computer system with 64KB of byte addressed main memory and a 256 byte cache, using 32-bit words. Assume that the cache line size is 8 bytes:

(a) Show the format in which a memory address for the above system is subdivided for use with a direct mapped cache (including the number of bits for each memory address section). (5 points)

Answer:

A 256 byte cache contains 256 / 4 = 64 words where each word contains 4 bytes. Each cache line / block contains 2 words (8 bytes). Therefore the cache contains 64 / 2 = 32 blocks total. With 32 cache lines / blocks we need 2^5 (32) indicies. We therefore require an index of 5 bits, a byte offset of 2 bits, and a block offset of 1 bit. 64 KB of byte addressed main memory requires 2^{16} address bits. Therefore the memory address has the following format:

Tag	Index	Block offset	Byte offset
8 bits	5 bits	1 bit	2 bits

(b) Into what cache line would the word with the following address be stored: **0001 0001 0001 1000** (1 point)

Answer:

The address yields a cache index of 00011. Therefore the data with the given address would be stored in the fourth cache line/block (ie the block with the index of 00011).

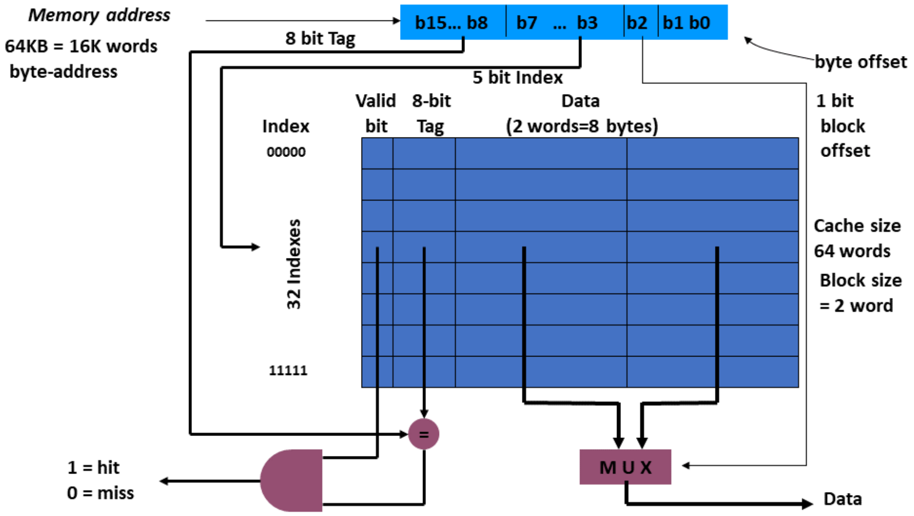
(c) Suppose the word from part b (located at address 0001 0001 0001 1000) is stored in the cache. What are the addresses of other words stored along with it (if any)? (2 points)

Answer:

One additional word with the address of 0001 0001 0001 1100 will be stored in the cache line/block. This is because both the tag and index of the memory address are the same, indicating that it is located in the same block as the target address.

(d) Draw a diagram of the direct mapped cache hardware organization and show briefly how the different fields of the address are used/interpreted. (8 points)

Answer:



11. (**Bonus Question**) What are the primary benefits and/or drawbacks discussed in class of a pipeline with a large number of stages? (4 points)

Answer:

A pipeline with more stages generally has a faster clock cycle (ie higher frequency) due to a smaler worst-case delay in the combinational logic. However, a pipeline with many stages tends to have a higher branch penalty.