ELEC 5200-001/6200-001 (Spring 2019)
Homework 6 - Solution
Assigned 04/01/19, due 04/08/19
(15 points possible)

Problem 1: Consider a 16-bit address space with the following list of memory addresses, given as word addresses.

3, 182, 16, 40, 181, 44, 17, 200, 180, 75, 2, 41

(a) For each of the above memory references, provide the full 16-bit binary memory **byte** address along with the binary tag(s) and index for a three way set associative cache with two-word blocks. The cache holds a total of 24 words. Assuming these addresses are again accessed sequentially, determine if each memory access is a hit or miss assuming the cache is initially empty. (4 points)

Word	16-Bit Byte Address	Tag	Index	Access
3	0000 0000 0000 1100	0000 0000 000	01	Miss
182	0000 0010 1101 1000	0000 0010 110	11	Miss
16	0000 0000 0100 0000	0000 0000 010	00	Miss
40	0000 0000 1010 0000	0000 0000 101	00	Miss
181	0000 0010 1101 0100	0000 0010 110	10	Miss
44	0000 0000 1011 0000	0000 0000 101	10	Miss
17	0000 0000 0100 0100	0000 0000 010	00	Hit
200	0000 0011 0010 0000	0000 0011 001	00	Miss
180	0000 0010 1101 0000	0000 0010 110	10	Hit
75	0000 0001 0010 1100	0000 0001 001	01	Miss
2	0000 0000 0000 1000	0000 0000 000	01	Hit
41	0000 0000 1010 0100	0000 0000 101	00	Hit

Problem 2: Consider a processor that uses a 32-bit virtual memory address. The memory consists of 32-bit words and is byte addressable. Determine,

a. How many bytes the virtual memory can have? (1 point)

Answer: The virtual memory can have 2^{32} = 4GB.

b. If the page size is 128KB, then how many records should the page table hold? (1 point)

Answer:

Number of records in page table = Number of virtual pages = 4GB/128KB = 32K.

c. How much data space should physical memory have to hold 16K pages? (2 points)

Answer: Physical memory size = 128KB × 16K = 2GB.

d. How many bits of storage will be needed in a record of TLB? (2 points)

Answer:

A TLB record contains 1 valid bit, 1 dirty bit, 1 reference bit, page table index requiring $\log_2(32K)$, or 15 bits, and physical page number requiring $\log_2(16K)$, or 14 bits. Therefore, a TLB record should hold 1 + 1 + 1 + 15 + 14 = 32 bits.

Problem 3: Suppose a 4-way set associative cache has 64 blocks that are 8 bytes each. Show how to break the following address into the tag, index, & offset(s): (2 points)

Note: assume a 16 bit word size

0000 1000 0101 1100 0001 0001 0111 1001

Answer:

Tag	Index	Block offset	Byte offset
0 0001 0000 1011 1000 0010 0010	1111	00	1

Problem 3: Consider a processor that has a CPI of 3.0 assuming a perfect cache. If there are 1.4 memory accesses per instruction, a miss penalty of 20 cycles, and a miss rate of 5%, what is the effective CPI with the real cache?. (3 points)

Answer:

Recall that CPI stands for Clocks Per Instruction (or cycles per instruction). We are told that there are 1.4 memory access per instruction on average (when you take into account instruction fetches and data accesses). With no cache misses we have a CPI of 3.0. However, for 5% of these memory access we have a cache miss and have an additional number of cycles we have to wait due to miss penalty. To determine the effective CPI we must add this miss penalty to the ideal CPI. Therefore the effective CPI is:

$$CPI_{EFF} = \text{Ideal CPI} + \text{penalty} = 3.0 + (1.4 * 0.05 * 20) = 4.4$$