ELEC 5200-001/6200-001 (Spring 2019)
Homework 3 - Solution
Assigned 03/01/19, due 03/08/19

Problem 1: Execution times of hardware blocks of a single cycle datapath are as follows:

Program counter write	5ps
Multiplexer	2ps
Control	3ps
Register file read or write	15ps
Sign extension	2ps
Shift left by 2	2ps
Adder or ALU	20ps
Instruction/data memory read or write	20ps

All other hardware times can be neglected. Find a lower bound on the cycle time for the program counter. (7 points)

Answer:

The critical path is exercised by the lw instruction. Execution of instruction begins by writing of the program counter (PC). The lw instruction is executed as follows [items in brackets are concurrent with the previous item but take less time and therefore do not affect the critical path delay]:

Operation	**Hardware used**	**Time required**
PC written	PC write	5ps
Instruction fetch	Instruction memory	20ps
[Adder, PC+4]	[Adder in parallel with memory]	[20ps]
Register read	register file	15ps
[Immediate argument]	[(control or sign ext.) + multiplexer]	[5ps]
Address computation	ALU	20ps
Data memory read	Data memory	20ps
Mux, mem data to reg file	Multiplexer	2ps
Write register	register file	15ps
Total time		**97ps**

The clock cycle time for PC must not be less than 97ps.

Problem 2: Consider the hardware times of major units (all others being negligible) in a datapath as:

Memory access (read or write)	25ps
ALU	20ps
Register file (read or write)	15ps

Determine minimum clock cycle time, average CPI, and average instruction execution time for single-cycle and multi-cycle datapaths for the following program statistics:

10% lw, 10% sw, 40% register-type, 20% branch and 20% jump. (7 points)

Answer:

Single-cycle clock period (cycle time) is determined by the lw instruction, which activates the critical path:

Cycle time = memory + reg. file + ALU + memory + reg. file
= 25 + 15 + 20 + 25 + 15 = 100ps

Avg. CPI = 1

Avg. time/instruction = 100 × 1 = 100ps

Multi-cycle clock period (cycle time) is determined by the slowest hardware unit (memory in this case):

Cycle time = 25ps

Clock cycles used by instructions are 5 for lw, 4 for sw, 4 for r-type, 3 for branch and 3 for jump. Therefore,

Avg. CPI = 0.1×5 + 0.1×4 + 0.4×4 + 0.2×3 + 0.2×3 = 3.7

Avg. time/instruction = 25 × 3.7 = 92.5ps

The following table summarizes the results:

Datapath	Min cycle type (ps)	Avg. CPI	Avg time/inst (ps)
Single cycle	100	1	100
Multi-cycle	25	3.7	92.5

Problem 3:

(a) Suppose an operation involving register file, memory or ALU each takes 1 time unit. Neglecting the time of all other hardware, how much time will each MIPS instruction take on a single-cycle datapath? Consider R-type, lw, sw, beq and j instructions. (1 point)

Answer:

Each instruction will take 5 units of time on a single-cycle datapath.

(b) What will be the execution times for MIPS instructions on a 5-cycle multi-cycle datapath using a clock period of 1 time unit? (5 points)

Answer:

Times for MIPS instructions to run on a multi-cycle datapath are:

Load, ***lw***	5 time units
Store, ***sw***	4 time units
R-type, ***add, sub, etc.***	4 time units
Branch, ***beq, bne***	3 time units
Jump, ***j***	3 time units

(c) A program contains the following mix of instructions: lw 5%, sw 5%, r-type 70%, branch 10%, jump 10%.

What is the ratio of single-cycle CPU time to multicycle CPU time for running this program on these datapaths? (3 points)

$$\text{(c) CPU time ratio} = \frac{\text{Single-cycle (cycles per instruction} \times \text{cycle time)}}{\text{Multicycle (average cycles per instruction} \times \text{cycle time)}}$$

$$= \frac{1 \times 5}{(0.05\times5 + 0.05\times4 + 0.7\times4 + 0.1\times3 + 0.1\times3) \times1}$$

$$= (1 \times 5) / (3.85 \times1) = 1.299$$

Problem 4: Clock rates for single-cycle and multicycle datapaths are given as 1GHz and 5GHz, respectively. The following subroutine is used for estimating performance. The argument register $a0 contains a large positive integer and $a1 contains integer 1.

```
loop    sub     $a0, $a0, $a1
        beq     $a0, $0, done
        j       loop
done    jr      $31
```

Determine:

(a) Average cycles per instruction (CPI) for two datapaths. (7 points)

Answer:

CPI:

Single-cycle CPI = 1.0, because each instruction executes in one cycle.

The instruction mix for multicycle datapath is:

sub takes 4 cycles and is executed **a0** times
beq takes 3 cycles and is executed **a0** times
j takes 3 cycles and is executed **a0** – 1 times
jr takes 3 cycles and is executed once

Total number of instructions = 3**a0** – 1 + 1 = 3**a0**

Multicycle CPI = (4×**a0** + 3×**a0** + 3×**a0** – 3 + 3) / (3×**a0**)
= 10/3 = 3.333

(b) How much faster is the multicycle execution of the program (ratio of single-cycle to multicycle execution times)? (3 points)

Answer:

Execution time ratio:

The multicycle clock period is 0.2 ns and the single-cycle clock period is 1 ns.

Therefore,

Performance ratio = (single-cycle time) / (multicycle time)
= (1×3**a0**) / (0.2×3.333×3**a0**)
= 1.5