Notes for Spring 2006 – Below is part of an old final exam. The emphasis with this course was somewhat different, so irrelevant material was removed. Expect additional material on:

1. **As described before the 6 week exam (see calendar for Feb 13). In particular, you will need to write MIPS code/functions.**
2. **As described before the 12 week exam (see calendar for April 3)**
3. **Since 12 weeks: Caching, Virtual Memory, Pipelining, Multiprocessors, Ethics (Reverse Engineering & DMCA) – additional problems at end.**

Also, you will be given the following possible useful information – you should familiarize yourself with it in advance:

1. A copy of the single-cycle and multi-cycle datapaths are provided to you – see last page.

2. For function calls:
   Integer values are passed in $a0, $a1, $a2, $a3
   Floating point values are passed in $f12, $f14
   Integer values are returned in $v0
   Floating point values are returned in $f0.

3. ALU control
   ALUOp = 00 → ALU will Add
   ALUOp = 01 → ALU will Subtract
   ALUOp = 10 → ALU will perform action indicated by the instruction's function field

4. Single precision floating point numbers – bias is 127
   Double precision floating point numbers – bias is 1023

Computer Architecture
PRACTICE Final Exam

Name _____ Alpha _____

Section: 5200 6200 (circle one) **Note:**

This exam is closed-book, closed-notes.

No calculators are permitted.

Leave answers in fractional form.

To receive partial credit, show all work and make it legible.

Page 1 (10 Pts)	_____
Page 2 (6 Pts)	_____
Page 3 (10 Pts)	_____
Page 4 (17 Pts)	_____
Page 5 (18 Pts)	_____
Page 6 (11 Pts)	_____
Page 7 (14 Pts)	_____
Page 8 (7 Pts)	_____
Page 9 (7 Pts)	_____
TOTAL	_____

(1 pt) Define abstraction, with respect to its importance to computer architecture.

(5 pts) A compiler designer is trying to decide between two code segments for a particular machine. The hardware designers have provided the following data below about the CPI for each class, and the instruction counts being considered for each code sequence.

Class	CPI for this instruction class
A	2
B	3

	Instruction Counts for Instruction Classes	
Code sequence	A	B
1	3	5
2	7	2

How many cycles are required for each code sequence?

Code sequence #1:
Code sequence #2:

Which is faster and how by how much?

What is the CPI for each code sequence?

CPI for code sequence #1:
CPI for code sequence #2:

(1 pt) Define Instruction Set Architecture.

(1 pt) List the five classic components of a computer.

(2 pts) Explain the stored-program concept.

(6 pts) Consider the logic function with three inputs: A, B, and C.

Output D is true if at least one input is true
Output E is true if exactly two inputs are true
Output F is true only if all three inputs are true

(2 pts) Show the truth table for these three functions.

A	B	C	D	E	F

(2 pts) Show the Boolean equations for these three functions.

(2 pts) Show an implementation consisting of gates (invertors, AND, OR, NOR, etc). Connect your circuit to the provided feeds (input and output).

Input **Output**

A ____ ____ **D**

B ____ ____ **E**

C ____ ____ **F**

(1 pt) What does the MIPS register $ra hold? Why is it important?

(2 pts) Name the fields for R-format MIPS instruction and list their size (in bits).

(3 pts) List and provide a short description for the 3 pipelining hazards:

(2 pts) Fill in the following sentence:

Pipelining improves the performance by _____ instruction throughput, as opposed to _____ the execution time of an individual instruction.

(3 pts) Show MIPS assembly code that would implement the following high level language code. Use the following register assignments: A is $t0, B is $t1, C is $t2, D is $t4, R is $v3.

```
A = B + C – D + R;
```

(3 pts) List 3 of the addressing modes utilized in MIPS.

(2 pts) List the 4 design principles associated with Instruction Set Architectures. Provide a brief explanation (or example) of each of them.

(5 pts) For a multicycle datapath (provided on page 8), list the 5 execution steps **AND** provide a brief explanation as to what happens in each step:

(3 pts) Which modern pipelining technique includes launching multiple instructions in every pipeline stage? (Circle the correct answer).

Super pipelining **or** Superscalar **or** Dynamic pipelining

(3 pts) Fill in the following chart:

Associativity	**Location Method**	**Comparisons Needed**
Direct Mapped		
Set Associative		
Fully Associative		

(3 pts) Fill in the following sentence:

-A magnetic disk is composed of 1 to 15 _____, which are divided into numerous (1000 to 5000) _____ per surface, which are subdivided into 64 to 200 _____.

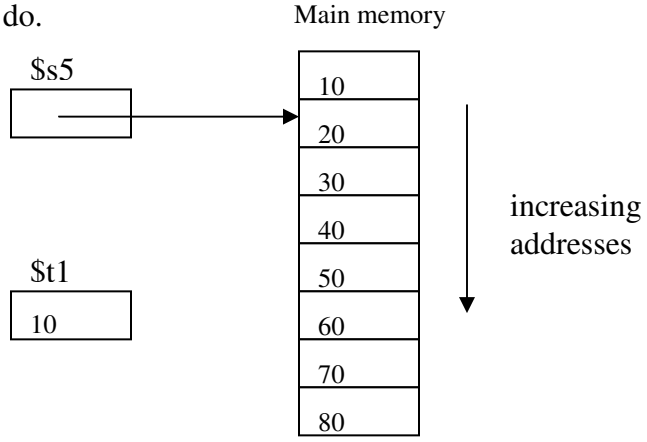
(1 pt) Floating point representation uses two's complement representation (Circle one) T F

(1 pt) When the immediate constant 1010 1010 1010 1010 is mapped to 32 bits, its value is 0000 0000 0000 0000 1010 1010 1010 1010 T F

(1 pt) Overflow has occurred when adding two negatives yields a _____ number.

(3 pts) Given that the base address of an array is stored in register $s5, and the size of each element is <u>one</u> <u>word</u>, show on the picture what will the following instruction do.

```
lw $t1, 16($s5)
```



(3 pts) Given the following bit pattern is a single precision floating point representation, what decimal number does it represent?

0011 1111 1111 0000 0000 0000 0000 0000

(2 pts) List 2 performance considerations for I/O systems.

(2 pts) What are the two writing strategies discussed in class/notes when there is a write "hit" in cache? Define each strategy.

(2 pts) Define spatial locality

(4 pts) Calculate the size of the tag and the size of the cache index and total number of bits is cache given that:
Cache is direct mapped; Cache size = 8K; Block size = 4 bytes

Index size =

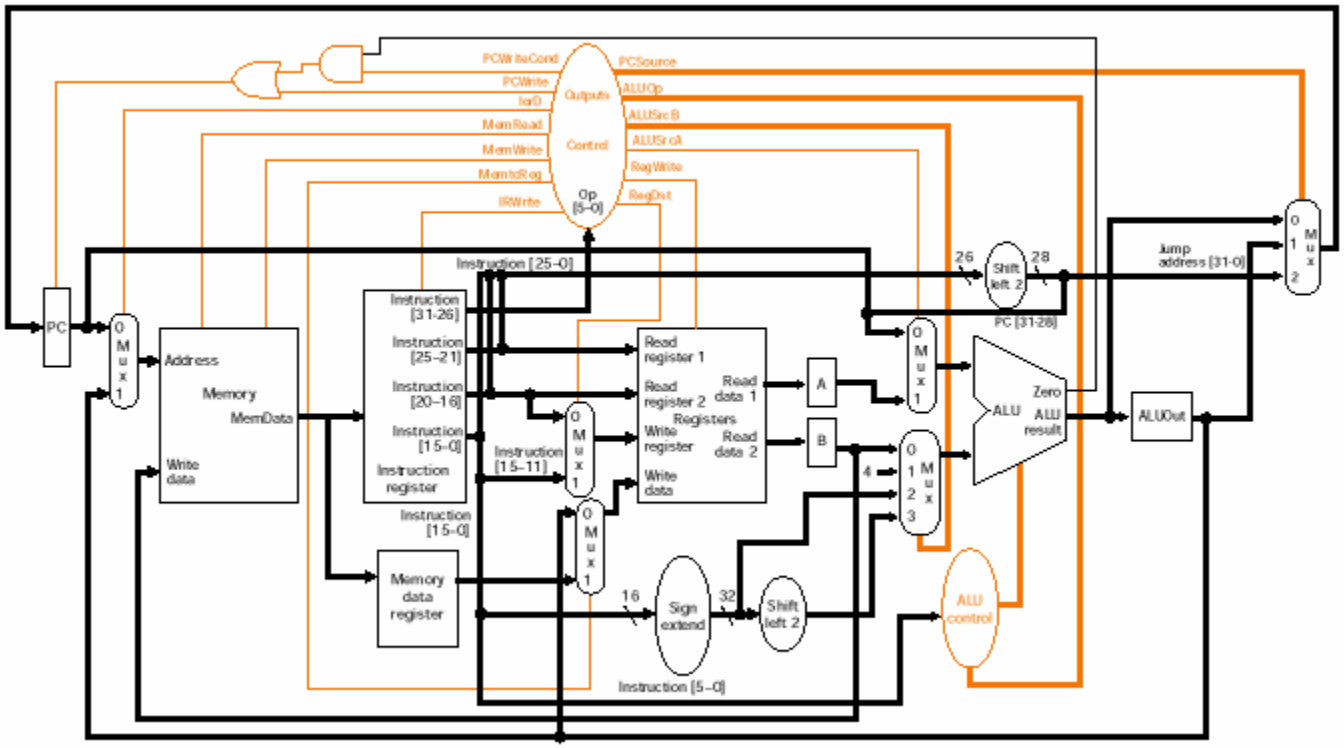
Tag size =

Total # of bits =

(1 pt) Explain why reduction / minimization is important:

(2 pts) How would decreasing the block size affect miss rate?

For these datapath and control questions use the multi-cycle datapath diagram provided below.



(4 pts) The RTL for Step 1, Instruction Fetch, is:

```
IR = Memory[PC];
PC = PC + 4;
```

Fill in the values that are required for the following control signals:

ALUSrcA =

ALUSrcB =

PCSource =

IorD =

(2 pts) The RTL for Step 2, Instruction Decode, is:

```
A = Reg[IR[25-21]]
B = Reg[IR[20-16]];
ALUOut = PC + (sign-extend(IR[15-0]) << 2);
```

Fill in the values that are required for the following control signals:

ALUSrcA =

ALUSrcB =

(1 pts) For an `lw` instruction, what is the value of RegDst?

RegDst =

Extra Problems for Practice – only covers since 12 week exam

Many of these are "why" questions – you should also look at the in-class Exercises for more practice problems.

1. **What is the difference between a conflict miss and a compulsory miss? How would you reduce each type?**

2. **What are two different strategies for dealing with cache writes? What is an advantage and disadvantage of each type?**

3. **Show the correct formula for calculating a cache index, given the following parameters:**
   a. **N = 16, Block size = 4, Associativity = 4**

   b. **N = 16, Block size = 8, direct-mapped**

4. **Suppose a direct-mapped cache has 64 blocks that are 8 bytes each.**
   Show how to break the following address into the tag, index, & byte offset.
   0000 1000 0101 1100 0001 0001 0111 1001

   How does this change if the cache is 4-way set associative?

5. **Why might we want more than one level of a cache?**

6. **Suppose we have a direct-mapped cache with 4 blocks of 2 bytes each. Label each of the following references as a hit or miss:**
   7 10 13 6 10 15 6 8

7. **Suppose a processor has a CPI of 3.0 given a perfect cache. If there are 1.4 memory accesses per instruction, a miss penalty of 20 cycles, and a miss rate of 5%, what is the effective CPI with the real cache?** ***Show the formula with values filled in, you don't have to actually complete the calculations.***

8. **What are two advantages of using virtual memory?**

9. **What is a TLB? Why do we need it?**

10. **What are two ways for the processor to send information to an I/O device? And 3 ways for an I/O device to send information to processor?**

11. **What is RAID? Why would you want to use it?**

12. **Which is usually faster – an asynchronous or a synchronous bus? Why would you ever use the slower type?**

13. **How does pipelining improve performance?**

14. Draw a pipeline diagram for this code, assuming the MIPS pipeline we used in class. Show stalls and/or forwarding where needed.

```
add $s1, $s3, $s4

lw  $v0, 0($s1)

sub $v0, $v0, $s1
```

15. If you had stalls in the above code, could you re-write it to avoid the stalls?

16. What is multiple issue? Is this the same as VLIW?

17. Why is branch prediction so important? Does multiple issue increase or decrease the need for such prediction?

18. Give one example of how a processor might use speculation to improve performance.

19. What is the difference between message passing machines and shared memory machines? Which one of these is commonly implemented with either centralized or distributed memory?

20. Explain the following: SIMD vs. MISD. Which of them is essentially never used?

21. If the cycle time and the maximum issue rate is the same, rank these three hardware architectures in terms of fastest to slowest:

a. **Fine-grain multithreading**
b. **Superscalar**
c. **Simultaneous multithreading**