

Table of Contents

Introduction

Hardware design

Domain-Specific Languages

Hardware EDSLs

Analyzed EDSLs

Choice criteria

Chosen EDSLs

Evaluation criteria

Modeled Circuits

Choice

ALU

Memory bank

CPU

Analysis of the EDSLs

Lava

ForSyDe

Coquet

Conclusions

Introduction

Hardware design

Domain-Specific
Languages

Hardware EDSLs

Analyzed EDSLs

Choice criteria

Chosen EDSLs

Evaluation criteria

Modeled Circuits

Choice

ALU

Memory bank

CPU

Analysis of the EDSLs

Lava

ForSyDe

Coquet

Conclusions



Section 1

Introduction

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Hardware design

Introduction

Hardware design

- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Example of an EDSL: Parsec

A simple parser for a "Game of Life"-like input format:

```
dead, alive :: Parser Bool
dead  = fmap (const False) (char '.')
alive = fmap (const True)  (char '*')

line :: Parser [Bool]
line  = many1 (dead <|> alive)

board :: Parser [[Bool]]
board = line 'endBy1' newline

parseBoardFromFile :: FilePath -> IO [[Bool]]
parseBoardFromFile filename = do
    result <- parseFromFile board filename
    return $ either (error . show) id result
```

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Universiteit Utrecht

Hardware EDSLs

An EDSL used for hardware design-related tasks. Can encompass:

- ▶ Modelling / description
- ▶ Simulation (validation)
- ▶ Formal verification
- ▶ Synthesis to other (lower-level) languages

Introduction

Hardware design
Domain-Specific
Languages
Hardware EDSLs

Analyzed EDSLs

Choice criteria
Chosen EDSLs
Evaluation criteria

Modeled Circuits

Choice
ALU
Memory bank
CPU

Analysis of the EDSLs

Lava
ForSyDe
Coquet

Conclusions



Example of a hardware EDSL

Some Lava code. . .

Introduction

- Hardware design
- Domain-Specific Languages

Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Section 2

Analyzed EDSLs

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Choice criteria

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

Choice criteria

- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Chosen EDSLs

The language we chose to evaluate, with the respective host language, were:

- ▶ Lava (Haskell - *chalmers-lava dialect*)
- ▶ ForSyDe (Haskell)
- ▶ Coquet (Coq)

Introduction

Hardware design
Domain-Specific
Languages
Hardware EDSLs

Analyzed EDSLs

Choice criteria
Chosen EDSLs
Evaluation criteria

Modeled Circuits

Choice
ALU
Memory bank
CPU

Analysis of the EDSLs

Lava
ForSyDe
Coquet

Conclusions



Evaluation criteria

- ▶ Simulation
- ▶ Verification
- ▶ Genericity
- ▶ Depth of embedding
- ▶ Tool integration
- ▶ Extensibility

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

Choice criteria
Chosen EDSLs

Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

Lava
ForSyDe
Coquet

Conclusions



Universiteit Utrecht

Section 3

Modeled Circuits

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Choice criteria

- ▶ Not too simple, not too complex
- ▶ Familiar to any hardware designer
- ▶ Well-defined, available specification

Introduction

Hardware design
Domain-Specific
Languages
Hardware EDSLs

Analyzed EDSLs

Choice criteria
Chosen EDSLs
Evaluation criteria

Modeled Circuits

Choice
ALU
Memory bank
CPU

Analysis of the EDSLs

Lava
ForSyDe
Coquet

Conclusions



Chosen circuits

We cherry-picked circuits from the book “Elements of Computing Systems”, as they satisfied all of our demands.

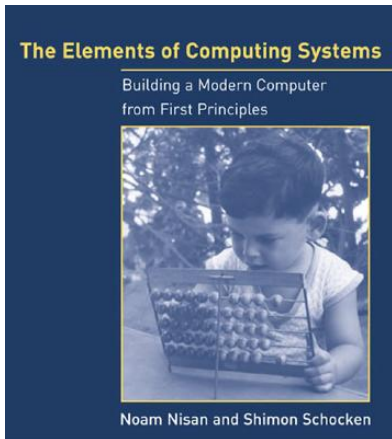


Figure: “Elements of Computing Systems” - Noam Nisan, Shimon Schocken, available at <http://www.nand2tetris.org>.

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

Choice

- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Universiteit Utrecht

ALU block diagram

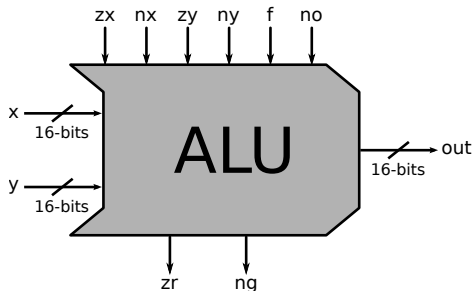


Figure: Input/Output ports of *circuit 1*, the ALU.

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Universiteit Utrecht

Memory bank block diagram

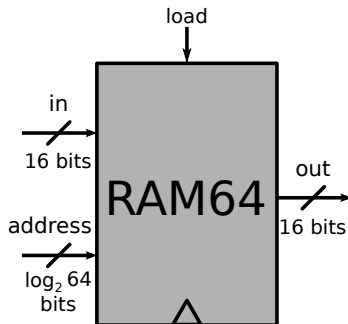


Figure: Input/Output ports of *circuit 2*, the RAM64 block.

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



CPU block diagram

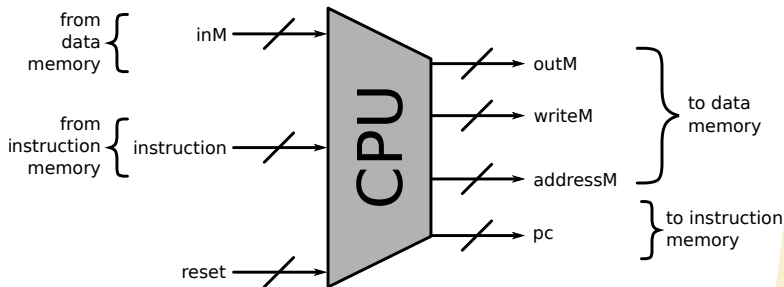


Figure: Input/Output ports of *circuit 3*, the *Hack CPU*.

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Section 4

Analysis of the EDSLs

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Lava

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

Lava

- ForSyDe
- Coquet

Conclusions



Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe**
- Coquet

Conclusions



Coquet

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet**

Conclusions



Section 5

Conclusions

Introduction

- Hardware design
- Domain-Specific Languages
- Hardware EDSLs

Analyzed EDSLs

- Choice criteria
- Chosen EDSLs
- Evaluation criteria

Modeled Circuits

- Choice
- ALU
- Memory bank
- CPU

Analysis of the EDSLs

- Lava
- ForSyDe
- Coquet

Conclusions



Thank you!

Questions?

