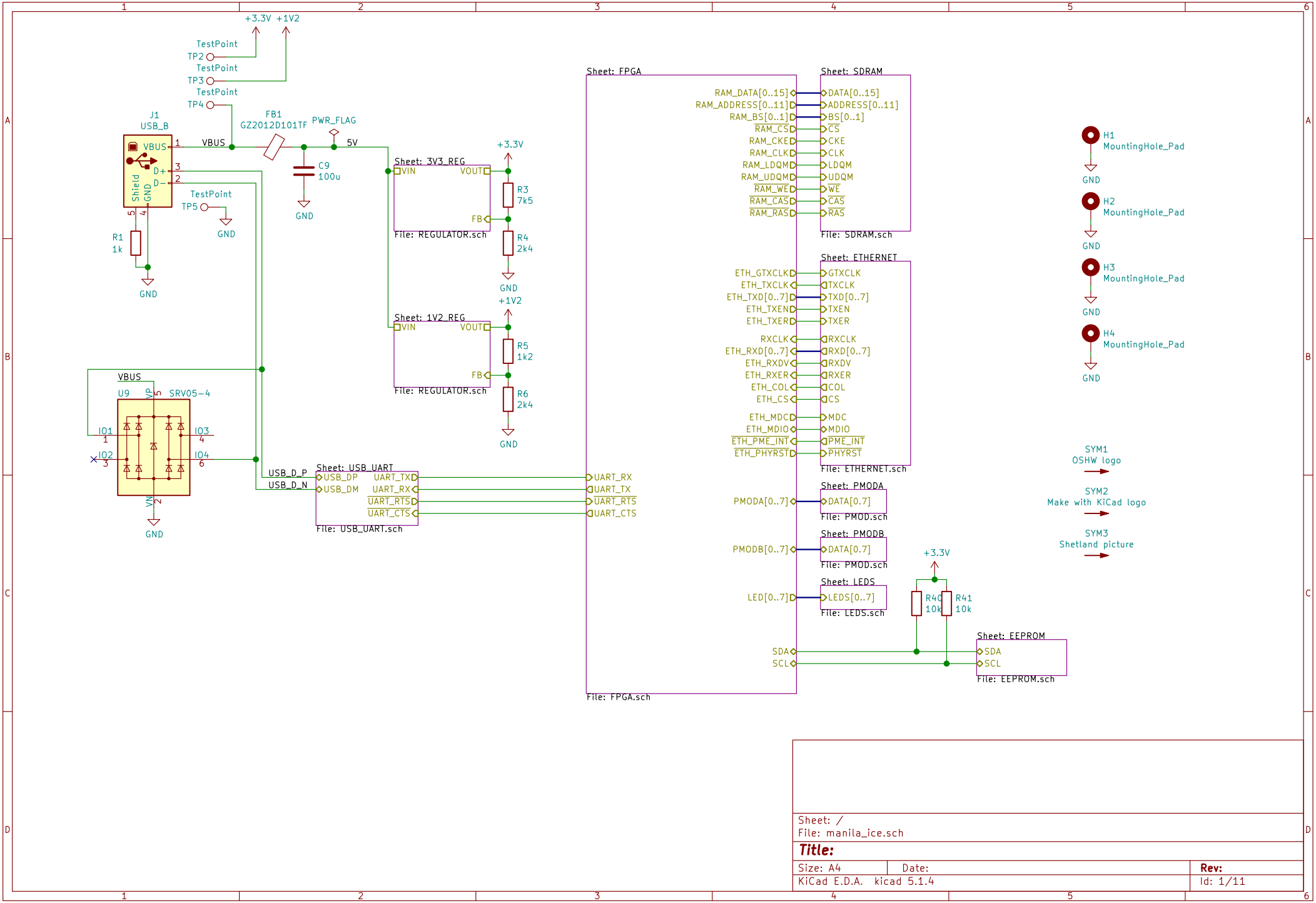
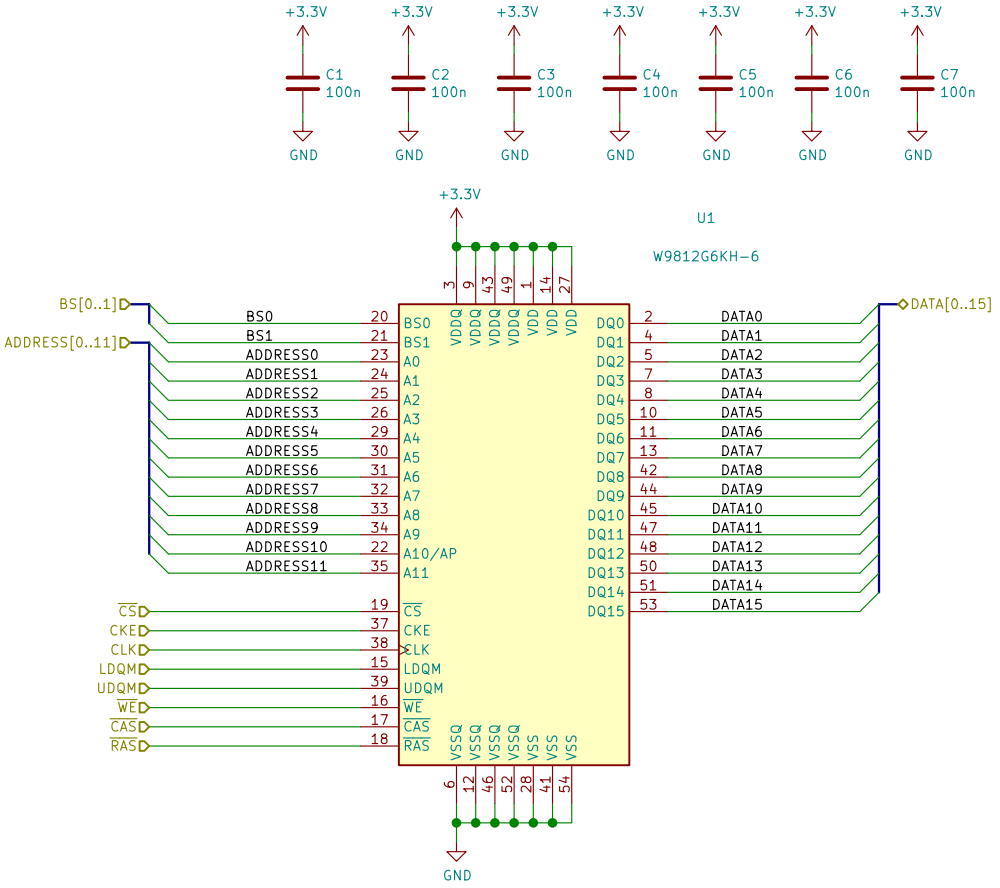
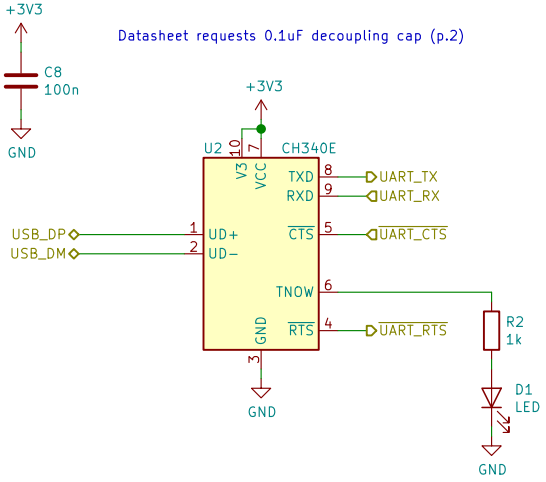

+3.3V
+1V2
TestPoint
TP2
TP3
TP4
TP5
J1
USB_B
VBUS
D+
D-
Shield
GND
FB1
GZ2012D101TF
PWR_FLAG
5V
C9
100u
R1
1k
Sheet: 3V3_REG
VIN
VOUT
FB
File: REGULATOR.sch
R3
7k5
R4
2k4
Sheet: 1V2_REG
R5
1k2
R6
2k4
U9
SRV05-4
IO1
IO2
IO3
IO4
USB_D_P
USB_D_N
Sheet: USB_UART
USB_DP
USB_DM
UART_TX
UART_RX
UART_RTS
UART_CTS
File: USB_UART.sch
Sheet: FPGA
File: FPGA.sch
Sheet: SDRAM
RAM_DATA[0..15]
RAM_ADDRESS[0..11]
RAM_BS[0..1]
RAM_CS
RAM_CKE
RAM_CLK
RAM_LDQM
RAM_UDQM
RAM_WE
RAM_CAS
RAM_RAS
DATA[0..15]
ADDRESS[0..11]
BS[0..1]
CS
CKE
CLK
LDQM
UDQM
WE
CAS
RAS
File: SDRAM.sch
Sheet: ETHERNET
ETH_GTXCLK
ETH_TXCLK
ETH_TXD[0..7]
ETH_TXEN
ETH_TXER
RXCLK
ETH_RXD[0..7]
ETH_RXDV
ETH_RXER
ETH_COL
ETH_CS
ETH_MDC
ETH_MDIO
ETH_PME_INT
ETH_PHYRST
GTXCLK
TXCLK
TXD[0..7]
TXEN
TXER
RXCLK
RXD[0..7]
RXDV
RXER
COL
CS
MDC
MDIO
PME_INT
PHYRST
File: ETHERNET.sch
Sheet: PMODA
PMODA[0..7]
DATA[0.7]
File: PMOD.sch
Sheet: PMODB
PMODB[0..7]
DATA[0.7]
File: PMOD.sch
Sheet: LEDS
LED[0..7]
LEDS[0..7]
File: LEDS.sch
R40
10k
R41
10k
Sheet: EEPROM
SDA
SCL
File: EEPROM.sch
H1
MountingHole_Pad
H2
MountingHole_Pad
H3
MountingHole_Pad
H4
MountingHole_Pad
SYM1
OSHW logo
SYM2
Make with KiCad logo
SYM3
Shetland picture
Sheet: /
File: manila_ice.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.4
Id: 1/11



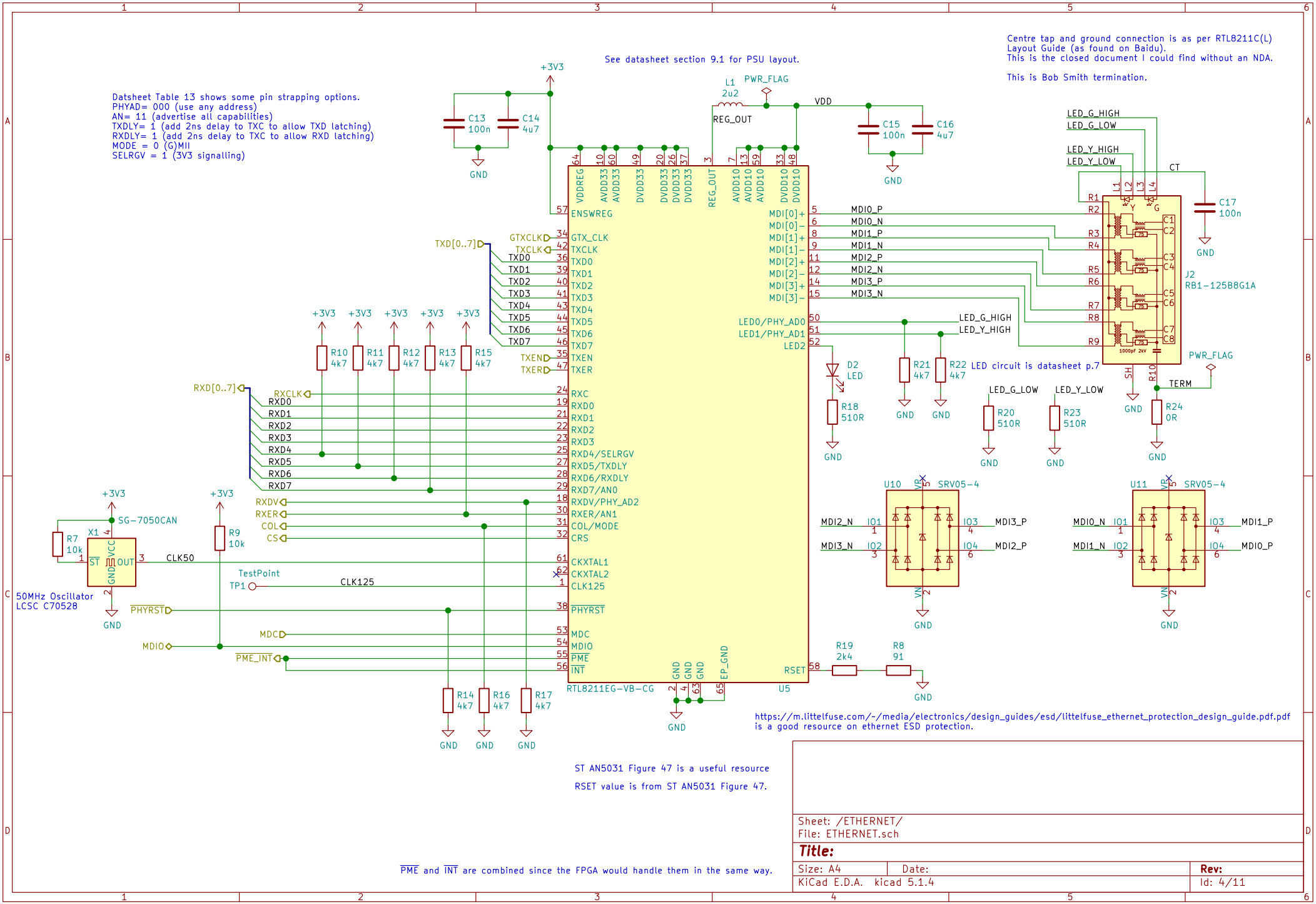
Sheet: /SDRAM/		
File: SDRAM.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4		Id: 2/11

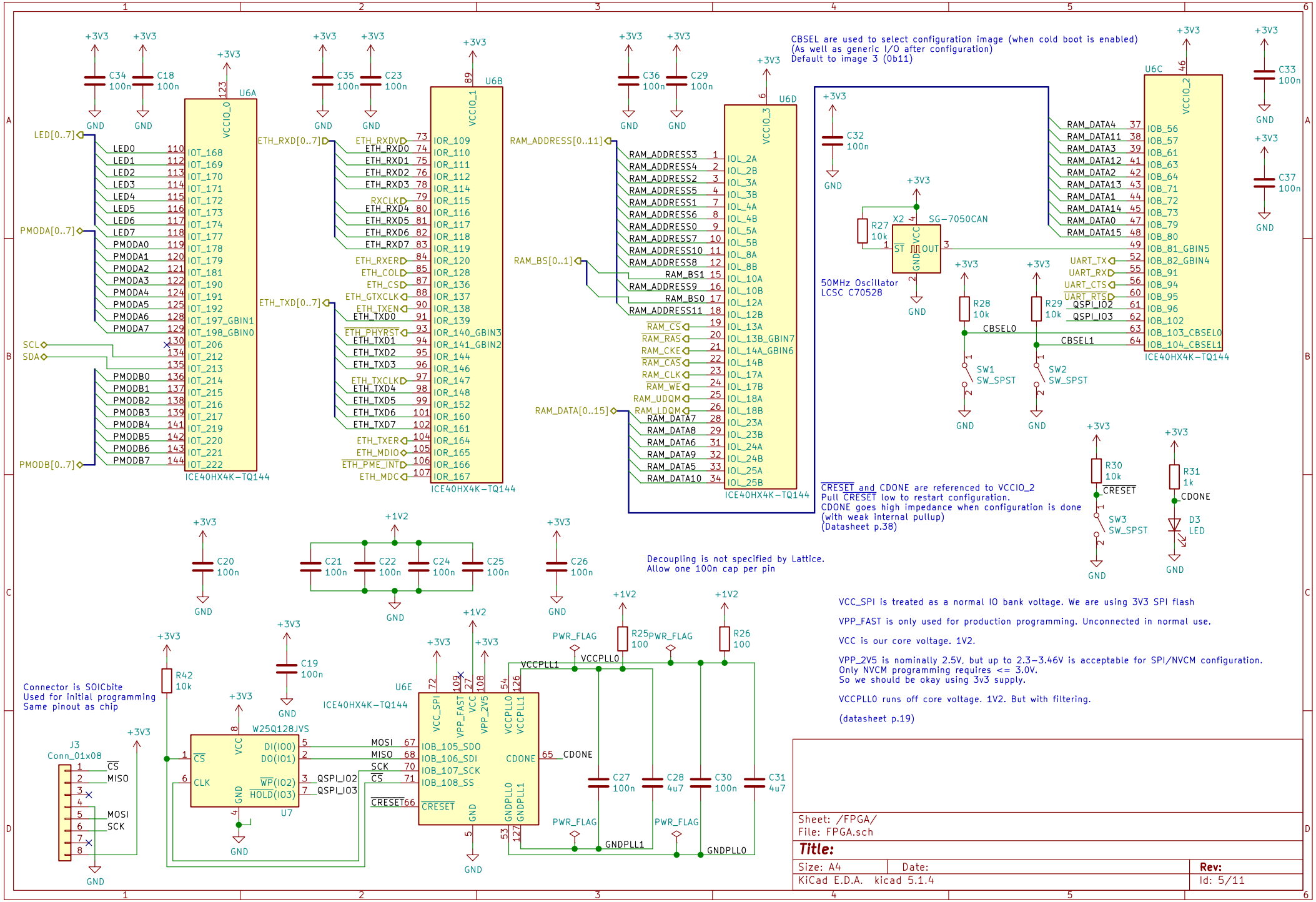
The chip supports both 5V and 3V3 operation.
For 3V3 operation. VCC connects to V3. (Datasheet p.4)



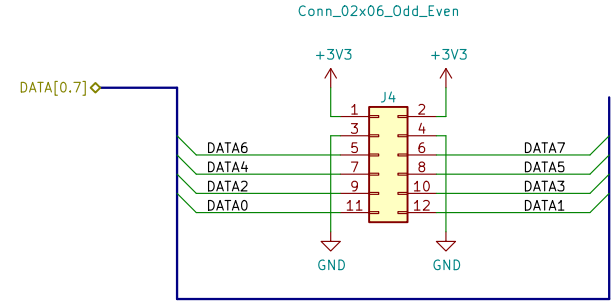
TNOW is an active high status output to show that transmission is in progress. (Datasheet p.3)
It is not clear how much current it can provide, but should be okay with 1.5mA for an LED.

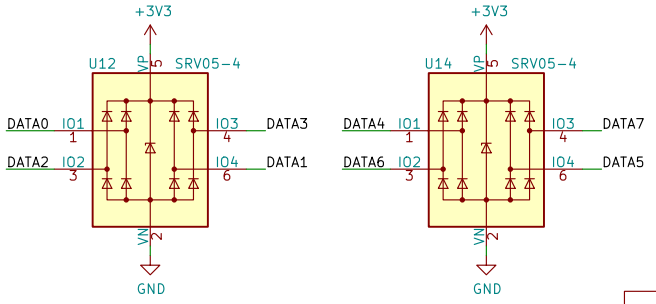
Sheet: /USB_UART/ File: USB_UART.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4		Id: 3/11


Datsheet Table 13 shows some pin strapping options.
PHYAD= 000 (use any address)
AN= 11 (advertise all capabilities)
TXDLY= 1 (add 2ns delay to TXC to allow TXD latching)
RXDLY= 1 (add 2ns delay to TXC to allow RXD latching)
MODE = 0 (G)MII
SELRGV = 1 (3V3 signalling)
See datasheet section 9.1 for PSU layout.
Centre tap and ground connection is as per RTL8211C(L) Layout Guide (as found on Baidu).
This is the closed document I could find without an NDA.
This is Bob Smith termination.
RTL8211EG-VB-CG
U5
J2
RB1-125B8G1A
SG-7050CAN
50MHz Oscillator
LCSC C70528
SRV05-4
U10
U11
LED circuit is datasheet p.7
https://m.littelfuse.com/~/media/electronics/design_guides/esd/littelfuse_ethernet_protection_design_guide.pdf.pdf
is a good resource on ethernet ESD protection.
ST AN5031 Figure 47 is a useful resource
RSET value is from ST AN5031 Figure 47.
PME and INT are combined since the FPGA would handle them in the same way.
Sheet: /ETHERNET/
File: ETHERNET.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.4
Id: 4/11


U6A
ICE40HX4K-TQ144
U6B
ICE40HX4K-TQ144
U6D
ICE40HX4K-TQ144
U6C
ICE40HX4K-TQ144
U6E
ICE40HX4K-TQ144
U7
W25Q128JVS
J3
Conn_01x08
CBSEL are used to select configuration image (when cold boot is enabled)
(As well as generic I/O after configuration)
Default to image 3 (0b11)
50MHz Oscillator
LCSC C70528
SG-7050CAN
CRESET and CDONE are referenced to VCCIO_2
Pull CRESET low to restart configuration.
CDONE goes high impedance when configuration is done
(with weak internal pullup)
(Datasheet p.38)
Decoupling is not specified by Lattice.
Allow one 100n cap per pin
Connector is SOICbite
Used for initial programming
Same pinout as chip
VCC_SPI is treated as a normal IO bank voltage. We are using 3V3 SPI flash
VPP_FAST is only used for production programming. Unconnected in normal use.
VCC is our core voltage. 1V2.
VPP_2V5 is nominally 2.5V, but up to 2.3–3.46V is acceptable for SPI/NVCM configuration.
Only NVCM programming requires <= 3.0V.
So we should be okay using 3v3 supply.
VCCPLL0 runs off core voltage. 1V2. But with filtering.
(datasheet p.19)
Sheet: /FPGA/
File: FPGA.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.4
Id: 5/11

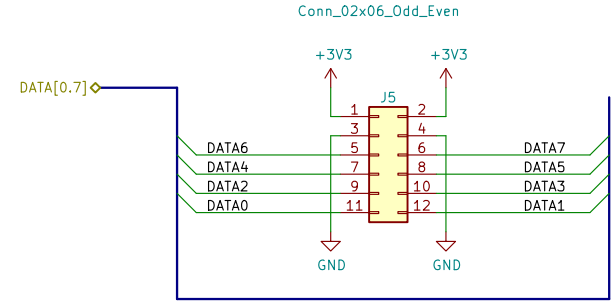
N.B Pinout does not match PMOD spec to fit in with KiCAD numbering

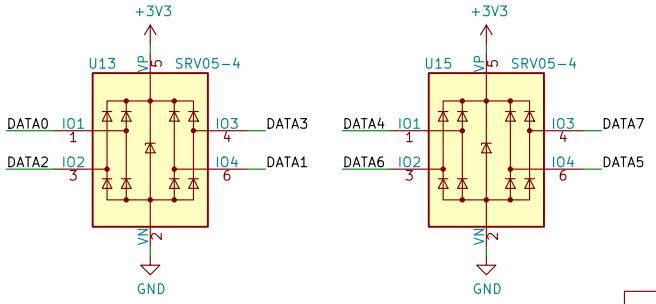




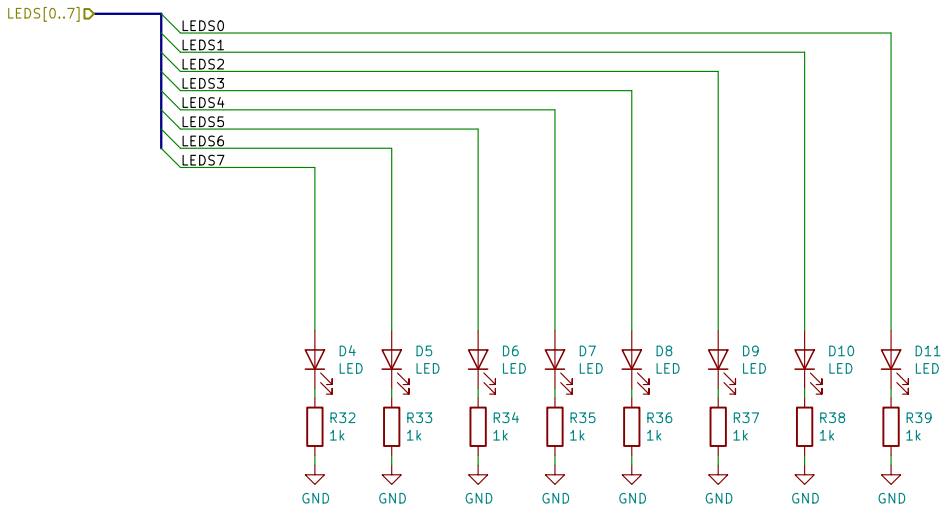
Sheet: /PMODA/		
File: PMOD.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4		Id: 6/11

N.B Pinout does not match PMOD spec to fit in with KiCAD numbering



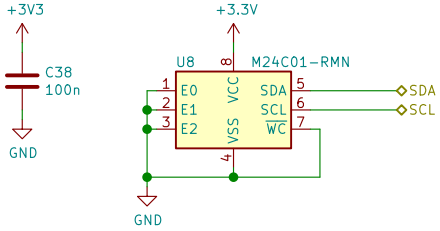


Sheet: /PMODB/ File: PMOD.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4		Id: 7/11



Sheet: /LEDS/		
File: LEDS.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4		Id: 8/11

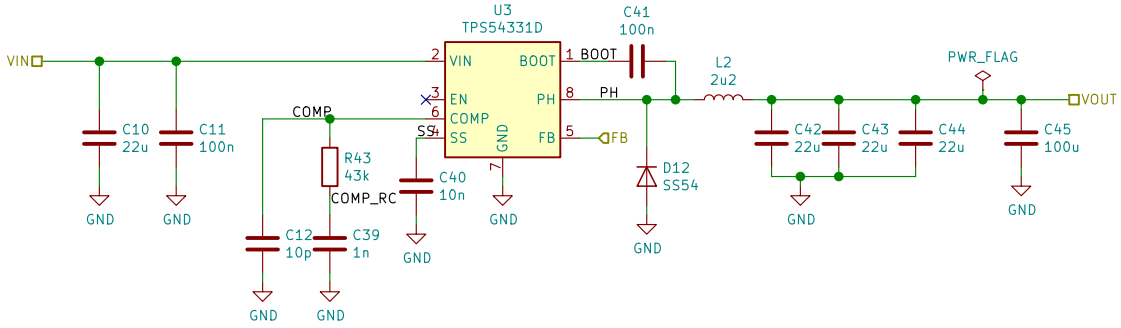
TODO: Change for real part: M24C64-RMN6TP
JLC C79988



Sheet: /EEPROM/		
File: EEPROM.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4		Id: 9/11

3A max output.
Designed using TI webench (tweaked from default values)
Inductor value is a little low, but allows part reuse

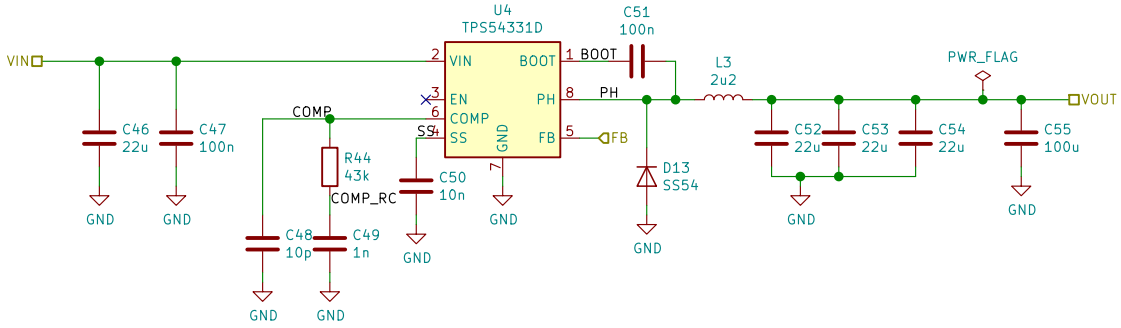
Vref = 0.8V



Sheet: /1V2_REG/		
File: REGULATOR.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4		Id: 10/11

3A max output.
Designed using TI webench (tweaked from default values)
Inductor value is a little low, but allows part reuse

Vref = 0.8V



Sheet: /3V3_REG/		
File: REGULATOR.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.4		Id: 11/11