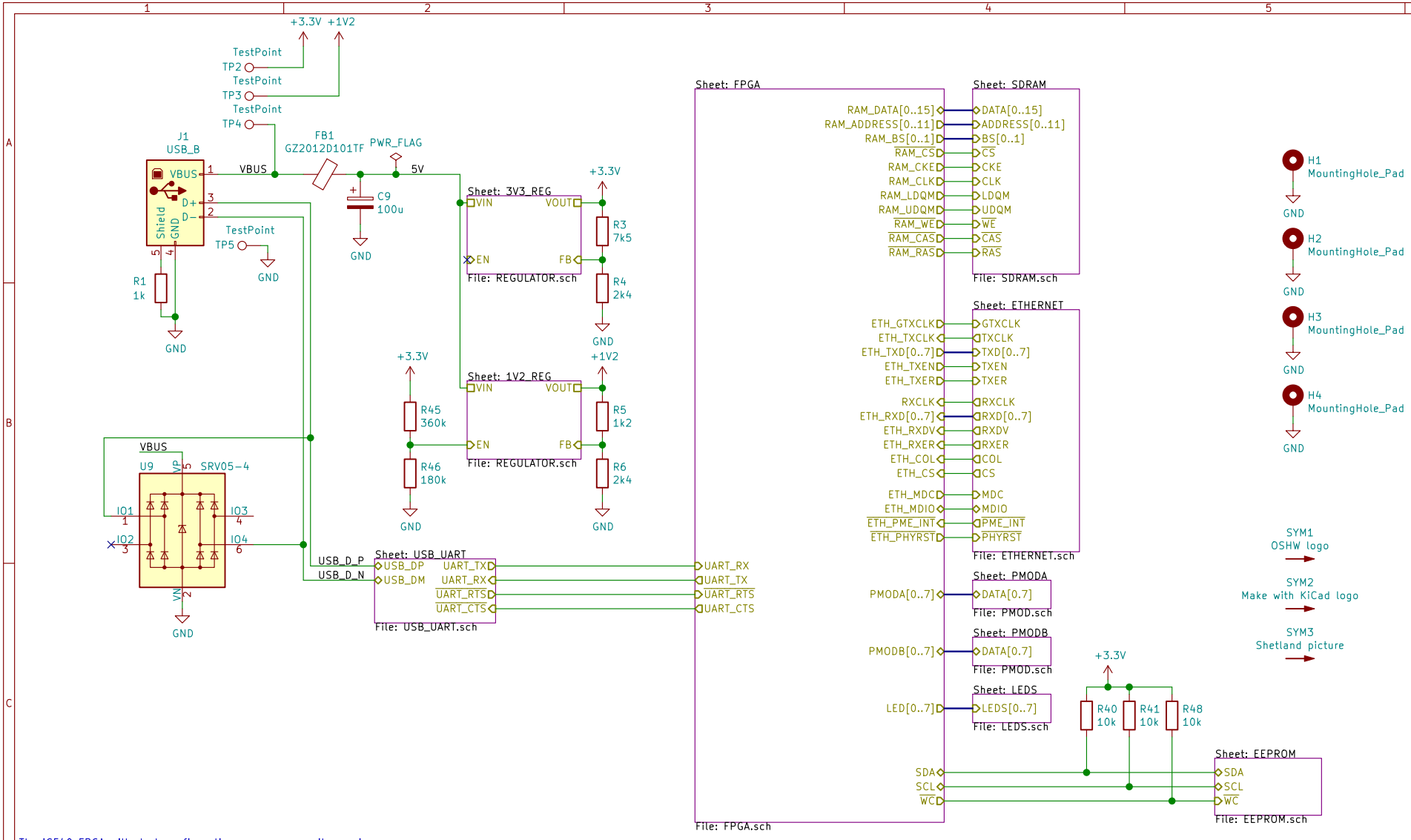


The iCE40 FPGA will start configuration once power rails are in range.
It considers the SPI voltage to be in range once it reaches 1V8, but our flash chip will not work until the 3V3 rail reaches 2V7.

We get around this by sequencing the 1V2 rail to only come up after the 3V3 is good. This avoids extra circuitry to hold $\overline{\text{CRESET}}$ low until the rails are stable.

This is acceptable becuase the iCE40 doesn't require a particular power sequencing order.

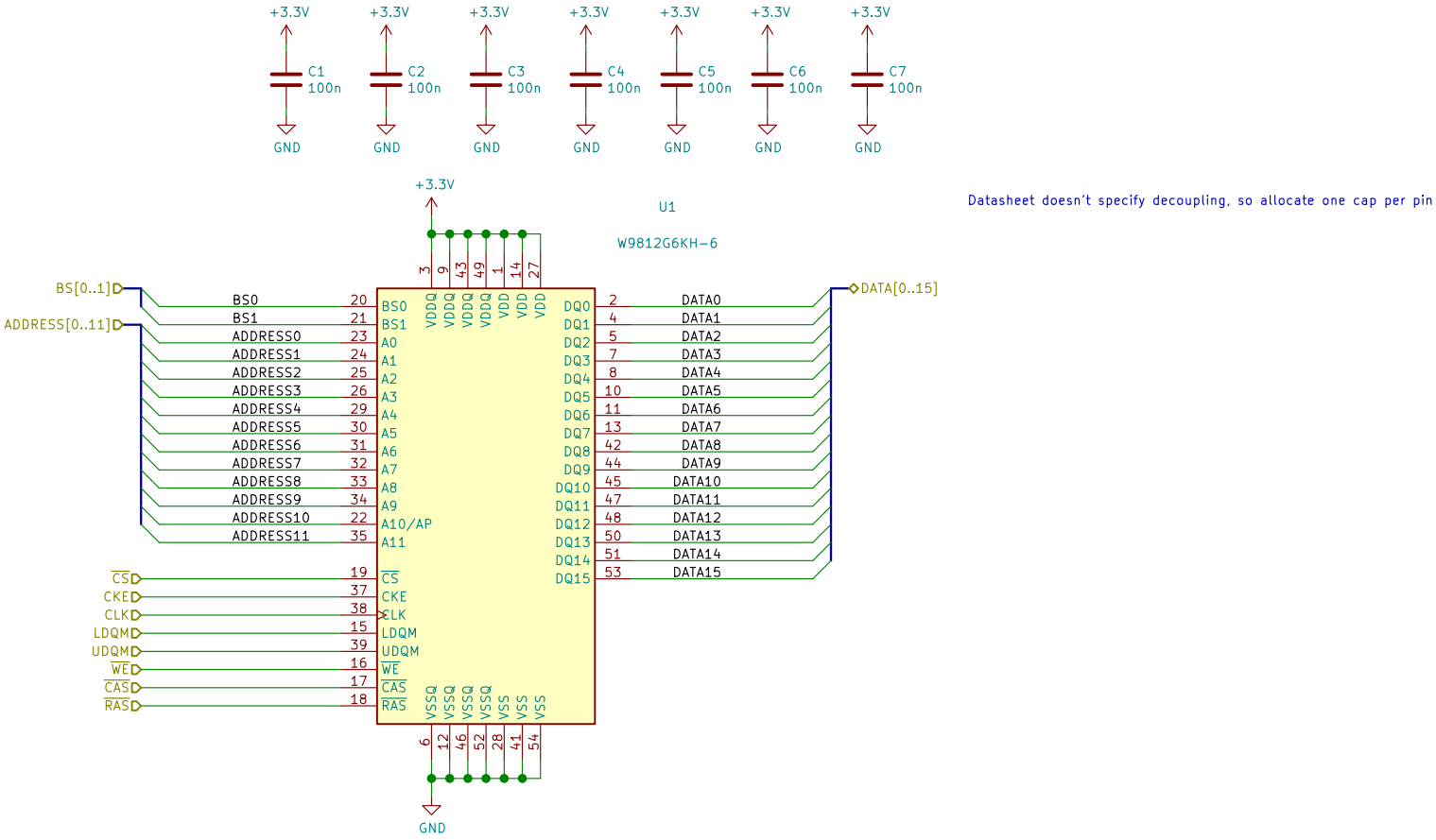
This works by (ab)using the EN pin of the power supply. It has hyseresis built in designed to only enable the supply when the input is in the correct voltage range.
The chosen resistor values turn the 1.2V supply on once the 3V3 supply is greater than 3.2V, but only turn it off again once the 3.3V supply has fallen below 2.13V.

We could probably get away without this, because the iCE40 automatically retries six times to get around power sequencing issues.
(TN1248 p.17
It is best to design robustly however, and only requires two extra resistors.

Sheet: /
File: manila_ice.sch

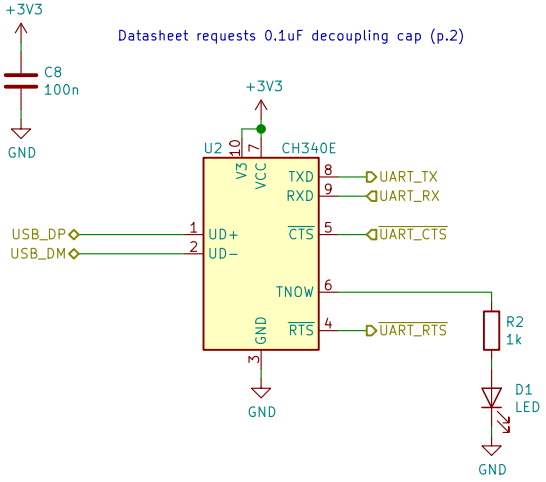
Title: manila iCE

Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 1/11



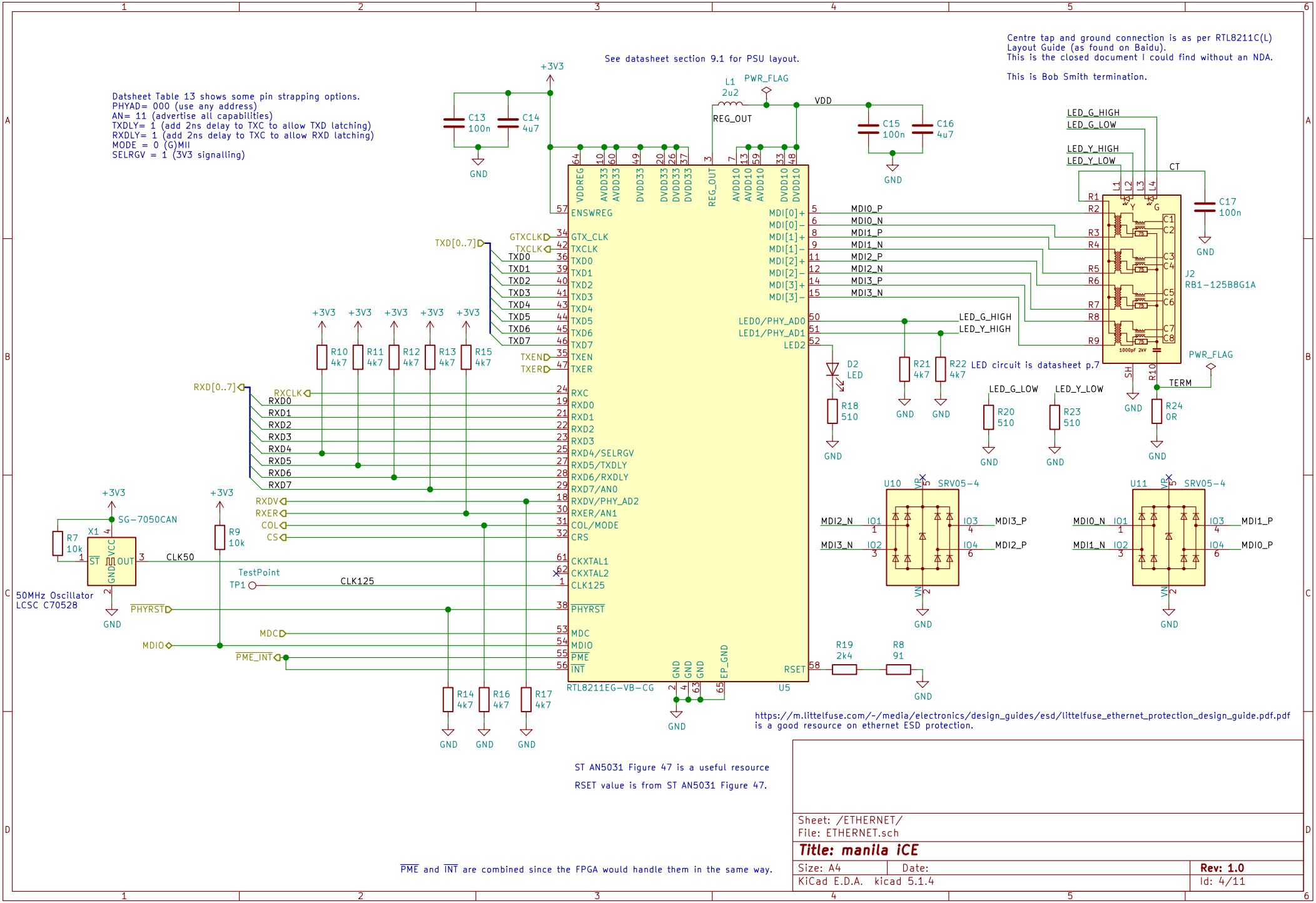
Sheet: /SDRAM/		
File: SDRAM.sch		
Title: manila iCE		
Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 2/11

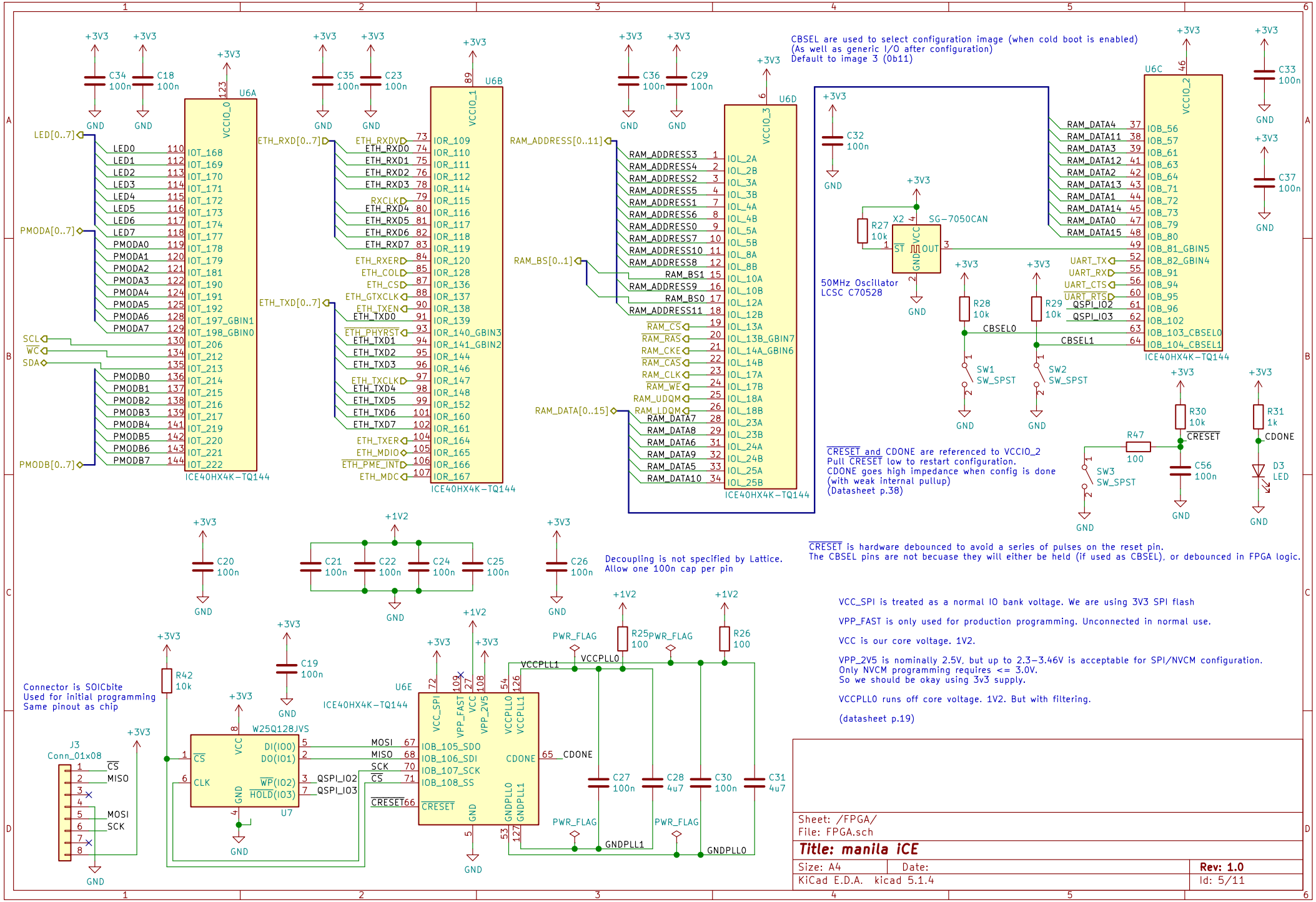
The chip supports both 5V and 3V3 operation.
For 3V3 operation. VCC connects to V3. (Datasheet p.4)



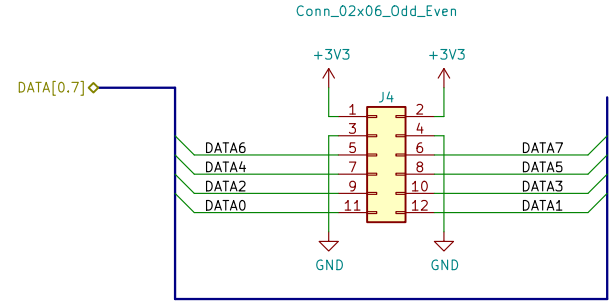
TNOW is an active high status output to show that transmission is in progress. (Datasheet p.3)
It is not clear how much current it can provide, but should be okay with 1.5mA for an LED.

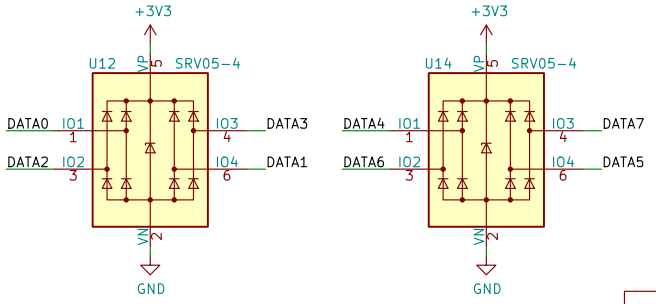
Sheet: /USB_UART/		
File: USB_UART.sch		
Title: manila iCE		
Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 3/11


Datsheet Table 13 shows some pin strapping options.
PHYAD= 000 (use any address)
AN= 11 (advertise all capabilities)
TXDLY= 1 (add 2ns delay to TXC to allow TXD latching)
RXDLY= 1 (add 2ns delay to TXC to allow RXD latching)
MODE = 0 (G)MII
SELRGV = 1 (3V3 signalling)
See datasheet section 9.1 for PSU layout.
Centre tap and ground connection is as per RTL8211C(L) Layout Guide (as found on Baidu).
This is the closed document I could find without an NDA.
This is Bob Smith termination.
RTL8211EG-VB-CG
U5
SG-7050CAN
50MHz Oscillator
LCSC C70528
SRV05-4
U10
U11
J2
RB1-125B8G1A
LED circuit is datasheet p.7
https://m.littelfuse.com/~/media/electronics/design_guides/esd/littelfuse_ethernet_protection_design_guide.pdf.pdf
is a good resource on ethernet ESD protection.
ST AN5031 Figure 47 is a useful resource
RSET value is from ST AN5031 Figure 47.
PME and INT are combined since the FPGA would handle them in the same way.
Sheet: /ETHERNET/
File: ETHERNET.sch
Title: manila iCE
Size: A4
Date:
Rev: 1.0
KiCad E.D.A. kicad 5.1.4
Id: 4/11


CBSEL are used to select configuration image (when cold boot is enabled)
(As well as generic I/O after configuration)
Default to image 3 (0b11)
50MHz Oscillator
LCSC C70528
CRESET and CDONE are referenced to VCCIO_2
Pull CRESET low to restart configuration.
CDONE goes high impedance when config is done
(with weak internal pullup)
(Datasheet p.38)
CRESET is hardware debounced to avoid a series of pulses on the reset pin.
The CBSEL pins are not becuase they will either be held (if used as CBSEL), or debounced in FPGA logic.
Decoupling is not specified by Lattice.
Allow one 100n cap per pin
Connector is SOICbite
Used for initial programming
Same pinout as chip
VCC_SPI is treated as a normal IO bank voltage. We are using 3V3 SPI flash
VPP_FAST is only used for production programming. Unconnected in normal use.
VCC is our core voltage. 1V2.
VPP_2V5 is nominally 2.5V, but up to 2.3–3.46V is acceptable for SPI/NVCM configuration.
Only NVCM programming requires <= 3.0V.
So we should be okay using 3v3 supply.
VCCPLL0 runs off core voltage. 1V2. But with filtering.
(datasheet p.19)
Sheet: /FPGA/
File: FPGA.sch
Title: manila iCE
Size: A4
Date:
Rev: 1.0
KiCad E.D.A. kicad 5.1.4
Id: 5/11

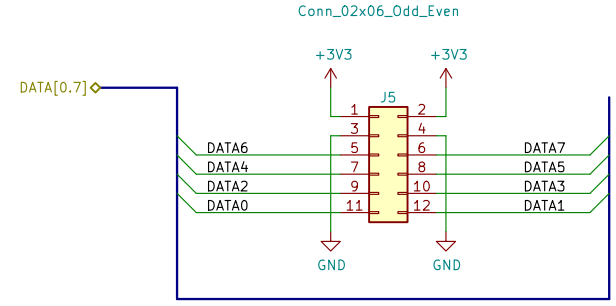
N.B KiCAD pin numbering is different to PMOD spec pin numbering.

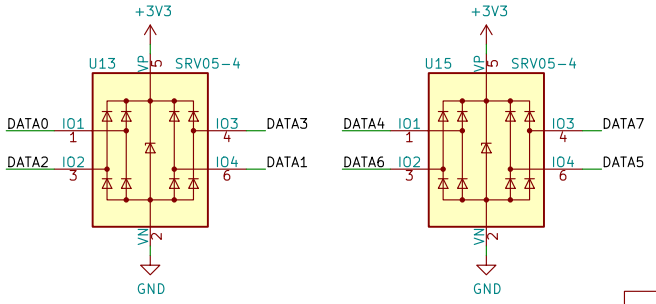




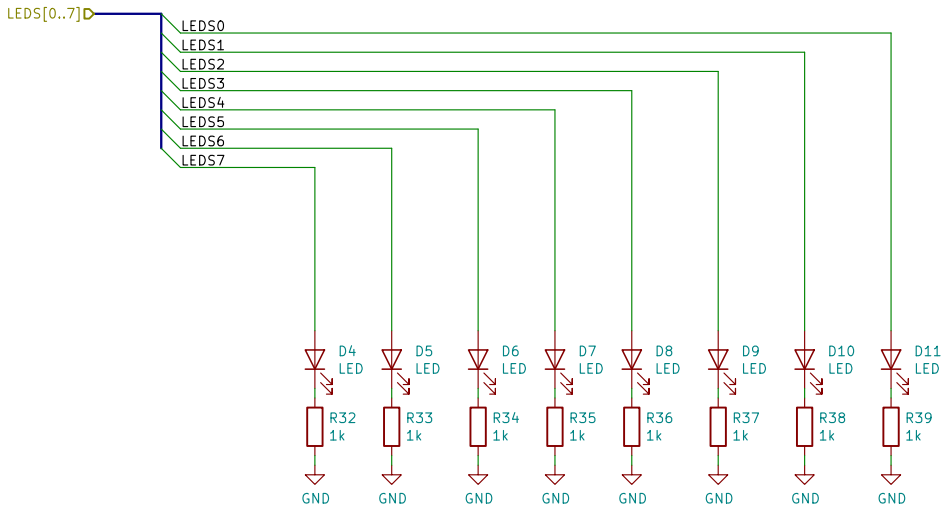
Sheet: /PMODA/		
File: PMOD.sch		
Title: manila iCE		
Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 6/11

N.B KiCAD pin numbering is different to PMOD spec pin numbering.



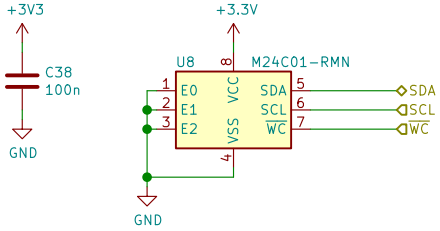


Sheet: /PMODB/		
File: PMOD.sch		
Title: manila iCE		
Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 7/11



Sheet: /LEDS/		
File: LEDS.sch		
Title: manila iCE		
Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 8/11

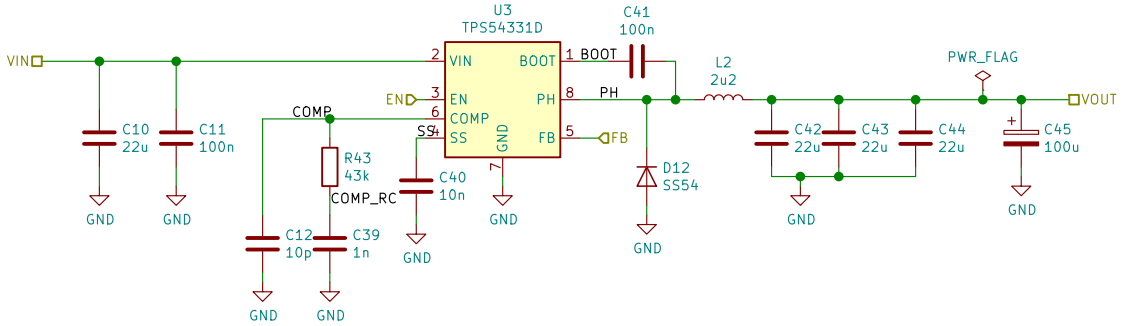
TODO: Change for real part: M24C64-RMN6TP
JLC C79988



Sheet: /EEPROM/		
File: EEPROM.sch		
Title: manila iCE		
Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 9/11

3A max output.
Designed using TI webench (tweaked from default values)
Inductor value is a little low, but allows part reuse

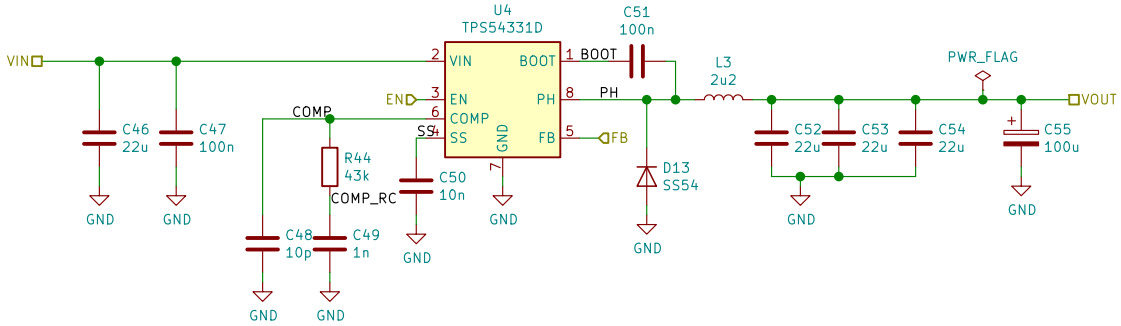
Vref = 0.8V



Sheet: /1V2_REG/		
File: REGULATOR.sch		
Title: manila iCE		
Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 10/11

3A max output.
Designed using TI webench (tweaked from default values)
Inductor value is a little low, but allows part reuse

Vref = 0.8V



Sheet: /3V3_REG/		
File: REGULATOR.sch		
Title: manila iCE		
Size: A4	Date:	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.4		Id: 11/11