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Jameco Part Number 42198

## 5101 FAMILY 256 x 4 BIT STATIC CMOS RAM

P/N	Typ. Current @ 2V ( $\mu$ A)	Typ. Current @ 5V ( $\mu$ A)	Max Access (ns)
5101L	0.14	0.2	650
5101L-1	0.14	0.2	450
5101L-3	0.70	1.0	650

- Single +5V Power Supply
- Ideal for Battery Operation (5101L)
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Output

The Intel® 5101 is an ultra-low power 1024-bit (256 words X 4 bits) static RAM fabricated with an advanced ion-implanted silicon gate CMOS technology. The device has two chip enable inputs. Minimum standby current is drawn by this device when CE2 is at a low level. When deselected the 5101 draws from the single 5-volt supply only 10 microamps. This device is ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

The 5101 uses fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 has separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

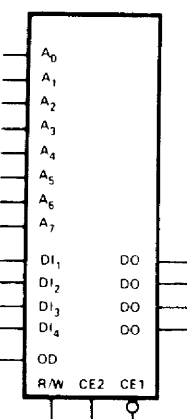
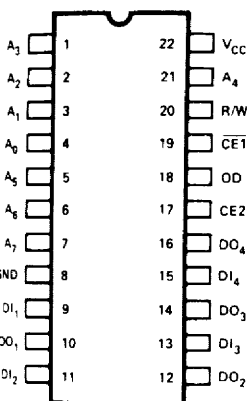
*The 5101L has the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.*

A pin compatible N-channel static RAM, the Intel® 2101A, is also available for low cost applications where a 256 X 4 organization is needed.

The Intel ion-implanted, silicon gate, Complementary MOS (CMOS) process allows the design and production of ultra-low power, high performance memories.

### PIN CONFIGURATION

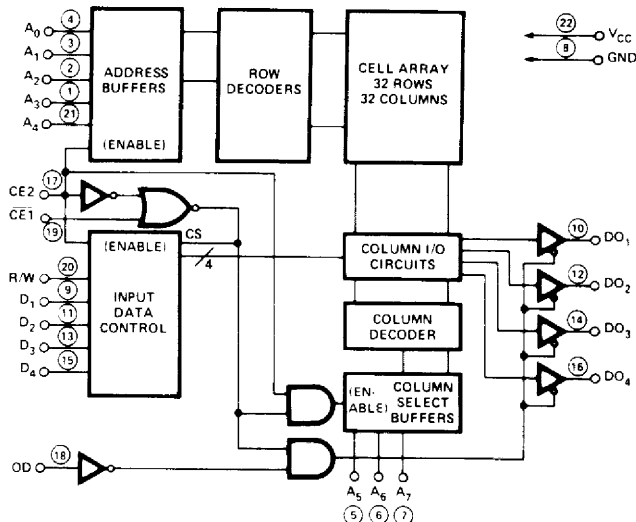
### LOGIC SYMBOL



### TRUTH TABLE

CE <sub>1</sub>	CE <sub>2</sub>	OD	R/W	D <sub>IN</sub>	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D <sub>IN</sub>	Write
L	H	L	H	X	D <sub>OUT</sub>	Read

### BLOCK DIAGRAM



## 5101 FAMILY

### Absolute Maximum Ratings \*

Ambient Temperature Under Bias . . . . . -10°C to 80°C  
 Storage Temperature . . . . . -65°C to +150°C  
 Voltage On Any Pin  
     With Respect to Ground . . . . . -0.3V to  $V_{CC} + 0.3V$   
 Maximum Power Supply Voltage . . . . . +7.0V  
 Power Dissipation . . . . . 1 Watt

### \*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### D. C. and Operating Characteristics

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$  unless otherwise specified.

Symbol	Parameter	5101L and 5101L-1 Limits			5101L-3 Limits			Units	Test Conditions
		Min.	Typ. <sup>[1]</sup>	Max.	Min.	Typ. <sup>[1]</sup>	Max.		
$I_{L2}^{[2]}$	Input Current		5			5		nA	
$I_{LO}^{[2]}$	Output Leakage Current			1			1	$\mu\text{A}$	$\overline{CE1} = 2.2V$ , $V_{OUT} = 0$ to $V_{CC}$
$I_{CC1}$	Operating Current		9	22		9	22	mA	$V_{IN} = V_{CC}$ , Except $\overline{CE1} \leq 0.65V$ , Outputs Open
$I_{CC2}$	Operating Current		13	27		13	27	mA	$V_{IN} = 2.2V$ , Except $\overline{CE1} \leq 0.65V$ , Outputs Open
$I_{CCL}^{[2]}$	Standby Current			10			200	$\mu\text{A}$	$\overline{CE2} \leq 0.2V$ , $T_A = 70^\circ\text{C}$
$V_{IL}$	Input Low Voltage	-0.3		0.65	-0.3		0.65	V	
$V_{IH}$	Input High Voltage	2.2		$V_{CC}$	2.2		$V_{CC}$	V	
$V_{OL}$	Output Low Voltage			0.4			0.4	V	$I_{OL} = 2.0\text{ mA}$
$V_{OH}$	Output High Voltage	2.4			2.4			V	$I_{OH} = -1.0\text{ mA}$

### Low $V_{CC}$ Data Retention Characteristics (For 5101L, 5101L-1 and 5101L-3) $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

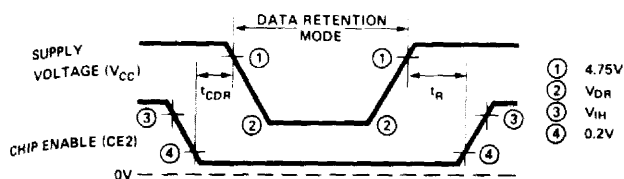
Symbol	Parameter	Min.	Typ. <sup>[1]</sup>	Max.	Units	Test Conditions	
$V_{DR}$	$V_{CC}$ for Data Retention	2.0			V	$\overline{CE2} \leq 0.2V$	
$I_{CCDR1}$	5101L or 5101L-1 Data Retention Current		0.14	10	$\mu\text{A}$		$V_{DR} = 2.0V$ , $T_A = 70^\circ\text{C}$
$I_{CCDR2}$	5101L-3 Data Retention Current		0.70	200	$\mu\text{A}$		$V_{DR} = 2.0V$ , $T_A = 70^\circ\text{C}$
$t_{CDR}$	Chip Deselect to Data Retention Time	0			ns		
$t_R$	Operation Recovery Time	$t_{RC}^{[3]}$			ns		

### NOTES:

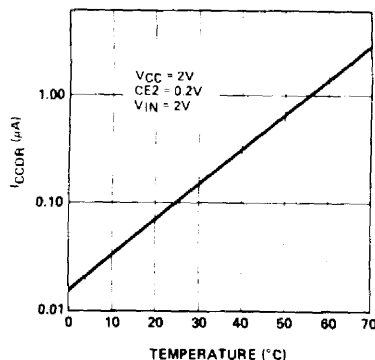
1. Typical values are  $T_A = 25^\circ\text{C}$  and nominal supply voltage.
2. Current through all inputs and outputs included in  $I_{CCL}$  measurement.
3.  $t_{RC}$  = Read Cycle Time.

# 5101 FAMILY

## Low $V_{CC}$ Data Retention Waveform



## Typical $I_{CCDR}$ Vs. Temperature



## A.C. Characteristics $T_A = 0^\circ C$ to $70^\circ C$ , $V_{CC} = 5V \pm 5\%$ , unless otherwise specified.

### READ CYCLE

Symbol	Parameter	5101L-1 Limits (ns)		5101L and 5101L-3 Limits (ns)	
		Min.	Max.	Min.	Max.
$t_{RC}$	Read Cycle	450		650	
$t_A$	Access Time		450		650
$t_{CO1}$	Chip Enable ( $\overline{CE1}$ ) to Output		400		600
$t_{CO2}$	Chip Enable ( $\overline{CE2}$ ) to Output		500		700
$t_{OD}$	Output Disable to Output		250		350
$t_{DF}$	Data Output to High Z State	0	130	0	150
$t_{OH1}$	Previous Read Data Valid with Respect to Address Change	0		0	
$t_{OH2}$	Previous Read Data Valid with Respect to Chip Enable	0		0	

### WRITE CYCLE

$t_{WC}$	Write Cycle	450	650
$t_{AW}$	Write Delay	130	150
$t_{CW1}$	Chip Enable ( $\overline{CE1}$ ) to Write	350	550
$t_{CW2}$	Chip Enable ( $\overline{CE2}$ ) to Write	350	550
$t_{DW}$	Data Setup	250	400
$t_{DH}$	Data Hold	50	100
$t_{WP}$	Write Pulse	250	400
$t_{WR}$	Write Recovery	50	50
$t_{DS}$	Output Disable Setup	130	150

## A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and  $C_L = 100pF$

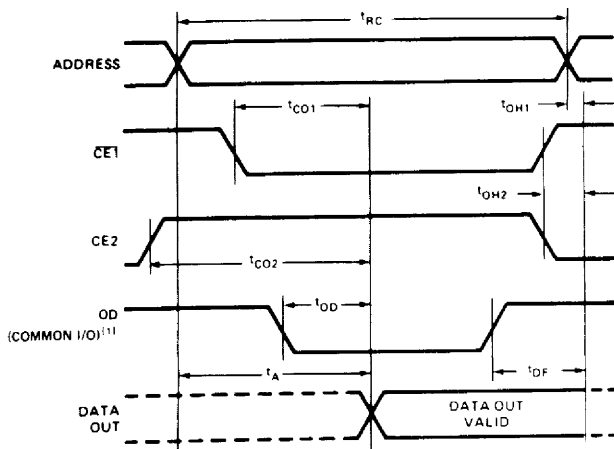
## Capacitance<sup>[2]</sup> $T_A = 25^\circ C$ , $f = 1 MHz$

Symbol	Test	Limits (pF)	
		Typ.	Max.
$C_{IN}$	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
$C_{OUT}$	Output Capacitance $V_{OUT} = 0V$	8	12

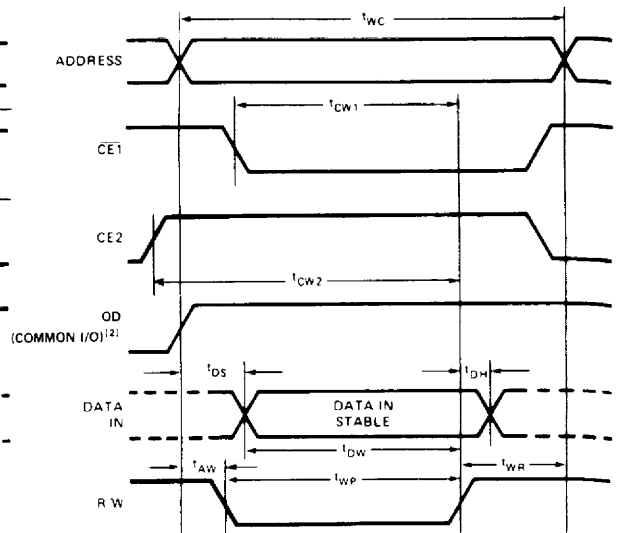
NOTES: 1. Typical values are for  $T_A = 25^\circ C$  and nominal supply voltage.  
2. This parameter is periodically sampled and is not 100% tested.

# Waveforms

## READ CYCLE



## WRITE CYCLE



### NOTES:

1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.