Document No.	853–0148
ECN No.	86487
Date of Issue	November 11, 1986
Status	Product Specification
Memory Products	

82S126
82S129
1K-bit TTL bipolar PROM

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 2 Chip Enable inputs for ease of memory expansion. They feature either Open Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S126 and 82S129 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.
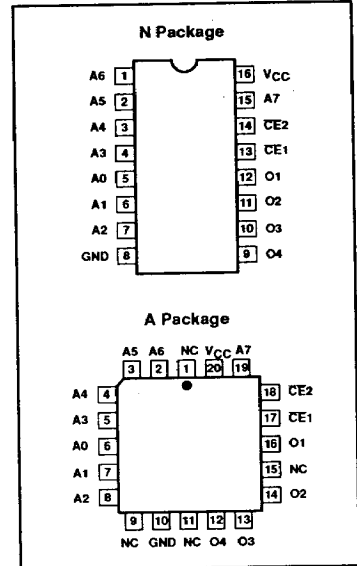
FEATURES

- Address access time: 50ns max
- Power dissipation: 0.5mW/bit typ
- Input loading: −100μA max
- On-chip address decoding
- Two Chip Enable inputs
- Output options:
  - N82S126: Open Collector
  - N82S129: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
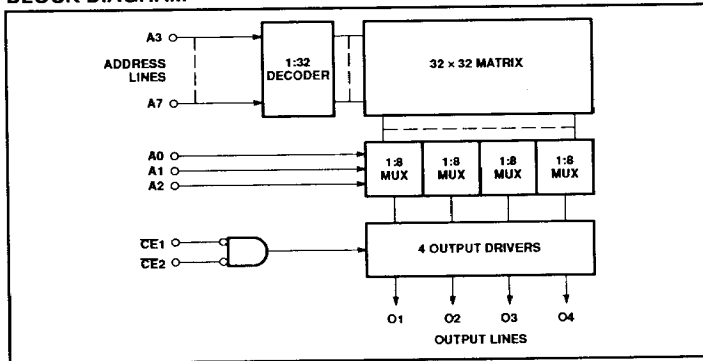- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

PIN CONFIGURATIONS

N Package

A6 1	16 Vcc
A5 2	15 A7
A4 3	14 CE2
A3 4	13 CE1
A0 5	12 O1
A1 6	11 O2
A2 7	10 O3
GND 8	9 O4

A Package

BLOCK DIAGRAM

ADDRESS LINES A3 ... A7 → 1:32 DECODER → 32 × 32 MATRIX

A0 A1 A2 → 1:8 MUX 1:8 MUX 1:8 MUX 1:8 MUX

CE1 CE2 → 4 OUTPUT DRIVERS

O1 O2 O3 O4 OUTPUT LINES

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1K-bit TTL bipolar PROM (256 × 4)

82S126 / 82S129

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Plastic Dual-In-Line 300mil-wide	N82S126 N, N82S129 N
20-Pin Plastic Leaded Chip Carrier 350mil-square	N82S126 A, N82S129 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH}	Output voltage High (82S126)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S129)	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			MIN	TYP[3]	MAX	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	$I_{IN} = -12mA$			-1.2	V
Output voltage						
V_{OL}	Low	$\overline{CE}1,2 = Low$ $I_{OUT} = 16mA$			0.45	V
V_{OH}	High (82S129)	$I_{OUT} = -2.0mA$	2.4			V
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			-100	µA
I_{IH}	High	$V_{IN} = 5.5V$			40	µA
Output current						
I_{OLK}	Leakage (82S126)	$\overline{CE}1$ or $\overline{CE}2 = High$, $V_{OUT} = 5.5V$			40	µA
I_{OZ}	Hi-Z state (82S129)	$\overline{CE}1$ or $\overline{CE}2 = High$, $V_{OUT} = 5.5V$			40	µA
		$\overline{CE}1$ or $\overline{CE}2 = High$, $V_{OUT} = 0.5V$			-40	µA
I_{OS}	Short circuit (82S129)[4]	$\overline{CE}1,2 = Low$, $V_{OUT} = 0V$, High stored	-15		-70	mA
Supply current[5]						
I_{CC}		$V_{CC} = 5.25V$			120	mA
Capacitance						
C_{IN}	Input	$\overline{CE}1$ or $\overline{CE}2 = High$, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		pF

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
4. Duration of short circuit should not exceed 1 second.
5. Measured with all inputs grounded and all outputs open.

1K-bit TTL bipolar PROM (256 × 4)   82S126 / 82S129
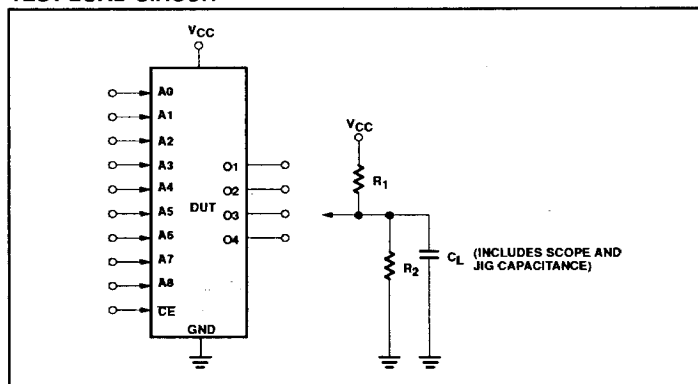
AC ELECTRICAL CHARACTERISTICS
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				MIN	TYP[1]	MAX	
Access time[2]							
t_{AA}		Output	Address		40	50	ns
t_{CE}		Output	Chip Enable			25	ns
Disable time[3]							
t_{CD}		Output	Chip Disable			25	ns

NOTES:
1. Typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. Tested at an address cycle time of 1µs.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.

TEST LOAD CIRCUIT

VOLTAGE WAVEFORMS

All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.