576-BIT BIPOLAR RAM (64×9) 82S09/82S19 (O.C.)

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/19 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

The 82S09/19 is available in the commercial and military temperature ranges. For the commercial temperature ranges (0°C to +75°C) specify N82S09/19, F or N and for the military temperature range (−55°C to +125°C) specify S82S09/19 I, R or F.

FEATURES

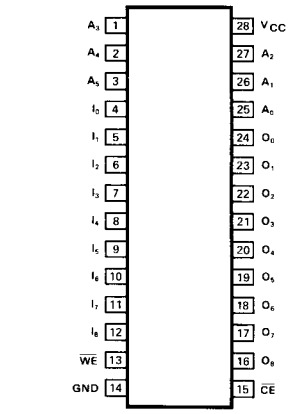
- **Address access time:**
  - **N82S09: 45ns max**
  - **S82S09: 80ns max**
  - **N82S19: 35ns max**
  - **S82S19: 60ns max**
- **Write cycle time:**
  - **N82S09/19: 45ns max**
  - **S82S09: 80ns max**
  - **S82S19: 70ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  - **N82S09/19: −100μA max**
  - **S82S09/19: −150μA max**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**
- **82S09 Output is Non-Blanked During Write**
- **82S19 Output is Blanked During Write**

APPLICATIONS

- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION

R,F,I,N PACKAGE*



F = Cerdip
N = Plastic
I = Ceramic
R = Flat Pak

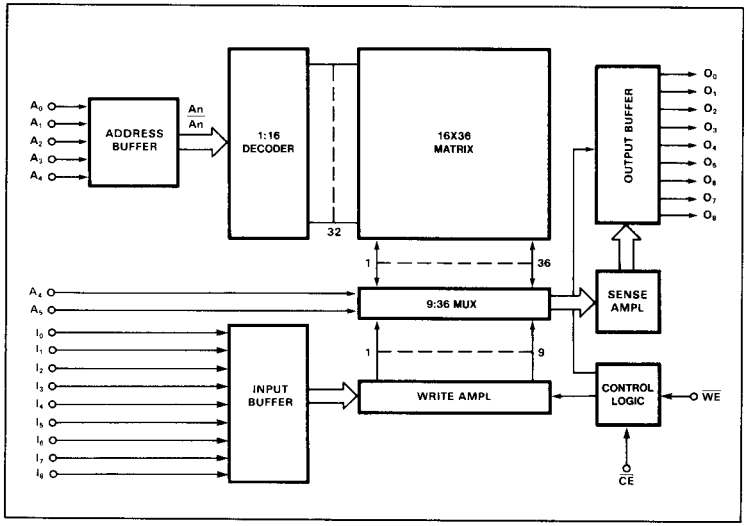
TOP VIEW

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	$\overline{O}_N$	
				82S09	82S19
Read	0	1	X	Complement of data stored	
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	1
Disabled	1	X	X	1	1

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
T_A	Temperature range		°C
	Operating		
	N82S09/19	0 to +75	
	S82S09/19	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS[1,7]

N82S09/19: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S09/19: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER[1]		TEST CONDITIONS	N82S09/19			S82S09/19			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.2			
V_{IC}	Clamp[2]	V_{CC} = Min, I_{IN} = −12mA			−1.5			−1.5	
	Output voltage								V
V_{OL}	Low[3]	V_{CC} = Min, I_{OL} = 8.0mA			0.5			0.5	
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			25			40	
	Output current								μA
I_{OLK}	Leakage[4]	V_{CC} = Max, V_{OUT} = 5.5V			40			60	
I_{CC}	V_{CC} supply current[5]	V_{CC} = Max			190			200	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

Refer to notes on next page.

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AC ELECTRICAL CHARACTERISTICS[7]

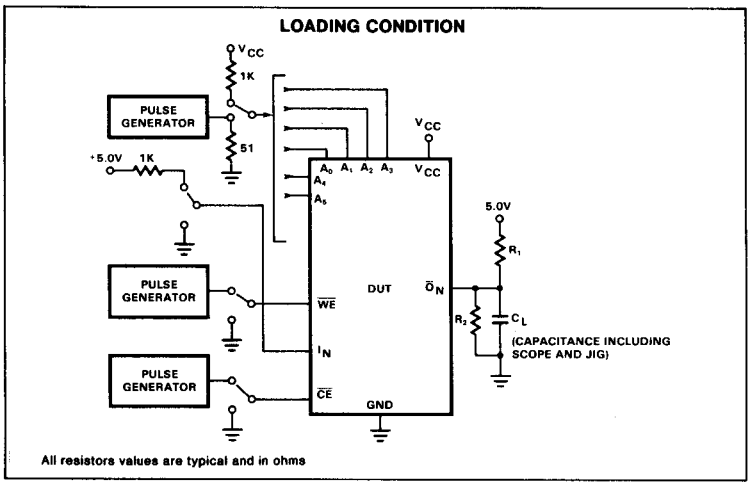
$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, for 82S09
$R_1 = 510\Omega$, $R_2 = 750\Omega$, $C_L = 30pF$, for 82S19
N82S19: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S19: $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TO	FROM	N82S09			S82S09			N82S19			S82S19			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Access time															ns
T_{AA}	Address					45			80			35			60	
T_{CE}	Chip enable					30			50			25			40	
T_{CD}	Disable time	Output	Chip enable			30			50			25			35	ns
T_{WD}	Valid time	Output	Write enable			50			80			25			50	ns
T_{WR}	Write recovery time	Output	Write enable									25			50	
	Setup and hold time															ns
T_{WSA}	Setup time	Write enable	Address	5			10			5			10			
T_{WHA}	Hold time			5			20			5			10			
T_{WSD}	Setup time	Write enable	Data in	35			50			30			45			
T_{WHD}	Hold time			5			5			5			5			
T_{WSC}	Setup time	Write enable	$\overline{CE}$	5			10			5			10			
T_{WHC}	Hold time			5			10			5			10			
	Pulse width															ns
T_{WP}	Write enable[6]			35			50			35			50			

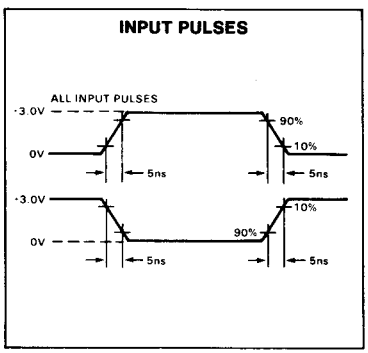
NOTES

1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT

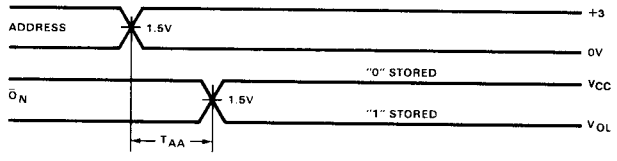


VOLTAGE WAVEFORM

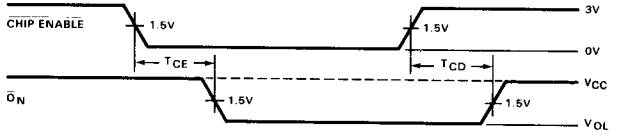


TIMING DIAGRAMS

READ CYCLE

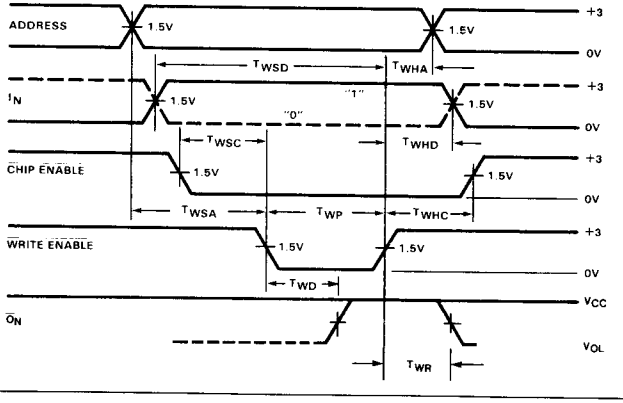


Address Access Time

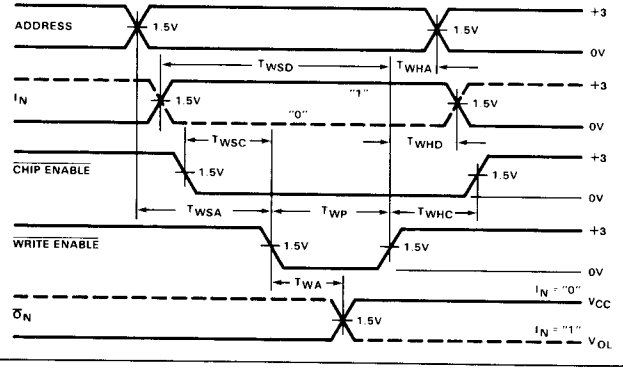


Chip Enable/Disable Times

WRITE CYCLE/82S19



WRITE CYCLE/82S09



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output goes high (blanks).
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)
T_{WA}	Delay between beginning of Write Enable pulse and when data output reflects complement of data input.