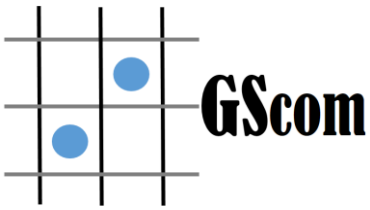

Decision Feedback Equalizer (DFE) combined with Carrier Recovery

Table of Contents

1. Introduction
2. Equalization
3. Carrier Recovery
4. Performance Evaluation
    4.1 Performance Evaluation Summary

1. Introduction

The need to increase the channel data rate in data communication systems without increasing the signal bandwidth drives the development toward more spectrally efficient modulation formats. QAM modulation is widely used in digital wireless communication systems for achieving high data transmission rates over relatively narrow signal bandwidth. Digital radio systems designed using such modulation schemes must balance the effects of phase noise from local oscillators with the demodulator parameters in determining overall performance. In an M-QAM system each symbol transmitted contains k bits, where $2^k = M$. In contrast, BPSK (binary phase shift keying) system transmits 1 bit per symbol and QPSK (quadrature phase shift keying) system transmits 2 bits per symbol while requiring the same RF (radio frequency) bandwidth for a given symbol rate.

The M states in high order M-QAM constellations are more closely spaced than in BPSK or QPSK constellations and therefore require lower noise relative to the average carrier power to eliminate errors. The RMS (root mean square) phase noise of the local oscillators, after being filtered by a demodulator, must be sufficiently low to not cause bit errors. For QPSK or M-PSK schemes (or systems), a multitude of carrier recovery algorithms exist that provide a high phase noise tolerance. However, these algorithms fail when applied to most of the higher order QAM constellations because these lack equidistant phases. Additionally, it has been shown that most of decision-directed carrier recovery is also not a viable option for higher order QAM constellations due to the inevitable relatively long feedback delay (or latency) in practical systems.

Phase noise is one of the most critically destructive noises affecting the performance of wireless high speed communication systems. In the general application area, a higher speed communication system requires the use of a higher order QAM (quadrature amplitude modulation) system. We need to use more accurate and more recently measured (i.e., low latency) phase noise estimates for a higher order QAM to mitigate the phase noise effect on the

signal. The present invention provides an effective phase noise mitigation approach with good accuracy and very low latency.

The present invention provides a phase noise tolerant method with very low latency by effectively combining the decision feedback equalizer (DFE) and the carrier recovery loop.

2. Equalization

Equalization is used to mitigate the channel effect on the received signal for clear communication. The equalizer estimates the communication channel distortion (such as amplitude distortion, phase distortion, fading, and interference, etc.) and mitigates the channel effect.

In micro-wave or millimeter wave communications which uses high carrier radio carrier frequency, the equalizer combined with the carrier recovery is one of the most powerful solutions to fight against phase noise through the latency reduction between phase noise estimation and correction.

We use a fractionally spaced decision feedback equalizer (DFE) to mitigate channel effect and inter-symbol interference. The DFE consists of two sections in the equalizer- the first is a Feed Forward Filter (FFF) and the second is a Feedback Filter (FBF). The FFF consists of a 24-tap or 32-tap T/2 spaced finite impulse response (FIR) filter (where T is a symbol interval). The FBF consists of a 4-tap or 5-tap T spaced FIR filter. In general, the number of taps used is determined by the modulation order (or symbol rate) that is used.

Figure.1 is the functional block diagram of the DFE which gets the phase noise estimate from the carrier recovery loop. The input signal of the DFE, u(n) , is the transmitted signal sent through the noisy communication channel which is received at the receiver. This is a noisy signal. The output signal, q(n), of the DFE is the summation of the output signal of the FFF and the output signal of the FBF in the adder. The output signal, $\hat{\mathrm{d}}(\mathrm{n})$, of the Decision Device (DD) is used in the decoder.

The phase noise correction (or compensation) is obtained by multiplying the respective input signal of the DFE, u(n), and the output signal, q(n), of the DFE with the negative value of the phase noise estimate, which is obtained from the carrier recovery DPLL (digital phase locked loop) in the multipliers, respectively. The phase noise compensated signal, Q(n), is the input of the DD. The DD uses the input signal, Q(n), to find its output from the M-QAM constellation by finding one of the M signal constellation points which is the closest to the input signal, Q(n), and selects the closest signal point to Q(N) as the output signal, $\hat{d}(\mathbf{n})$, of the DD. The error signal, e(n), is obtained by subtracting the output signal, $\hat{d}(\mathbf{n})$, from the input signal, Q(n), of

the DD. We also obtain the SNR estimate by applying a signal and noise energy measurement algorithm at the output of DD in DFE.

For equalizer operation perspectives, we use preamble symbols which are in the Acquisition Frame as a training sequence for equalizer during Acquisition mode before the data mode operation (Pease refer to Acquisition Frame Format in section 3.4.3.2 in the white paper of "Broadband wireless modem" system description document).

For equalizer operation perspectives for data mode, we use preamble symbols and pilot symbols which are in the Data Frame for the channel estimation and mitigation purpose (Pease refer to Data Frame Format in the white paper of "Broadband wireless modem" system description document).

We use a least mean square (LMS) algorithm for the filter coefficient updates in both the FFF and the FBF filters. The step size (μ) used for the filter coefficient updates in the LMS algorithm is programmable.

The following Figure 1 is the equalizer functional block diagram.

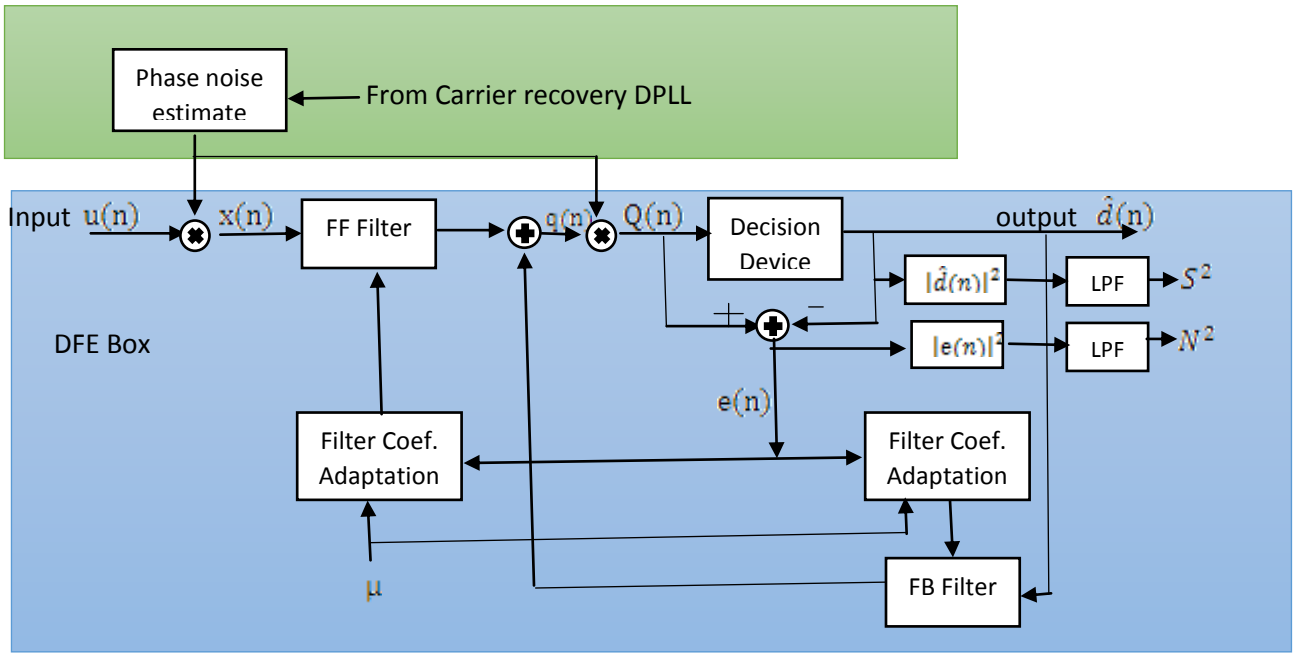

Figure 1. Functional Block Diagram of Decision Feedback Equalizer

The Feed Forward Filter (FFF) is a T/2 spaced complex asymmetric FIR filter (where T is a symbol interval). The FFF performs a decimation-by-2 function where two symbols are shifted in for each symbol produced at the output of the FFF. The FFF supports either 24 or 32 complex coefficients depending on the modulation order used. The Feedback Filter (FBF) is an adaptive T spaced complex filter. The filter has four or five complex filter coefficients depending on the modulation order used.

The input and output of DFE, phase noise compensated DFE output signal $\mathrm{Q(n)}$, data estimate, and its error can be calculated as follows (as can be seen in figure 1):

Output of DFE: $\mathrm{q(n)} = \sum_{k=1}^{K} f_k(n) x_k(n-k) + \sum_{l=1}^{L} b_l(n) \hat{d}_l(n-l)$

Phase noise compensated DFE output: $\mathrm{Q(n)} = \mathrm{q(n)}\, e^{-j\hat{\theta}_n}$

Data estimate: $\hat{d}(n) = \mathrm{Demap}\ (\ \mathrm{Q(n)}\ )$

Error estimate: $\mathrm{e(n)} = Q(n) - \hat{d}(n)$,

Where, K and L are the filter order of the FFF and the FBF respectively, and $\hat{\theta}_n$ is the phase noise estimate obtained from the carrier recovery loop.

The signal to noise ratio (SNR) estimate is obtained by applying the time average of the data estimate ($\hat{d}(n)$), and the error estimate ($\mathrm{e(n)}$), using a 1-pole IIR (infinite impulse response) filter as follows:

Signal energy: $S^2(n) = \alpha S^2(n-1) + (1-\alpha)\hat{d}(n)\hat{d}^*(n) = \alpha S^2(n-1) + (1-\alpha)|\hat{d}(n)|^2$

Noise energy: $N^2(n) = \alpha N^2(n-1) + (1-\alpha)e(n)e^*(n) = \alpha N^2(n-1) + (1-\alpha)|e(n)|^2$

SNR estimate: $\mathrm{SNR} = 10 * \log10\ (\ S^2(n)/N^2(n)\ )$,

Where, α is an average parameter and is the pole of a 1-pole IIR filter. Its value is $0 < \alpha < 1$ and is close to 1.

The decision directed LMS, where the filter coefficients are adapted to minimize the Mean Squared Error (MSE) at the Decision Device (DD) input, is used in this application. The filter coefficient adaption (or update) is performed as follows for both the FF and the FB filters, respectively:

$$f_k(n+1) = f_k(\mathrm{n}) + \mu * \mathrm{e(n)} * x_k(\mathrm{n}), \qquad \mathrm{k} = 1,2,\ldots.,\mathrm{K}$$

$$b_l(n+1) = b_l(\mathrm{n}) + \mu * \mathrm{e(n)} * \hat{d}_l\ (\mathrm{n}), \qquad l = 1,2,\ldots.,\mathrm{L}$$

Where,

f_k(n) and $f_k(n+1)$ are the present k^{th} FF filter coefficient and the next k^{th} FF filter coefficient, respectively.

And,

b_l(n) and $b_l(\mathrm{n}+1)$ are the present l^{th} FB filter coefficient and the next l^{th} FB filter coefficient, respectively.

And,

x_k(n) and $\hat{d}_l$(n) are the input of the k^{th} filter coefficient of the FFF and the input (or the output of FFF) of the l^{th} filter coefficient of the FBF, respectively.

3. Carrier Recovery

The carrier synchronization loop tracks the phase error at the input of the decision device (DD) in the decision feedback equalizer (DFE). The carrier synchronization loop is a 2nd order type II digital phase locked loop (DPLL) operating at the symbol rate. The phase error estimate is obtained from the phase difference between the input and output of the decision device and is decision directed. Figure 2 is the functional block diagram of the carrier recovery loop (CRL) combined with the part of the DFE that is designed for joint detection, estimation, and compensation of the phase noise. The CRL tracks the phase error at the input of the DD in the DFE.

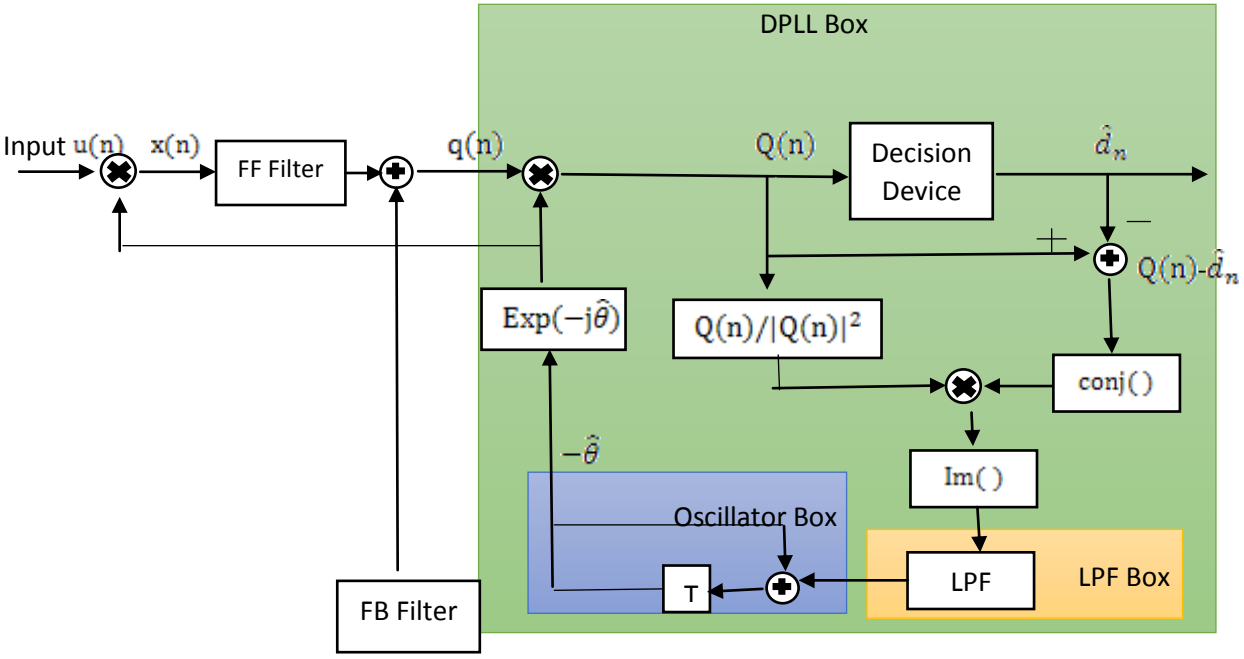

Figure 2. Carrier Synchronization Loop block diagram

The input signal of the DFE (u(n)), is the transmitted signal sent through the noisy communication channel and received at the receiver. This is a noisy signal. The $q(n)$ in the above Figure 2 is the output of the DFE and is supposed to be the transmitted data symbol (d), in the no noise communication environment. However, it is a data estimate which may include the noisy components in it. The phase noise correction (or compensation) is obtained by multiplying the respective input signal of the DFE (u(n)), and the output signal of the DFE (q(n)) , with the negative value of the phase noise estimate**,** which is obtained from the carrier recovery DPLL (digital phase locked loop). The phase noise compensated signal (Q(n)), is the input of the DD.

The $Q(n)$ is the phase noise compensated version of q(n) and can be represented as:

$Q(n) = q(n)\, e^{-j\hat{\theta}_{n-\Delta}} = \hat{d}_n e^{j\hat{\theta}_n}$, where $\hat{d}$ is the data estimate and $e^{j\hat{\theta}_n}$ is the phase noise.

As can be seen from Figure 2, the phase error estimate is obtained as follows:

$$Q(n) = \hat{d}\; e^{j\hat{\theta}_n}$$

$$E[\ (Q_n - \hat{d}_n)^*\, Q_n / \ |Q_n|^2\ ] = E[\ 1 - \ e^{j\hat{\theta}_n}\ ]$$

For a small phase noise error of $\hat{\theta}_n$, $E[\ \mathrm{Im}(1 - \ e^{j\hat{\theta}_n})\ ] \approx E[-\ j\hat{\theta}_n\ ]$

The Low-Pass-Filter (LPF) in the Digital Phase Locked Loop (DPLL) in Figure 2 has two signal paths in it. The first is the proportional path and the second is the integration path as shown in Figure 2 and described in the Symbol Timing Synchronization portion of section 3.4.3.1 in the white paper of the "Broadband wireless modem system document". As discussed before, the proportional path gain K_p and integration path gain K_i in the LFP determines the bandwidth of the carrier synchronization loop filter.

The carrier synchronization loop supports a range of loop bandwidths, designed to maximize the phase noise tracking capability and minimize the effect of the additive white Gaussian noise (AWGN). We need to optimize the loop bandwidth based on the expected-signal-to noise ratio (SNR) and phase noise.

4. Performance Evaluation

We carried out the performance test of the DFE combined with the carrier recovery in the dynamic range of the SNR of the additive white Gaussian noise and phase noise. We used two phase noise masks in the performance evaluation. The first is the one in the DVB-S2 specification and the second is the one obtained from the system development division in the one of the tier-1 company. The following tables show the phase noise masks of those two phase noise masks.

– **Phase Noise Mask for DVB-S2 (ETSI EN_302307)**

Frequency	100 Hz	1 KHz	10 KHz	100 KHz	1 MHz	> 10 MHz
Agg1 (typical) (dBc)	-25	-50	-73	-93	-103	-114
Agg2 (critical) (dBc)	-25	-50	-73	-85	-103	-114

– **Phase Noise Mask for Backhaul (Tier-1)**

Frequency	100 Hz	2 KHz	10 KHz	100 KHz	100 MHz
Agg (critical) (dBc)	-37	-37	-58	-88	-148

As can be seen from the above two noise masks, Tier-1's phase noise mask is more aggressive. We illustrate the performance result which we obtained by using Tier-1's phase noise mask in varying levels of SNR in this section.

We tested the performance of the DFE combined with the Carrier Recovery in the five levels of QAM modulation systems- 4QAM, 16QAM, 64QAM, 256QAM, and 1024QAM. We used several levels of signal to noise ratios to test the performance in each of the QAM modulation systems. The following table shows the performance improvement obtained, in each of the QAM modulation systems, using our system (DFE combined with carrier recovery) versus the system using the DFE only, with reference to the point where we can achieve 10^{-6} bit error rate (BER).

- **Performance Improvement due to DPLL**

4QAM	16QAM	64QAM	256QAM	1024QAM
0 dB	1dB	7 dB	6 dB	8 dB

4.1 Performance Evaluation Summary

- We used 1 DPLL to take care of the phase noise (PN). In a practical communication system, we would typically use an analog PLL on top of the DPLL, which would give us a few more dB of performance improvement.
- We achieved excellent performance of the phase noise mitigation when combining the DFE and the Carrier Recovery in terms of the signal quality recovery and the latency.