Automatic Gain Control
Systems Document

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1. General

Automatic Gain Control (AGC) is used to accommodate a wide dynamic range of input signal and to provide a constant level of signal to the communication system to make the communication system operate reliably and effectively. Usually receivers are required to operate at over a 100 dB dynamic range of signal in Point to Point (PTP) or Point to Multi Point (PMP) RF systems. For the future stage of the ASIC design and implementation, we may need to use a very limited number of bits in the A/D converter because of the required high sampling rate due to the high symbol rate in PTP systems.

2. Introduction

The AGC may be implemented in either digital or in analog circuitry. This document will describe the digital AGC, although most of the design philosophy and design approach can be applied to design analog AGC's as well. There are, in general, two design approaches for AGC's depending upon the application. The first one is to keep the output signal constant by using a simple AGC counter which is dependent on the relative differences between the input signal and the AGC reference value. The second one is the AGC which requires an absolute output signal level. This AGC design needs to keep the output of the VGA (variable gain amplifier) constant by keeping the sum of the input power, the LNA (low noise amplifier) gain, and the VGA input constant. In this approach, we need to make sure that the numerical control signal matches the physical signal level consistently. The AGC required in wireless backhaul systems belong to the second criteria of the above AGC.

There are two parameters that describe the AGC from the data communication perspective. One is the speed of the control loop and the second is the size of the discrete amplification step. We will use these two parameters to meet one of the requirement specs for the flat fading rate of 100dB/sec. In addition, there are three parameters associated with the A/D converter which include the number of bits required, the average level of the signal in the A/D converter range, and the accuracy of the AGC control.

AGC's need to cope with two types of signal fluctuations, one is for slow fading and the other is for fast fading. Slow fading is normally so slow that almost any kind of averaging will be adequate enough to mitigate the slow fading. There are two approaches to mitigate the fast fading. One is to average out the rapid fluctuations in the signal and the other is to follow the signal fluctuation speed with a very fast AGC circuit.

In a PTP system, a fast AGC should not impair the function of the receiver algorithms. Unless the AGC is capable of perfectly tracking the fast fading or fast block rate of 100dB/sec, we may have a headroom problem in the AGC and the signal will be clipped by the A/D converter. The fast AGC will however impair the soft information collected for decoding. For this case, we may need to use weighting with RSSI (received signal strength information). For backhaul communication systems, the AGC time constant will be 1.25 ms and may not impact the performance in the estimation of the fine delay as long as the estimation is done within a 1 millisecond.

3. Functional Description

3.1. General Description

The AGC power control loop consists of an antenna, LNA, VGA and AGC loop. The received input signal passes through the antenna, LNA, and the input of the VGA. The VGA has two inputs, one from the LNA directly or indirectly, and the other from the output of the AGC. In general, the output signal from the AGC is used to control the VGA input signal from the LNA to keep the VGA output signal constant. Fig.1 models the general AGC loop diagram representing the LNA and VGA as summation nodes.

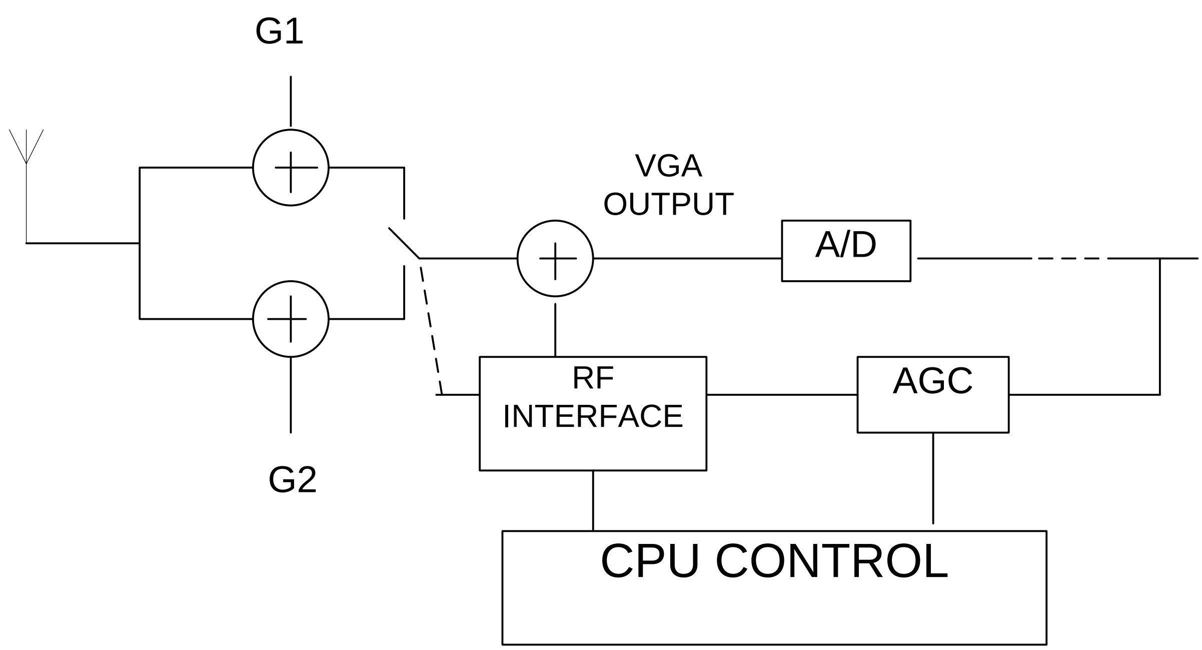

Fig. 1 AGC Loop System Diagram

From the power level perspective, we can summarize the signal flow as follows:

$P_{IN} + G_{LNA} + G_{VGA}$ = VGA OUT = Constant

Where, P_{IN}= Input power from the antenna, G_{LNA}= LNA gain, G_{VGA}= VGA gain.

In other words, as the power of input signal changes, the gain of the VGA should change according to the change in the input power of the VGA. If the input of the VGA is increasing, the gain of the VGA should be decreased to keep its output constant. We use an AGC loop to control the gain of VGA, G_{VGA}.

The AGC control loop consists of a signal energy estimation block, an energy comparison block with AGC reference (or target), and a RF interface block. The signal energy estimation block estimates the input signal energy and then the energy estimate is used to compare with the AGC reference signal and the difference is used to estimate the input signal power of Pin (which is the received signal strength indicator (RSSI) or the AGC loop output power estimate). The RF interface block transforms the output of the power estimation block into the VGA control input signal, VGA_{IN}. The VGA_{IN} is used to control the VGA gain, G_{VGA}, to keep the output of the VGA constant.

4. AGC Design

The AGC design is performed in two steps. The first is the AGC parameter design and the second is the AGC loop parameter design.

4.1. AGC Parameter Design for backhaul System

Figure 2 is the functional block diagram of the AGC Loop and the RF interface. The input of the AGC is the output of the root raised cosine (RRC) channel filter which is a digital signal whose sample rate is 200MHz. The dynamic range of the input power which the AGC takes care of is 70 dB.

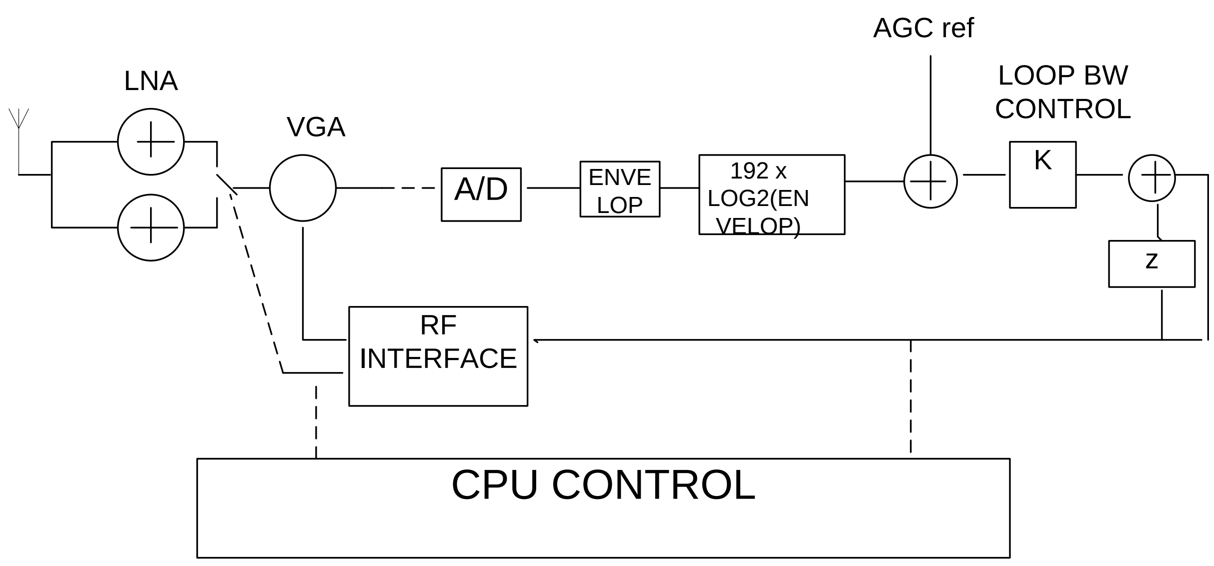

Figure 2 AGC Loop and RF Interface Block Diagram

The system requirements that the AGC should meet are as follows:

Maximum IF input signal level: -1 dBm

The output signal level of the equalizer: -20 dBm +/- 5 dB

The signal dynamic range that the AGC should cover: [-90 dBm -20 dBm]

Flat fading rate: 100 dB/sec

Dynamic range of the LNA gain: 36 dB

Sampling rate of the AGC input: 200MHz

As the output signal level is specified in the physical signal level, the output of the VGA needs to be able to provide a signal that matches with the -20 dBm +/- 5dB. This means that the AGC reference needs to be designed to match the physical power level of output signal of the equalizer. In other words, the AGC should be able to measure the physical input signal strength and then should be able to generate the physical output signal level accordingly.

From the above requirement, we can assign the AGC parameter as follows:

As the signal dynamic range is 70 dB and huge, the second logarithm of the signal envelope will be used to determine the number of bits required to accommodate the signal envelope in the AGC loop. Therefore, the number of bits needed to accommodate the above 70 dB dynamic range = 70 / 6 = 12 bits. We need an additional six bits (peak to peak) to satisfy the 18 dB head room margin requirement. As a result, we need 18 bits to accommodate the envelope of the input signal. The headroom needs to be optimized to get optimum performance with consideration of clipping noise and quantization noise in the signal envelope estimator.

For the AGC gain resolution and loop bandwidth the AGC gain resolution is designed to have 1/8 dB each step to supply a smooth signal gain transition. The AGC should be fast enough to track the flat fading rate of 100 dB per second. This means that we need to update at a minimum of 800 (= 100 / (1/8)) times the gain updating rate in each second of time. The updating rate of 800+ means that we need to update the AGC gain at least every 1.25 msec. This update interval is used to design the integration length of the signal envelope to a length of 1024 and the loop bandwidth parameter using a modulo-128 loop counter.

For the AGC Ref design the second logarithm of the sum of 1024 envelope samples is multiplied with the constant 192 in the input block of comparison function. The multiplication constant of 192 comes from the design concept to have 1/8 dB resolution in each of 8 dBm segments in the 70 dB dynamic range of the gain. The AGC Ref parameter is designed to use the value which is the second logarithm of the sum of 1024 envelope samples multiplied by 192 when the signal level is -20 dBm.

As a result, the AGC Ref is obtained as follows:

AGC_{ref} = 192 (Log2(N) + ENV(rms-bit)), where N is the number of input samples (or bits) in integrations (1024 in our design). ENV (rms-bit) is the rms (root mean squared) value of the Envelope signal and can be obtained from: ENV (rms-bit) = 0.5*Log2($I^2 + Q^2$), where I and Q are the in-phase and quadrature components of the input signal.

The meaning of head-room is the number of bits reserved to take care of the peak to peak signal component on top of the number of bits used to accommodate the rms (root mean squared) of the input signal. The head-room in terms of the number of bits can be obtained as follows:

Hr (bits) = ENV_{max} (rms-bit) – ENV (rms-bit) = 1/2Log2(2^{18}) – 1/2Log2(I^2+Q^2)

The head-room should be designed to get optimal performance of the system by performing the trade-off between the clipping noise and quantization noise in the A/D converter.

4.2. AGC Loop Operating Parameter Design

The power of the complex input is calculated once per sample integrated over N samples. As the AGC in the PTP system needs to accommodate the huge dynamic of the input signal power and high sampling rate of data, we need to use two efficient approximation approaches to save complexity of system. The first uses the envelope of the signal instead of using the sample power and the second uses the second logarithm of the energy estimate. We also could use the Taylor's approximation of the envelope (this can be seen as an absolute value of the complex signal). To achieve the equal change rate between the cases of increasing power amplification and of decreasing power amplification, the power of the input signal is not used. Instead, the second logarithm of the signal power is used. The second logarithm provides a pretty good estimate, with less than 0.3 dB accuracy loss, and requires minimal implementation complexity

Conversion Table between AGC output, real signal power and VGA input signal:

Index	**0**		**1**		**2**		**3**		**4**		**5**		**6**
RSSI (dBm)	**0**	**-4**	**-8**	**-12**	**-16**	**-20**	**-24**	**-28**	**-32**	**-36**	**-40**	**-44**	**-48**
AGC out	**0**	**32**	**64**	**96**	**128**	**160**	**192**	**224**	**256**	**288**	**320**	**352**	**384**
Stored values	2654	2526	2399	2271	2144	2016	1888	1761	1633	1506	1378	1251	1123
Gain	0.1	.1585	.2512	.398	.631	1.0	1.58	2.512	3.981	6.31	10	15.85	25.12

Index		7		8		9		10		11	
RSSI (dBm)	-52	-56	-60	-64	-68	-72	-76	-80	-84	-88	-90
AGC out	416	448	480	512	544	576	608	640	672	704	720
Stored values	996	868	740	613	485	358	230	103	-25	-153	-216
Gain	39.8107	63.0957	100	158.4893	251.1886	398.1072	630.9573	1000	1584.8932	2511.8864	3162.2777

CPU Control Unit

The CPU control signal will be designed during the implementation stage.

5. Performance Evaluation

5.1. AGC System Simulation

The purpose of using floating point simulation is to test the functionality, reliability and verification of the performance of the AGC system. The AGC system is designed to meet the requirement specification of the AGC which are as follows:

AGC dynamic range: 70 dB (from -20 dBm to – 90 dBm)

AGC signal level tracking speed: 100 dB/sec

AGC output signal level: -20 dBm +/-5dB

A random data signal whose variance is 1, with an average of 0, was used as the input signal to the (I) and (Q) channels for this simulation. The data signal was provided as the reference signal which matches the output signal level of -20dBm. Based on the reference signal level we used a proportional input signal gain to generate the desired input signal. For example, a gain of 10 was used to generate the 0dBm input signal, and a gain of 0.1 to generate the -40dBm input signal, respectively. The conversion table above was used to calculate the AGC gain after measuring the signal strength of the input signal. The gains in the conversion table are the gains which the AGC will pick up to keep the output signal level -20dBm after the AGC estimates the input signal level from the output of AGC loop. Figure 3 was obtained in the simulation by changing the input signal level (or input signal gain) as a function of time. As can be seen from the figure, the AGC gain increases with the same rate of slope as the input signal level (input signal gain) decreases to keep the AGC output signal at a constant level of -20dBm.

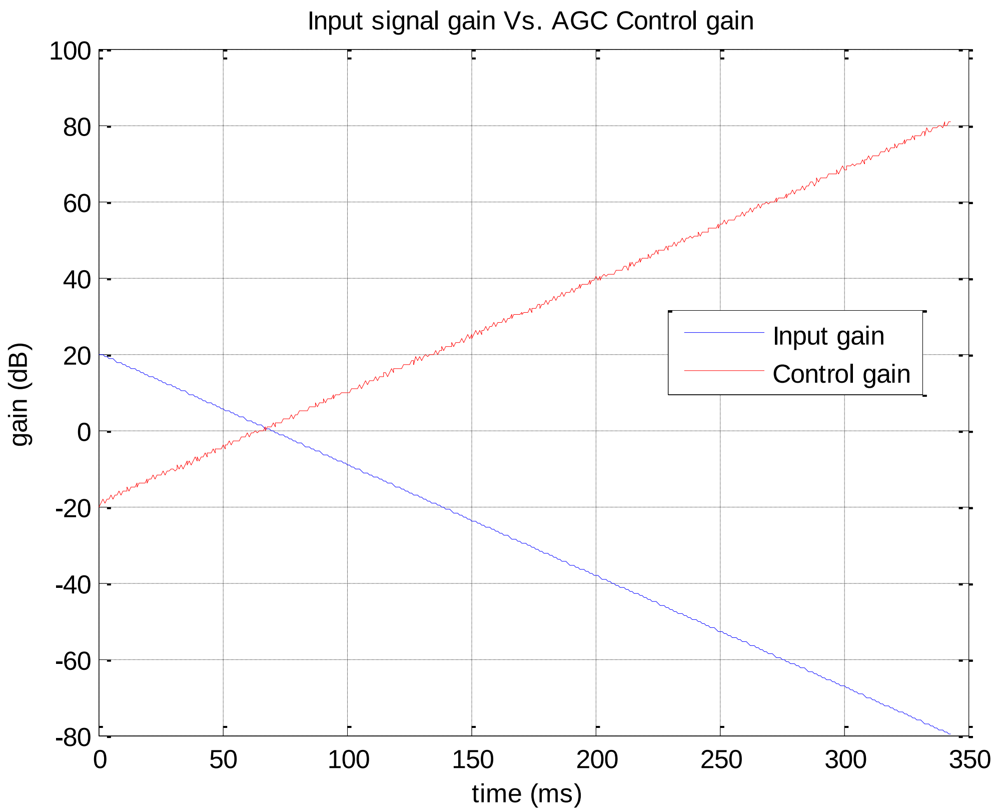

Figure 3: AGC gain (control gain) vs. Input signal level (input gain)

We measured the received signal strength of the input signal (RSSI) as a function of the input signal. Figure 4 shows the input signal level, its measured signal strength (RSSI) and the output signal level of the AGC. As can be seen in the figure, the RSSI matches the slope of the input signal and the output signal keeps at the level of -20dBm+/- 2dB regardless of the input signal level.

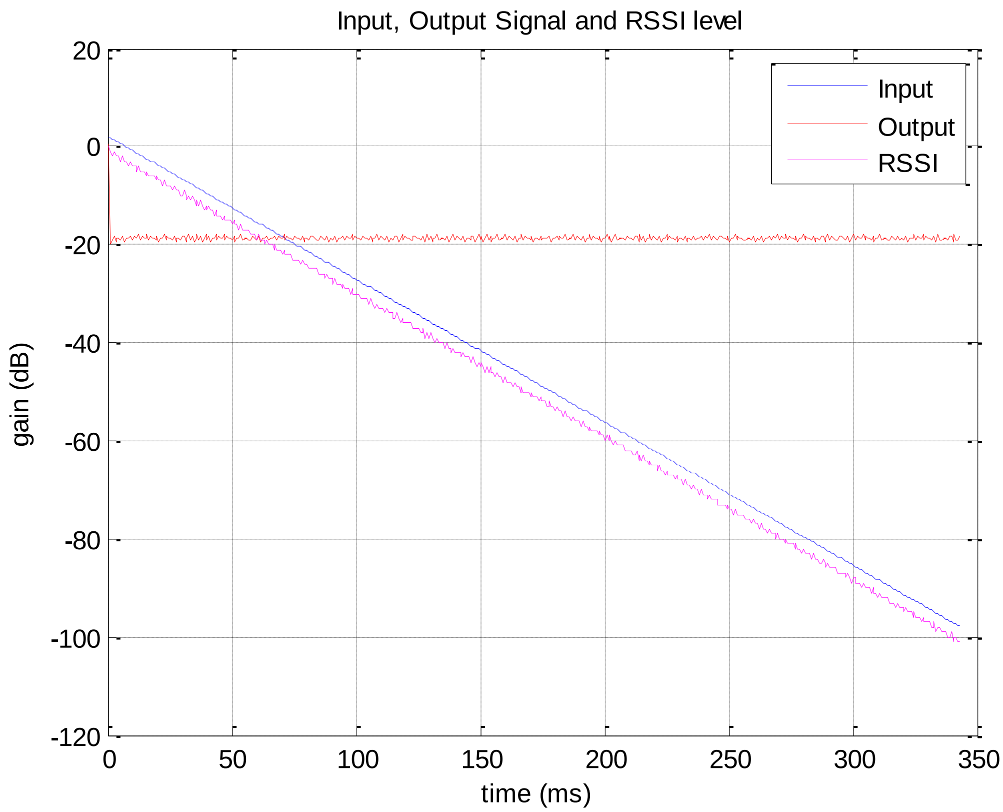

Figure 4: Input signal level, measured RSSI and AGC output signal level.

As can be seen from figures 3 and 4, the AGC can track the change of the input signal of 100dB/sec and the dynamic range of the AGC is over 90 dB. This simulation did not include the LNA which sits in the front end of the AGC. As a result, the dynamic range and the linearity of the AGC will be governed by the LNA. We are investigating the candidate of the LNA which we will use with the AGC designed. We need to design the analog input control signal from the measured RSSI to get maximum linearity and dynamic range of the AGC during the implementation phase.

Figure 5 shows the output signal level of the AGC and its measured signal strength (RSSI) from the AGC using the input signal level of -40 dBm when changing the signal levels. As can be seen in the figure, the RSSI measures the input signal level within the tolerance of +/- 1dB and the output signal keeps the level of -20dBm+/- 2dB regardless of the input signal level.

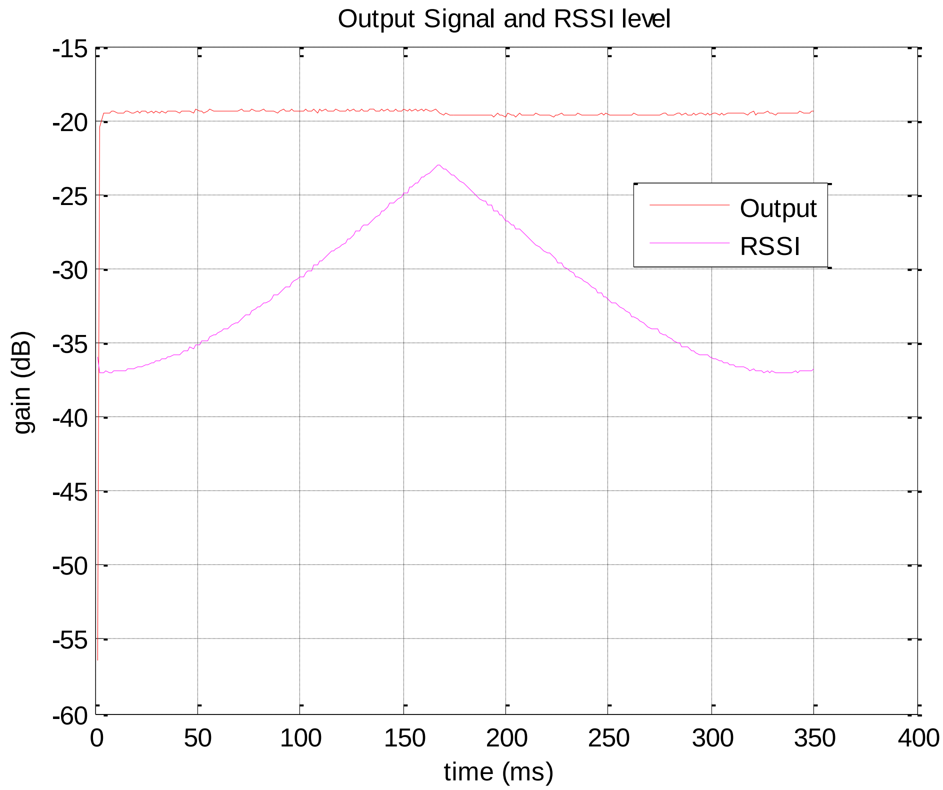

Figure 5: Measured RSSI and AGC output signal level.