

Analog Interfaces

Connecting analog world to digital computers

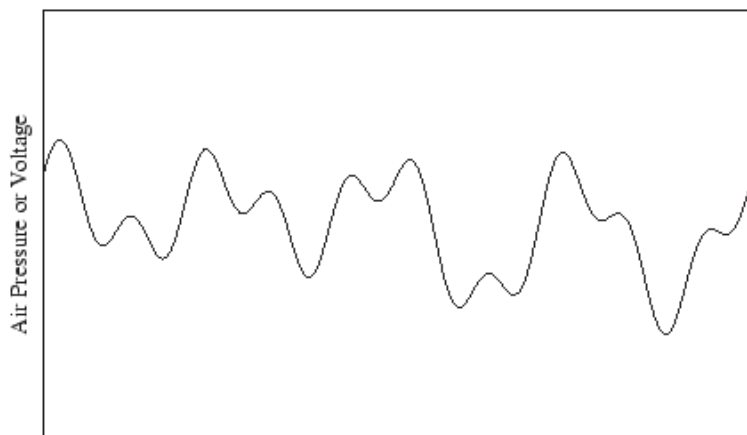
Dpt. Enginyeria de Sistemes, Automàtica i Informàtica Industrial

Some analog magnitudes



Barometer / altimeter
Air pressure.

An audio signal



Audio

...



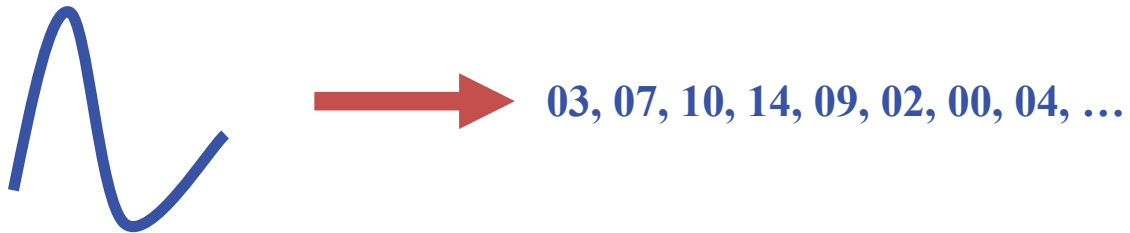
Temperature

Analog to Digital Conversion

World is analog ...

but computers deal with digital information.

ADC: Representing a continuously varying physical quantity by a sequence of discrete numerical values.



Basic of A/D Conversion

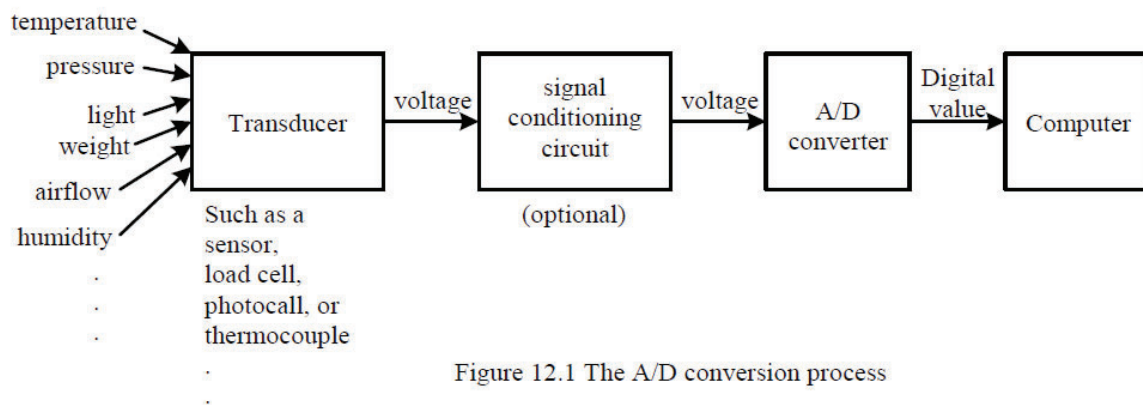
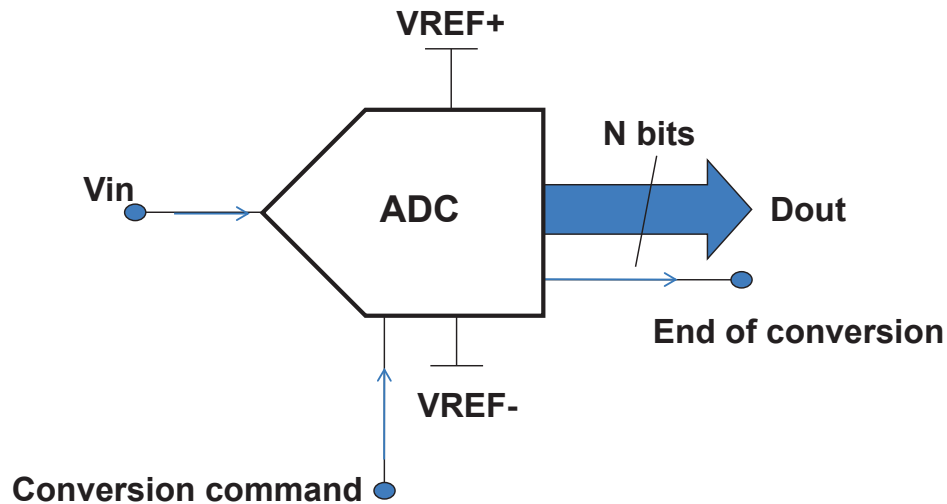


Figure 12.1 The A/D conversion process

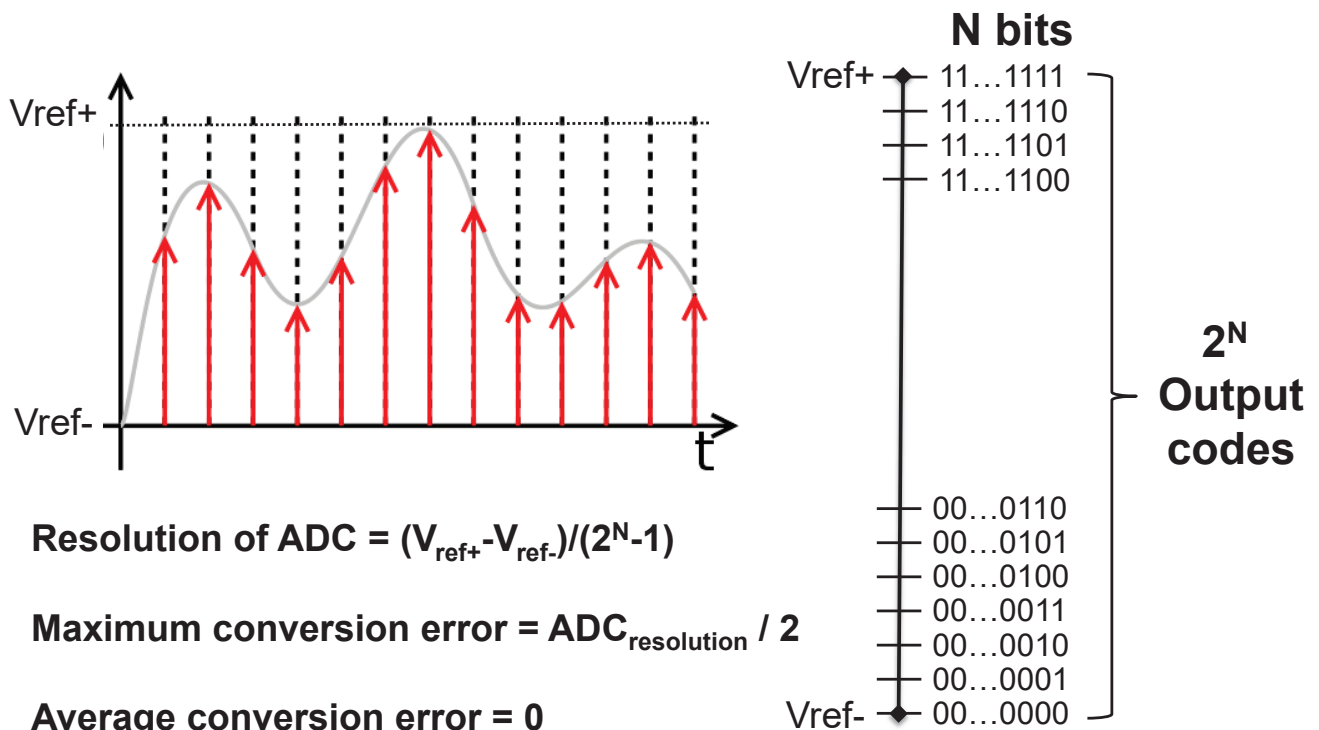
Analog to digital converter concept (ADC)

ADC Scheme (with a synchrony signal *End of conversion*)



$$D_{out} = \text{round} \left[(2^N - 1) \cdot \frac{(V_{IN} - V_{REF-})}{(V_{REF+} - V_{REF-})} \right]$$

Analog versus Digital



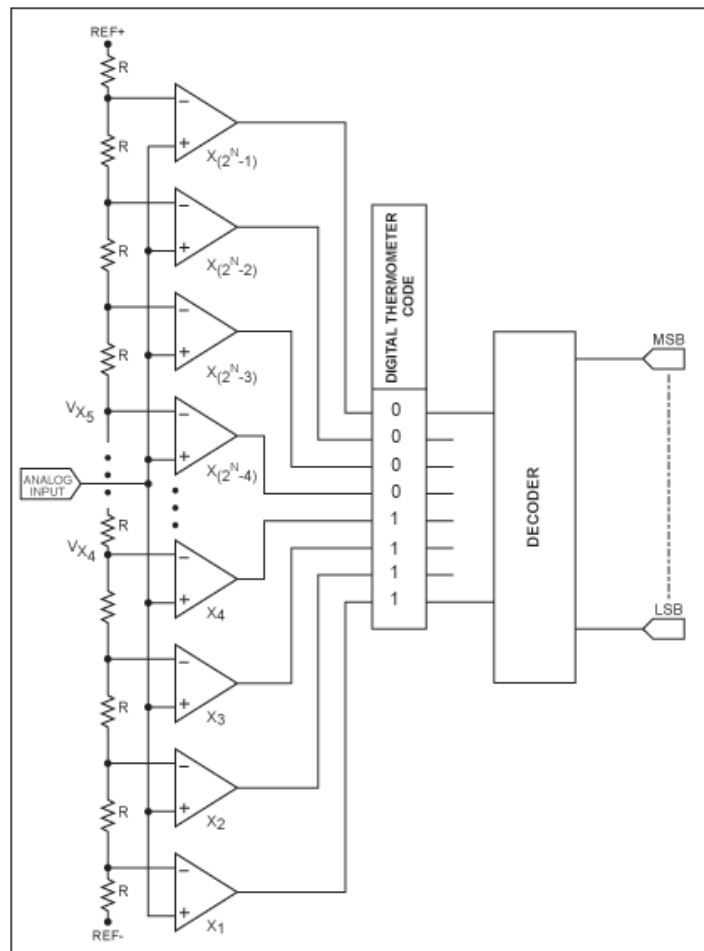
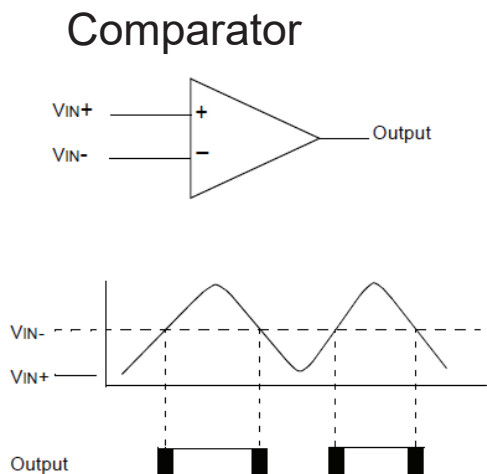
$$D_{out} = \text{round} \left[(2^N - 1) \cdot \frac{(V_{IN} - V_{REF-})}{(V_{REF+} - V_{REF-})} \right]$$

Devices

1. A/D Flash Converter
2. Digital to Analog Converter *
3. Slope A/D Converter
4. Successive approximations A/D Converter *

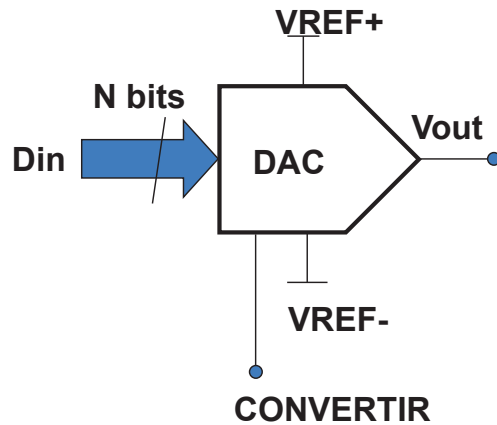
* These devices can be found on PIC18F45K22

1. A/D Flash



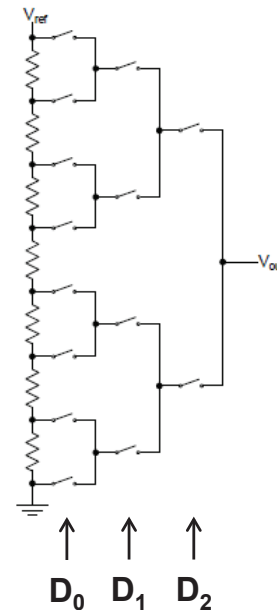
2. Digital to Analog Converter (DAC)

Symbol



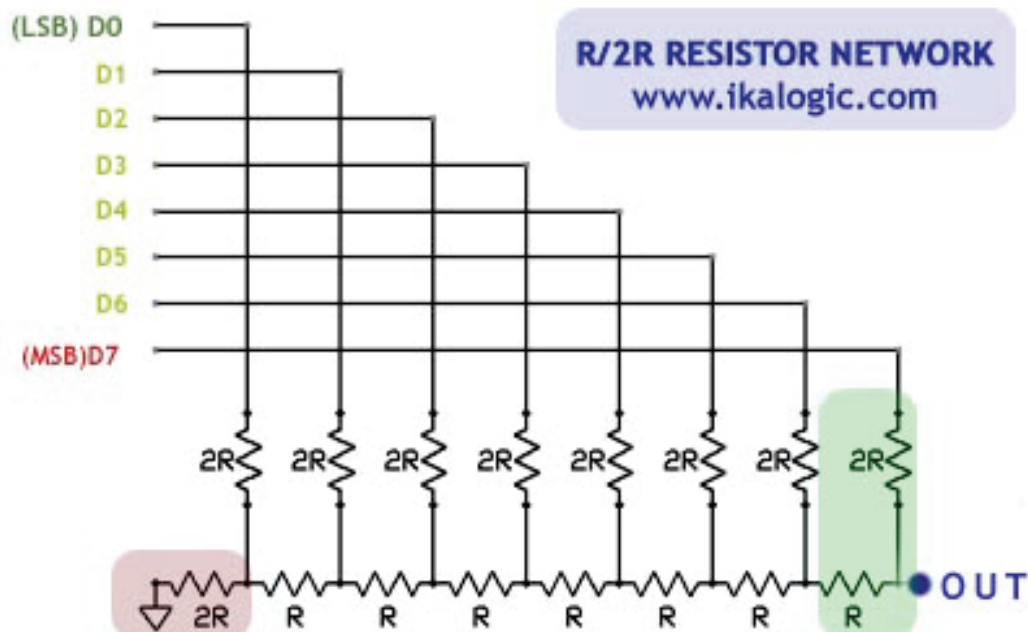
Possible implementation:

Resistor ladder (asymmetrical)

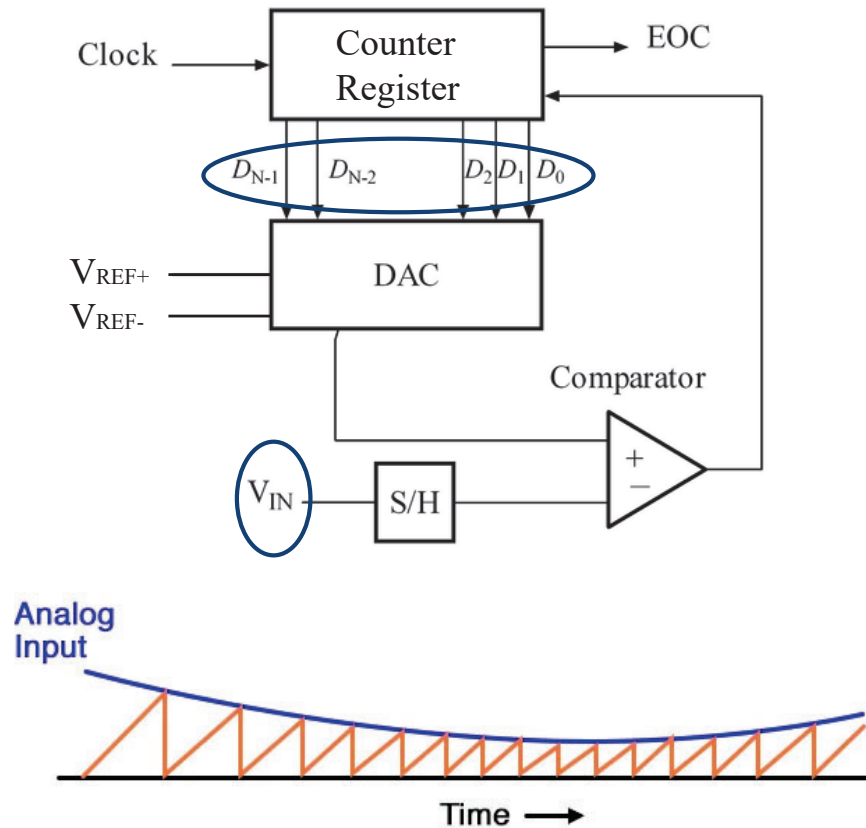


$$V_{out} = V_{REF-} + (V_{REF+} - V_{REF-}) \cdot \frac{D_{in}}{(2^N - 1)}$$

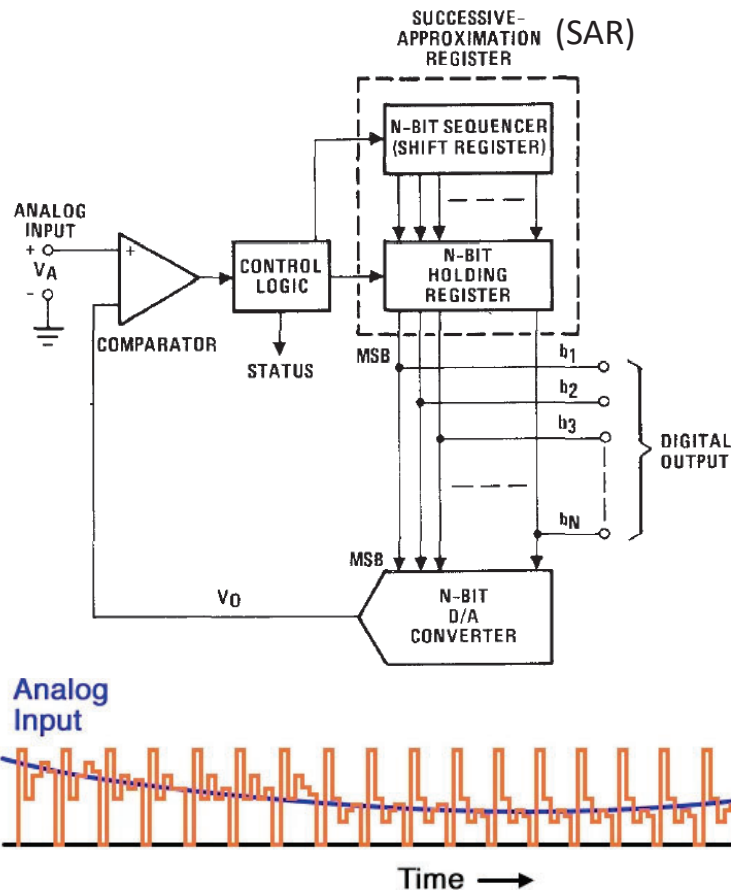
D/A Converter



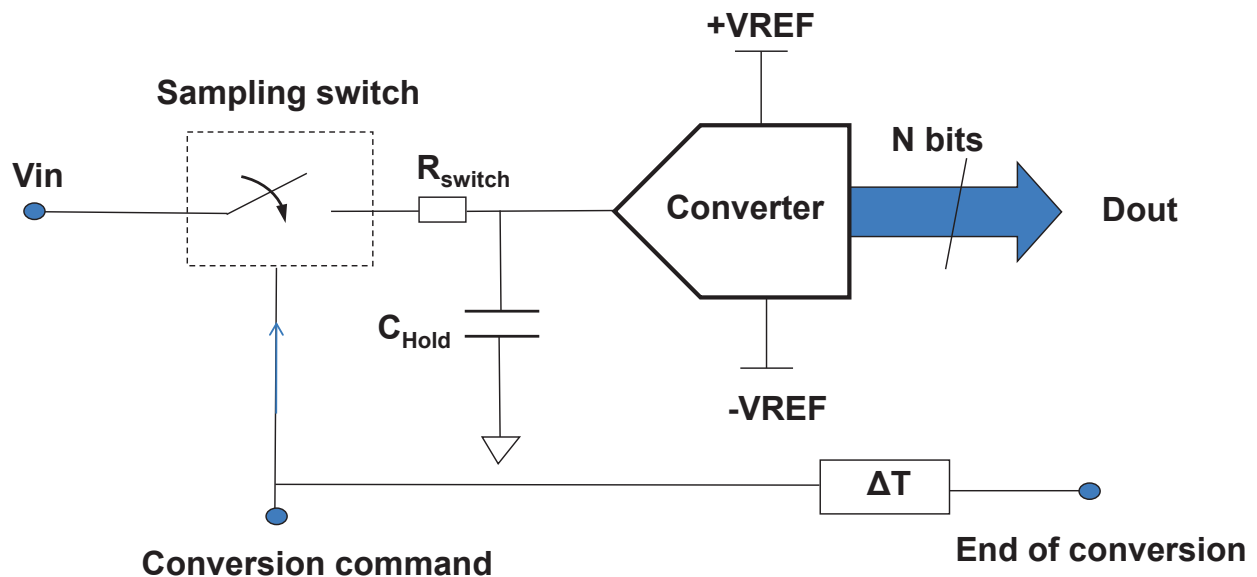
3. Slope A/D converter



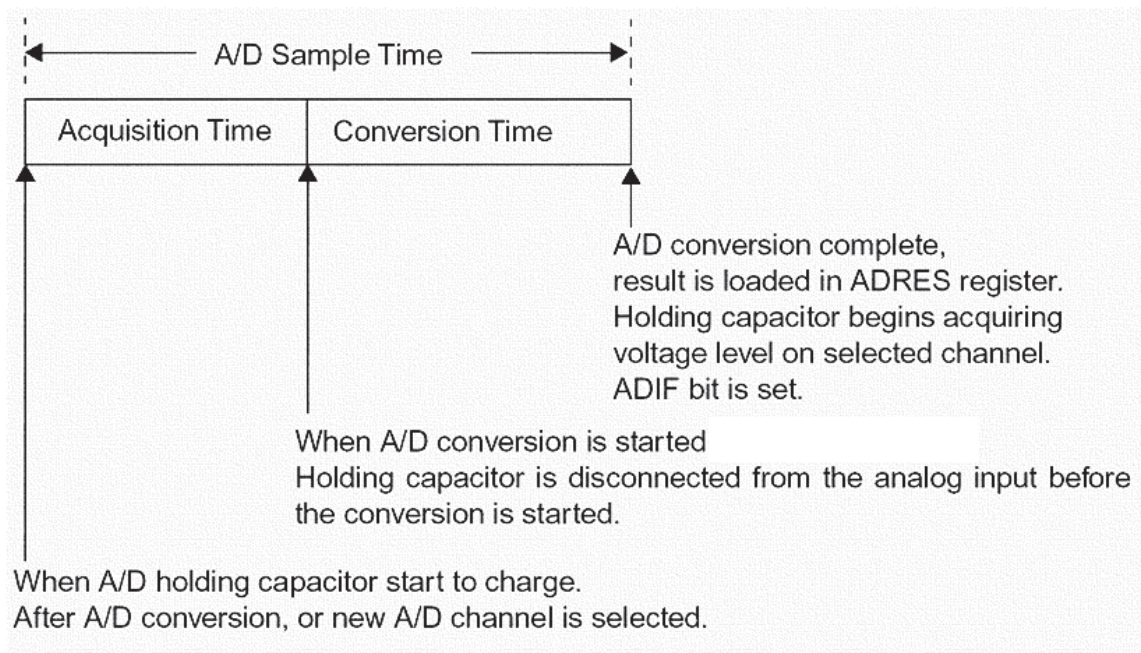
4. Successive approximations A/D Converter



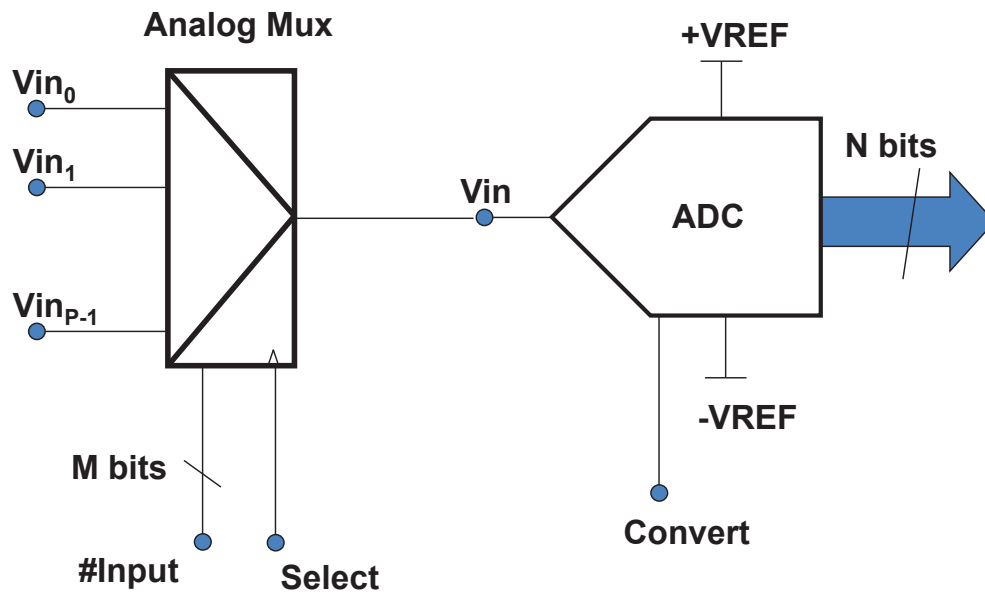
ADC: sample and hold + converter



Acquisition & Conversion times



Multiplexed inputs



Sensors and Resolution

Common usage of ADC is to read information from an analog sensor, to get the value of a physical magnitude (e.g. temperature, audio, etc.)

Sensors datasheet tell us how output voltage changes depending on measured magnitude. Usually is a linear function, defined by:

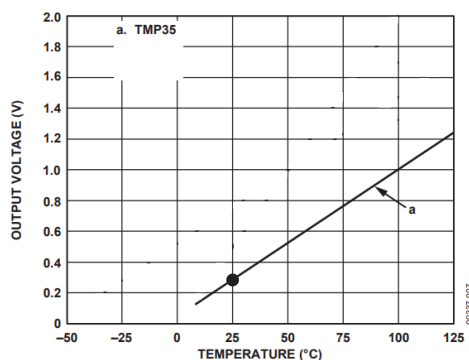


Figure 6. Output Voltage vs. Temperature

- A point: e.g. 250mV at 0°C
- A slope: e.g. 10mV/°C

Resolution

Suppose a binary number with N bits is to represent an analog value ranging from 0 to A

There are 2^N possible numbers

$$\text{Resolution} = A / (2^N - 1)$$

Resolution Example

Temperature range of 0 K to 300 K to be linearly converted to a voltage signal of 0 to 2.5 V, then digitized with an **8-bit** A/D converter

$$2.5 / (2^8 - 1) = 0.0098 \text{ V, or about } 10 \text{ mV per step}$$

$$300 \text{ K} / (2^8 - 1) = 1.18 \text{ K per step}$$

Resolution Example

Temperature range of 0 K to 300 K to be linearly converted to a voltage signal of 0 to 2.5 V, then digitized with a **10-bit** A/D converter

$$2.5 / (2^{10}-1) = 0.00244\text{V}, \text{ or about } 2.4 \text{ mV per step}$$

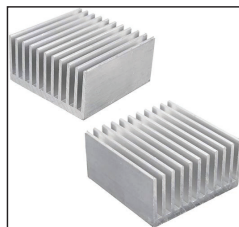
$$300 \text{ K} / (2^{10}-1) = 0.29 \text{ K per step}$$

Is the noise present in the system well below 2.4 mV ?

N bits vs. Resolution

AD converter
needed ?

Example 1:



Heatsink Range Temp: 0 – 60°C

Needed resolution: 1°



Bits of ADC: $\log_2 [(60/1)+1] = \text{Min. } 6 \text{ bits}$

Example 2:



Current sensor

Current Sensor for motor: 0 – 20A

Needed resolution: 1mA

Bits of ADC: $\log_2 [(20/0.001)+1] = \text{Min. } 15 \text{ bits} \rightarrow \text{Difficult}$

Resolution for 12 bits ADC standard?

$$2^{12}=4096 \rightarrow 20/4095 \approx 4.5 \text{ mA}$$

Example

The output voltage range for these devices is typically 100 mV at -40°C , 500 mV at 0°C , 750 mV at $+25^{\circ}\text{C}$, and +1.75 V at $+125^{\circ}\text{C}$. As shown in Figure 12.14, the TC1047A has a $10\text{ mV}/^{\circ}\text{C}$ voltage slope output response.

Measure air temperature (-20°C to 60°C with a 0.5 resolution). $V_{\text{ref}+}=5\text{ V}$ i $V_{\text{ref}-}=0\text{ V}$.

Define the required bits of the ADC.

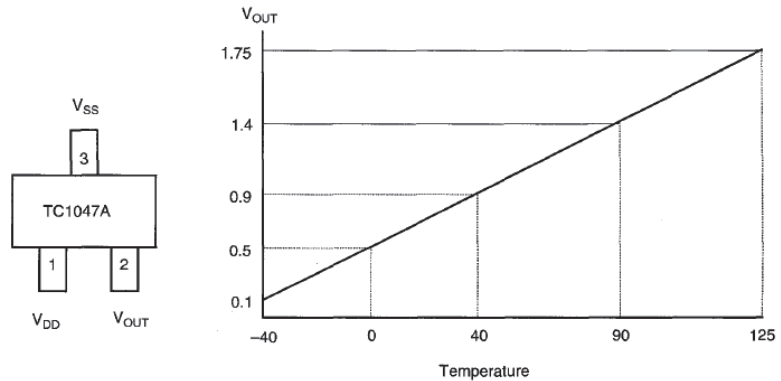
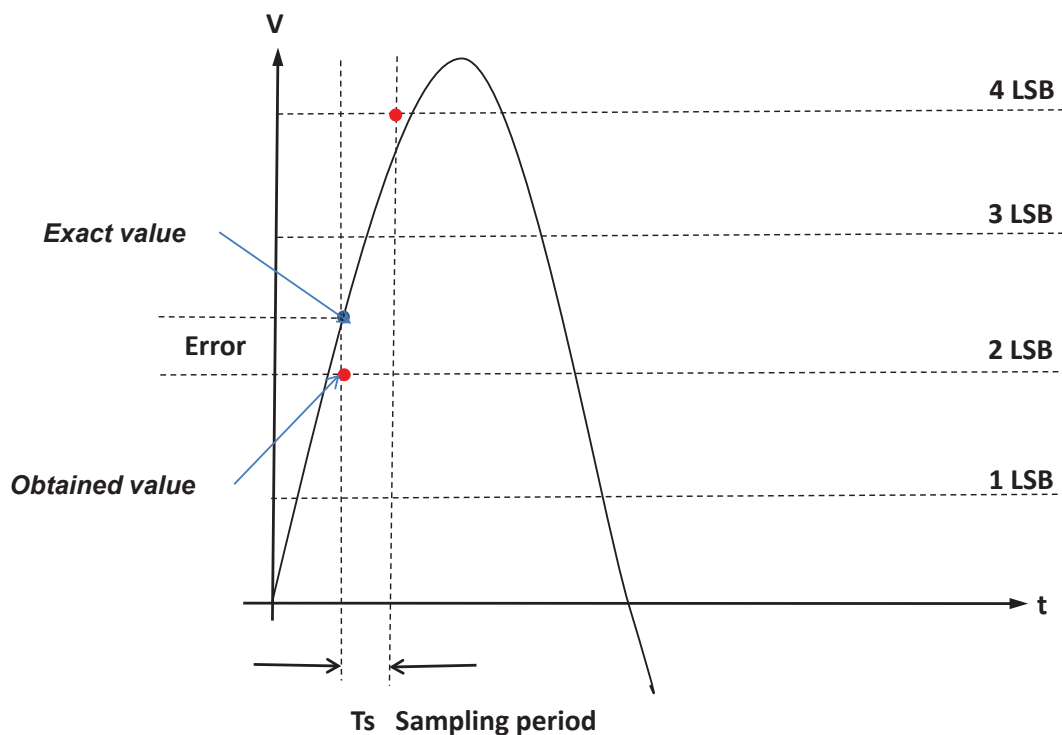
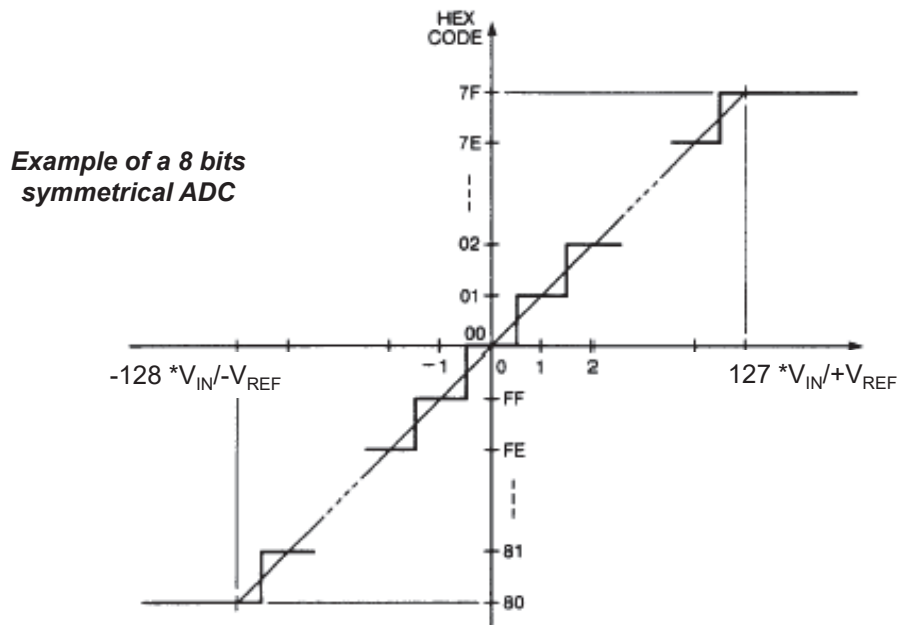


Figure 12.14 ■ TC1047A V_{OUT} vs. temperature characteristic

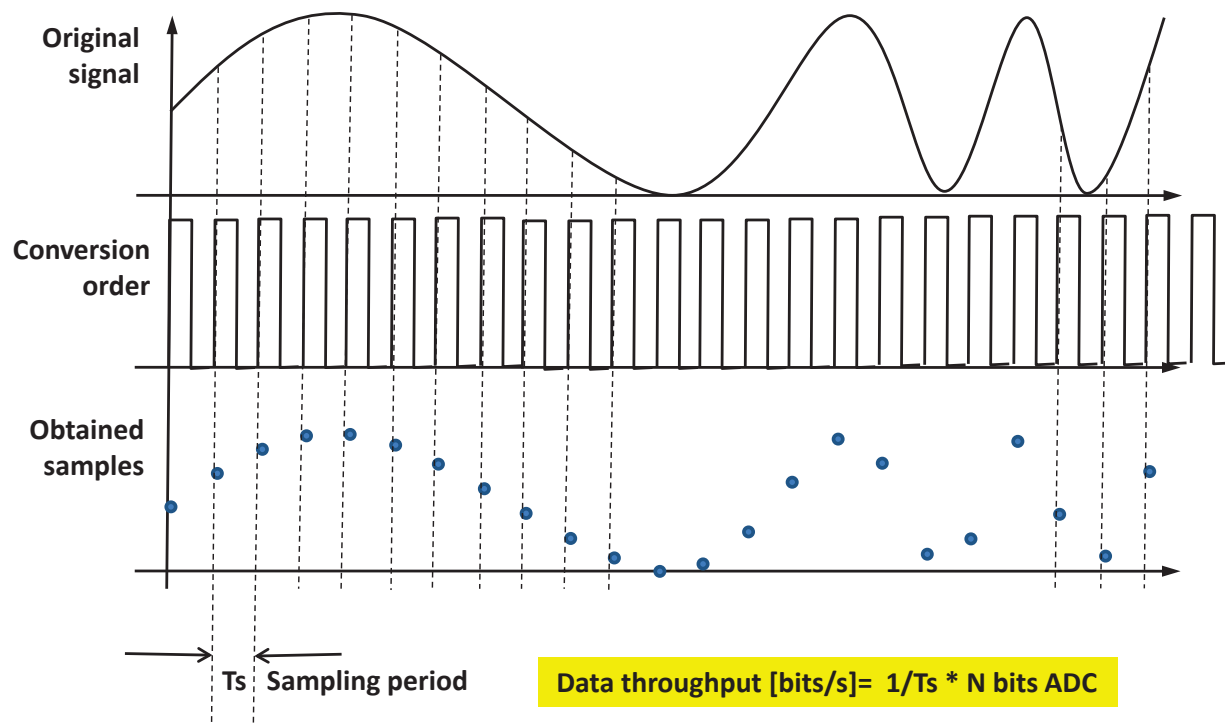
Quantization error: $\pm 0.5\text{ LSB}$



Symmetrical ADC output



Sampling (time)

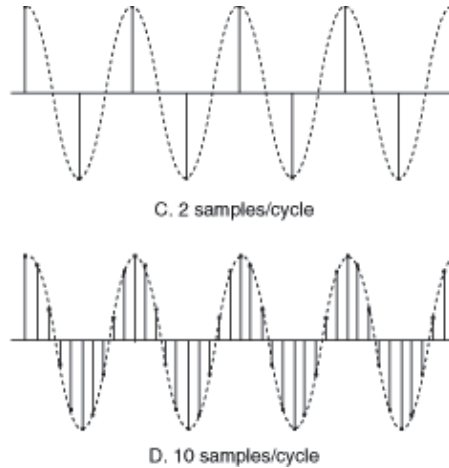


Nyquist criterion

To avoid aliasing

$$f_{\text{sampling}} > 2 \cdot f_{\text{signal max frequency}}$$

Nevertheless, higher sampling frequencies, higher quality



Data Collection – Sampling Rate

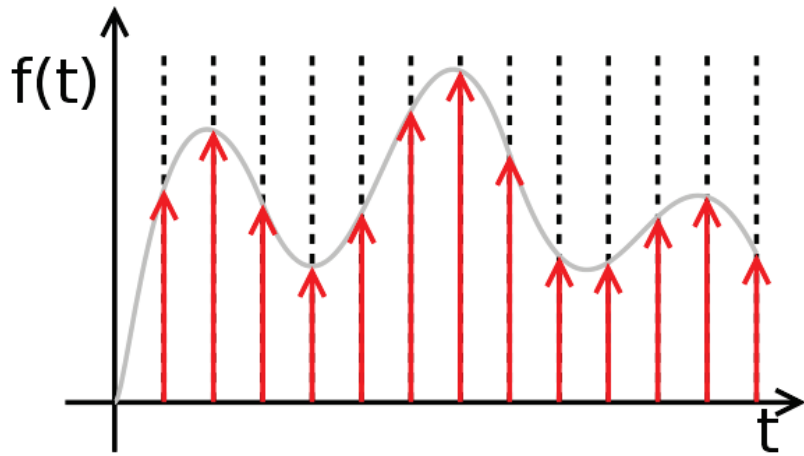
The Nyquist Rate

A signal must be sampled at a rate at least twice that of the highest frequency component that must be reproduced.

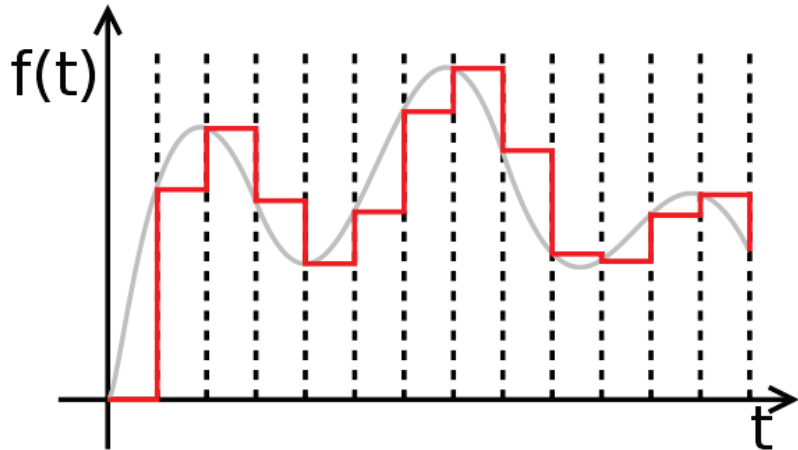
Example – Hi-Fi sound (20-20,000 Hz) is generally sampled at about 44 kHz.

External temperature during flight need only be sampled every few seconds at most.

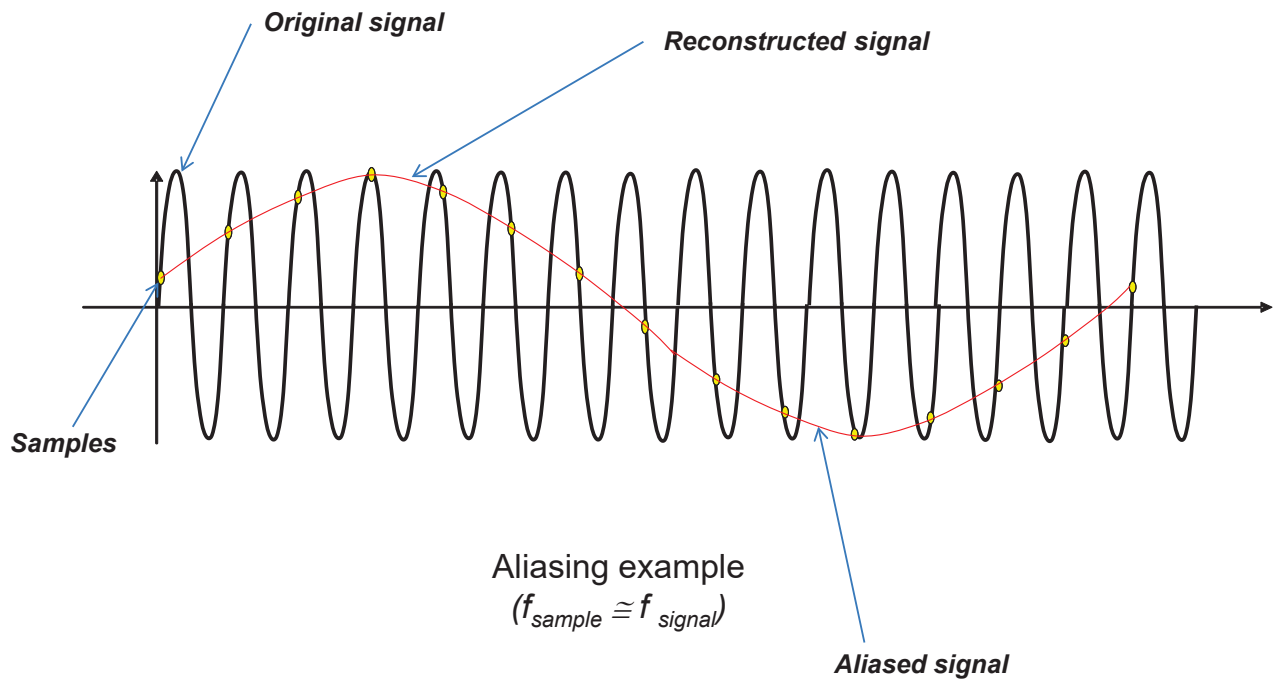
Original signal
& Sampling



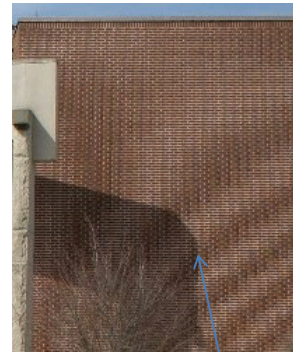
Original signal
vs Sampled version



Aliasing (1D)

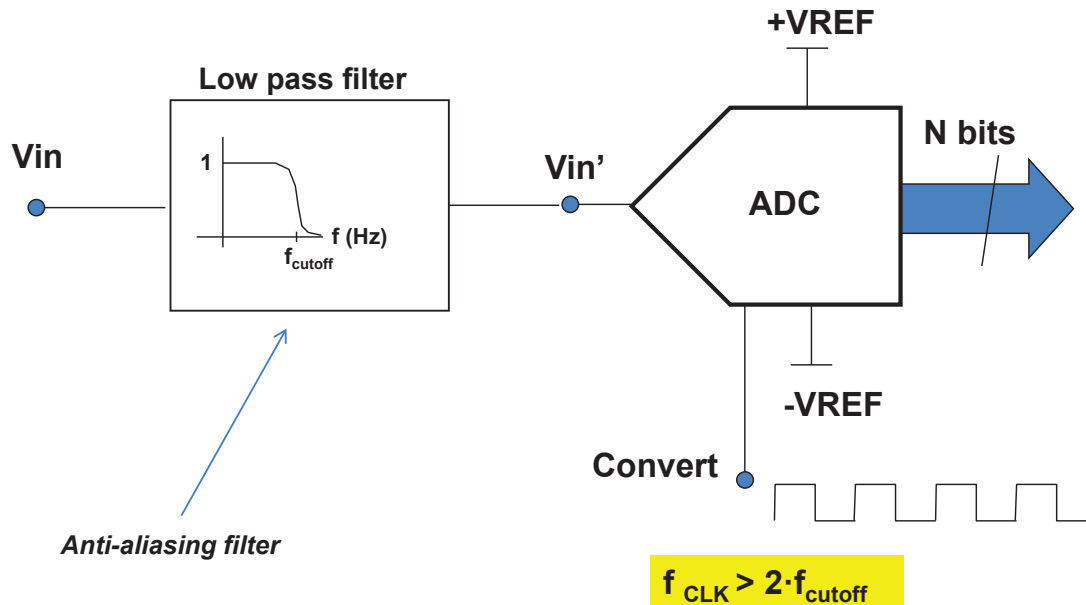


Aliasing (2D)



Aliased signal

Anti-aliasing filter

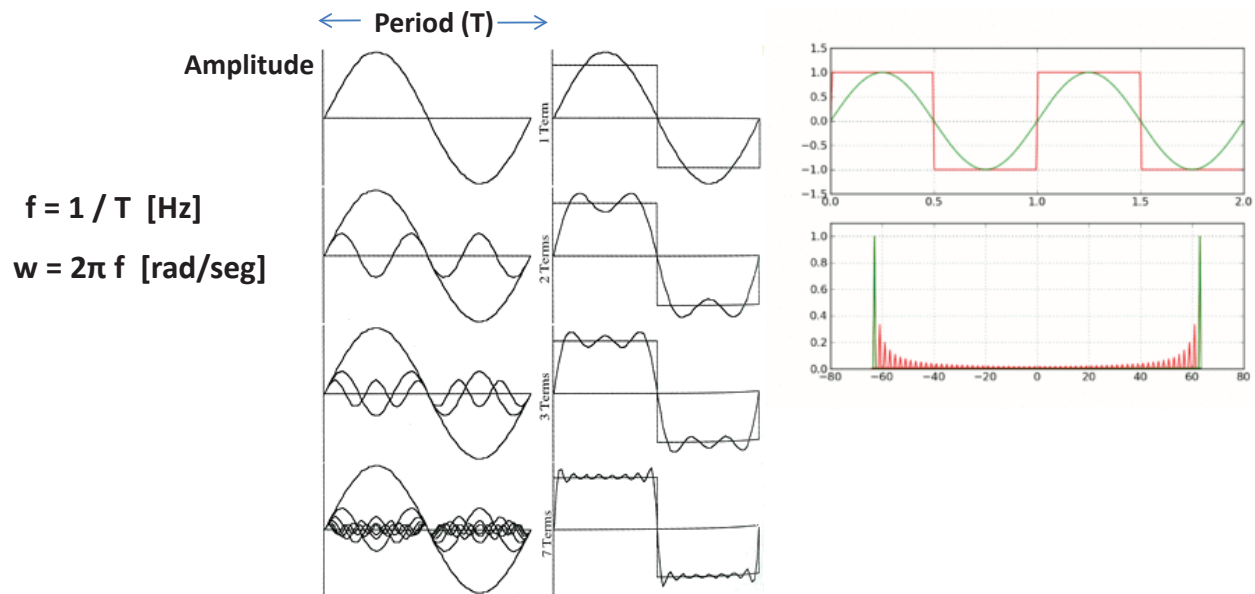


Signal characteristics: basic concepts

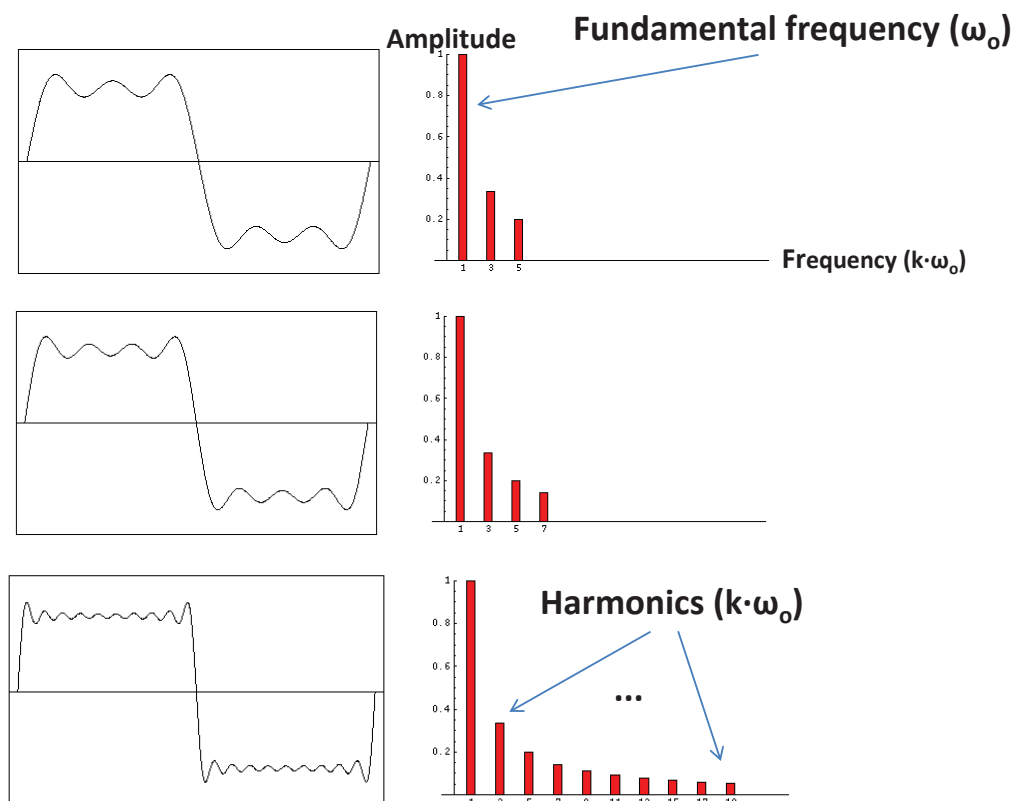
A periodic signal can be described as a sum of sinusoidal and cosinusoidal signals (Fourier series decomposition).

I.e. A square wave $x(t)$ is decomposed as:

$$x(t) = \frac{4}{\pi} (\sin(\omega_0 t) + \frac{1}{3} \sin(3\omega_0 t) + \frac{1}{5} \sin(5\omega_0 t) + \dots)$$

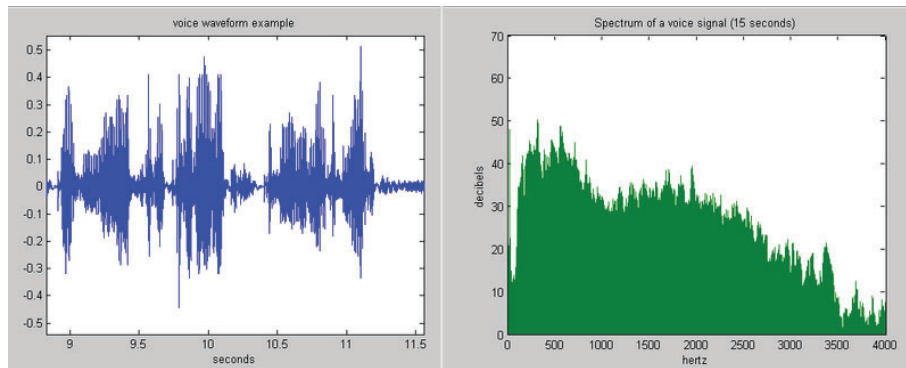
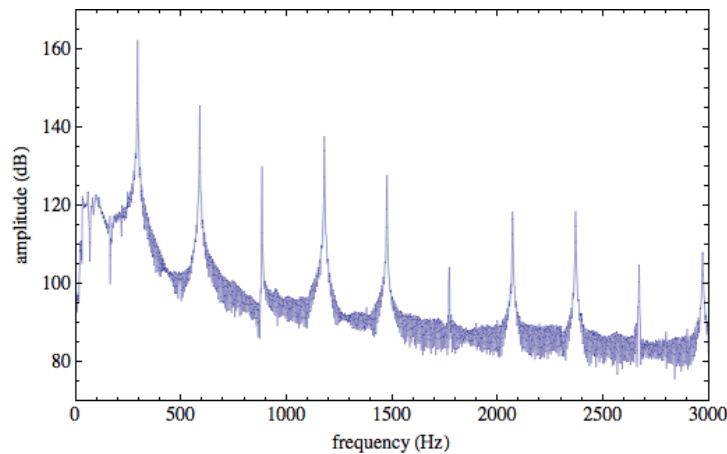


Fundamental frequency and harmonics



Signal's Frequency Spectrum

Piano spectrum
(note D4)



Voice signal and its associated spectrum

Time and frequency characteristics of audio signals

Audio facts

Range of audible frequencies: 20 Hz to 20KHz (individual depending)

Frequency range of an analog phone call: 350 Hz to 3500 Hz

Violin frequency range: 96 Hz to 10 kHz (approx.)

8 Hz Lowest organ note (*note = fundamental freq*)

32 Hz Lowest note on a standard 88-key piano

80 Hz Lowest note reproducible by the average female human voice

500 Hz Fundamental frequency of a crying baby

1050 Hz Highest note reproducible by the average female human voice

4186 Hz The highest note on a standard 88-key piano

16K Hz The highest harmonic of a female human voice

120 dB The loudest sound that can be tolerated (I.e. Chainsaw)

60 dB Level of a normal conversation

20 dB A whisper

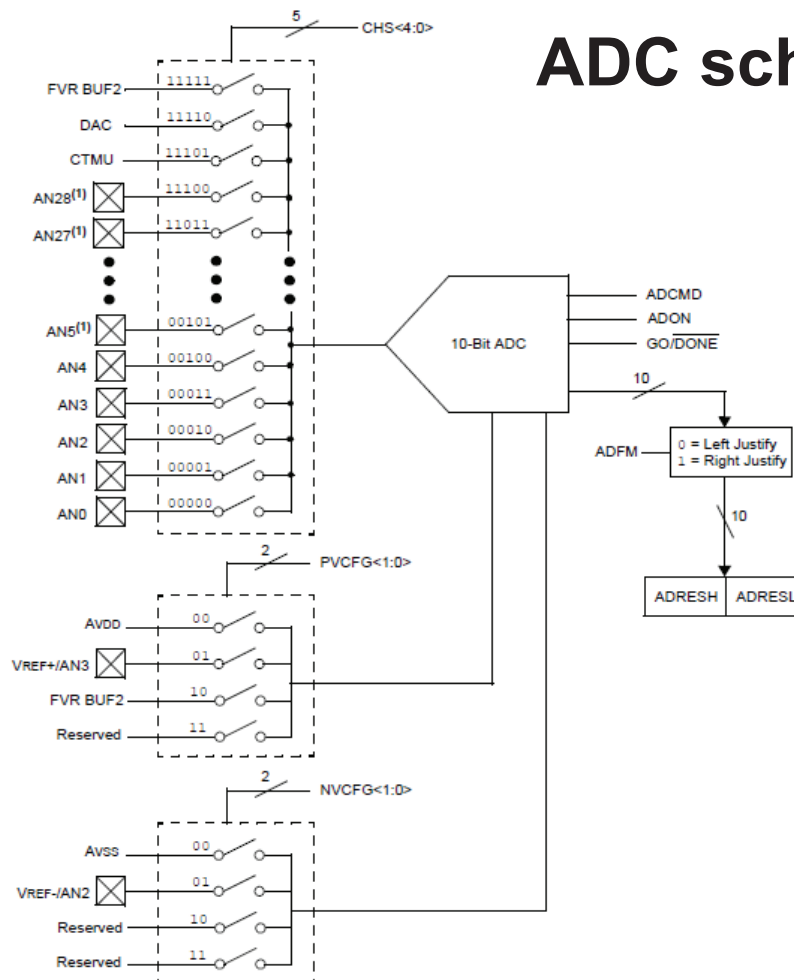
0 dB The faintest audible sound (at 1KHz)

$$\text{Decibel: } \text{dB} = 10 \log_{10} (P_s / P_e)$$

The PIC18 A/D Converter

- The PIC18 has a 10-bit A/D Successive Approximations converter.
- The number of analog inputs varies among different PIC18 devices.
- The A/D converter has the following registers:
 - A/D Result High Register (ADRESH)
 - A/D Result Low Register (ADRESL)
 - A/D Control Register 0 (ADCON0) (source selection)
 - A/D Control Register 1 (ADCON1) (reference selection)
 - A/D Control Register 2 (ADCON2) (timing selections)
- The contents of these registers vary with the PIC18 members.
- Other parameters must be considered:
ANSELX (pin configurations), ADIF, ADIE, ADIP (for AD interrupt)...

ADC schematic



REGISTER 17-1: ADCON0: A/D CONTROL REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CHS<4:0>					GO/DONE	ADON
bit 7							bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6-2 **CHS<4:0>:** Analog Channel Select bits
- 00000 = AN0
 - 00001 = AN1
 - 00010 = AN2
 - 00011 = AN3
 - 00100 = AN4
 - 00101 = AN5⁽¹⁾
 - 00110 = AN6⁽¹⁾
 - 00111 = AN7⁽¹⁾
 - 01000 = AN8
 - 01001 = AN9
 - 01010 = AN10
 - 01011 = AN11
 - 01100 = AN12
 - 01101 = AN13
 - 01110 = AN14
 - 01111 = AN15
 - 10000 = AN16
 - 10001 = AN17
 - 10010 = AN18
 - 10011 = AN19
 - 10100 = AN20⁽¹⁾
 - 10101 = AN21⁽¹⁾
 - 10110 = AN22⁽¹⁾
 - 10111 = AN23⁽¹⁾
 - 11000 = AN24⁽¹⁾
 - 11001 = AN25⁽¹⁾
 - 11010 = AN26⁽¹⁾
 - 11011 = AN27⁽¹⁾
 - 11100 = Reserved
 - 11101 = CTMU
 - 11110 = DAC
 - 11111 = FVR BUF2 (1.024V/2.048V/2.096V Volt Fixed Voltage Reference)⁽²⁾
- bit 1 **GO/DONE:** A/D Conversion Status bit
- 1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
 - This bit is automatically cleared by hardware when the A/D conversion has completed.
 - 0 = A/D conversion completed/not in progress
- bit 0 **ADON:** ADC Enable bit
- 1 = ADC is enabled
 - 0 = ADC is disabled and consumes no operating current

Note 1: Available on PIC18(L)F4XK22 devices only.
Note 2: Allow greater than 15 μ s acquisition time when measuring the Fixed Voltage Reference.

ADCON0 Register

ADCON1 Register

REGISTER 17-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIGSEL	—	—	—	PVCFG<1:0>		NVCFG<1:0>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **TRIGSEL:** Special Trigger Select bit
- 1 = Selects the special trigger from CTMU
 - 0 = Selects the special trigger from CCP5
- bit 6-4 **Unimplemented:** Read as '0'
- bit 3-2 **PVCFG<1:0>:** Positive Voltage Reference Configuration bits
- 00 = A/D VREF+ connected to internal signal, AVDD
 - 01 = A/D VREF+ connected to external pin, VREF+
 - 10 = A/D VREF+ connected to internal signal, FVR BUF2
 - 11 = Reserved (by default, A/D VREF+ connected to internal signal, AVDD)
- bit 1-0 **NVCFG<1:0>:** Negative Voltage Reference Configuration bits
- 00 = A/D VREF- connected to internal signal, AVSS
 - 01 = A/D VREF- connected to external pin, VREF-
 - 10 = Reserved (by default, A/D VREF- connected to internal signal, AVSS)
 - 11 = Reserved (by default, A/D VREF- connected to internal signal, AVSS)

ADCON2 Register

REGISTER 17-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT<2:0>			ADCS<2:0>	
bit 7						bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7 **ADFM:** A/D Conversion Result Format Select bit

1 = Right justified
 0 = Left justified

10 bit data result format!

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT<2:0>:** A/D Acquisition time select bits. Acquisition time is the duration that the A/D charge holding capacitor remains connected to A/D channel from the instant the GO/DONE bit is set until conversions begins.

000 = 0⁽¹⁾
 001 = 2 T_{AD}
 010 = 4 T_{AD}
 011 = 6 T_{AD}
 100 = 8 T_{AD}
 101 = 12 T_{AD}
 110 = 16 T_{AD}
 111 = 20 T_{AD}

Acquisition time for AD

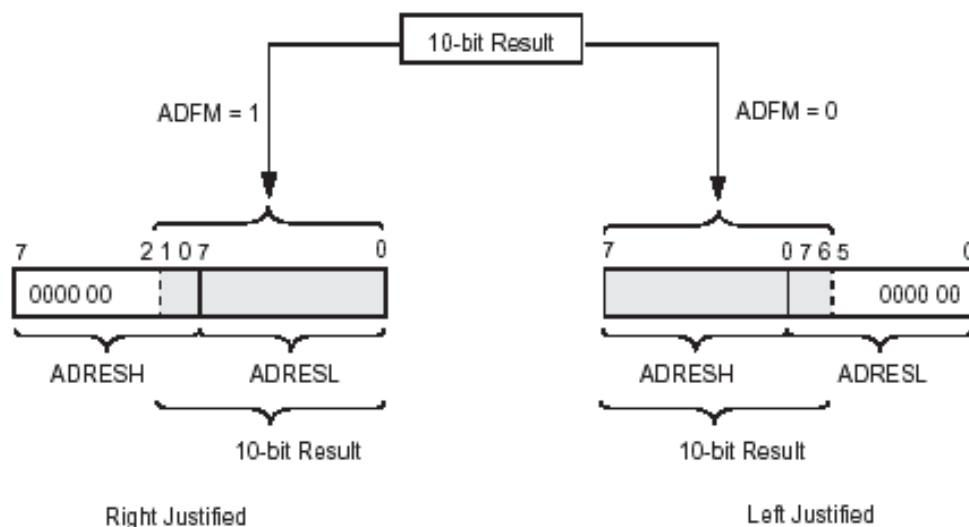
bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = Fosc/2
 001 = Fosc/8
 010 = Fosc/32
 011 = FRC⁽¹⁾ (clock derived from a dedicated internal oscillator = 600 kHz nominal)
 100 = Fosc/4
 101 = Fosc/16
 110 = Fosc/64
 111 = FRC⁽¹⁾ (clock derived from a dedicated internal oscillator = 600 kHz nominal)

Base clock for AD

Note 1: When the A/D clock source is selected as FRC then the start of conversion is delayed by one instruction cycle after the GO/DONE bit is set to allow the SLEEP instruction to be executed.

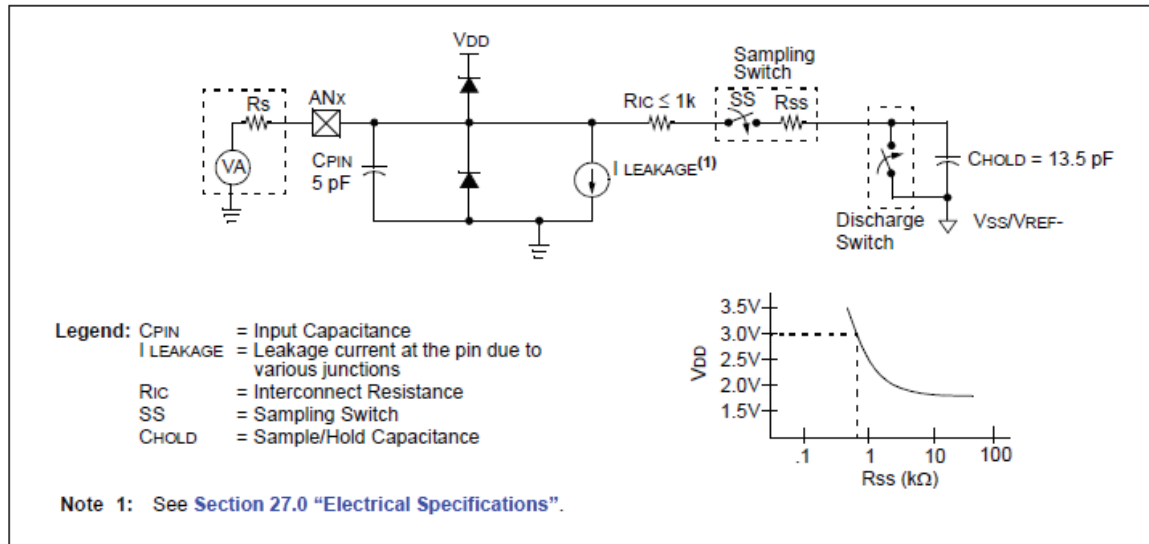
Result format



A/D Acquisition Time Requirements

- The A/D converter has a sample-and-hold circuit for analog input.
- The sample-and-hold circuit keeps the voltage stable when it is converted.
- The sample-and-hold circuit is shown in Figure 17-5.

FIGURE 17-5: ANALOG INPUT MODEL



- The capacitor C_{HOLD} holds the voltage to be converted. It must be charged to a stable value in order to get the maximum precision.
- The required minimum acquisition time T_{ACQ} is computed as follows:

EQUATION 17-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 3.0V VDD

$$\begin{aligned}
 T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\
 &= T_{AMP} + T_C + T_{COFF} \\
 &= 5\mu s + T_C + [(Temperature - 25^\circ C)(0.05\mu s/^\circ C)]
 \end{aligned}$$

The value for T_C can be approximated with the following equations:

$$V_{APPLIED} \left(1 - \frac{1}{2047} \right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within } 1/2 \text{ lsb}$$

$$V_{APPLIED} \left(1 - e^{-\frac{T_C}{RC}} \right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left(1 - e^{-\frac{T_C}{RC}} \right) = V_{APPLIED} \left(1 - \frac{1}{2047} \right) \quad ;\text{combining [1] and [2]}$$

Solving for T_C :

$$\begin{aligned}
 T_C &= -CHOLD(RIC + RSS + RS) \ln(1/2047) \\
 &= -13.5pF(1k\Omega + 700\Omega + 10k\Omega) \ln(0.0004885) \\
 &= 1.20\mu s
 \end{aligned}$$

Therefore:

$$\begin{aligned}
 T_{ACQ} &= 5\mu s + 1.20\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/^\circ C)] \\
 &= 7.45\mu s
 \end{aligned}$$

Other Time Requirements

TABLE 27-22: A/D CONVERSION REQUIREMENTS PIC18(L)F2X/4XK22

Standard Operating Conditions (unless otherwise stated) Operating temperature Tested at +25°C							
Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
130	TAD	A/D Clock Period	1	—	25	μs	-40°C to +85°C
			1	—	4	μs	+85°C to +125°C
131	Tcnv	Conversion Time (not including acquisition time) (Note 1)	11	—	11	TAD	
132	TACQ	Acquisition Time (Note 2)	1.4	—	—	μs	VDD = 3V, RS = 50Ω
135	Tswc	Switching Time from Convert → Sample	—	—	(Note 3)		
136	Tdis	Discharge Time	1	—	1	Tcy	

Note 1: ADRES register may be read on the following Tcy cycle.

Note 2: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (RS) on the input channels is 50 Ω.

Note 3: On the following cycle of the device clock.

$$T_{AD} \geq 1 \mu s$$

$$T_{ACQ} > 1.4 \mu s \text{ (but } T_{ACQ} > 7.45 \mu s \text{ in the example)}$$

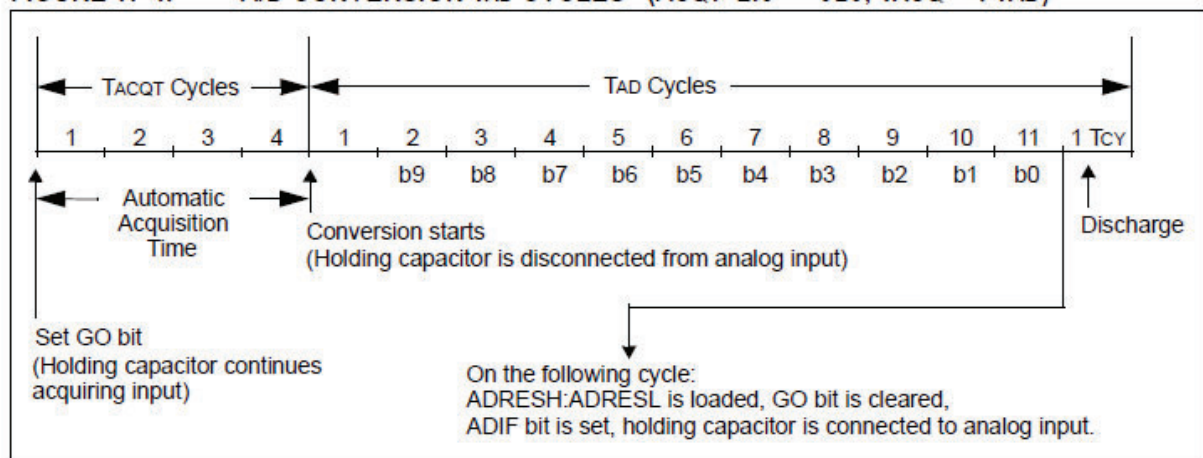
$$T_{CNV} = 11, \text{ we need } 11 T_{AD} \text{ for conversion.}$$

$$T_{DIS} = 1 \text{ Cycle}$$

AD Conversion

Timing example for $T_{ACQ} = 4 T_{AD}$

FIGURE 17-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



Automatic and manual modes

17.1.4 SELECTING AND CONFIGURING ACQUISITION TIME

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set.

Acquisition time is set with the ACQT<2:0> bits of the ADCON2 register. Acquisition delays cover a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there is no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. When an acquisition time is programmed, there is no indication of when the acquisition time ends and the conversion begins.

Procedure for Performing A/D Conversion

17.2.10 A/D CONVERSION PROCEDURE

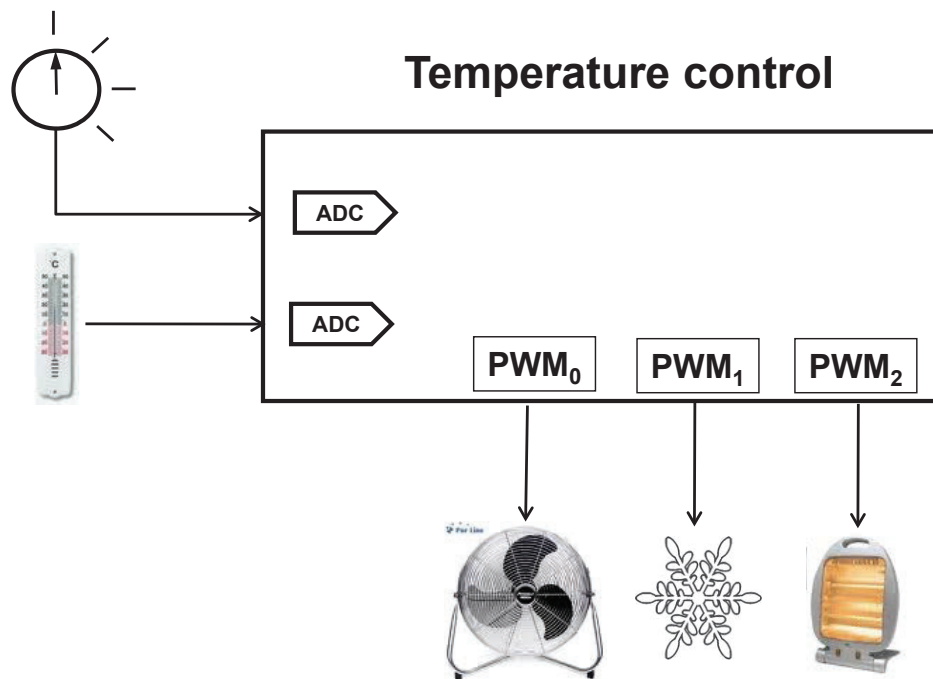
This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
 - Disable pin output driver (See TRIS register)
 - Configure pin as analog
2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Select result format
 - Select acquisition delay
 - Turn on ADC module
3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
4. Wait the required acquisition time⁽²⁾.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

EXAMPLE 17-1: A/D CONVERSION

```
;This code block configures the ADC
;for polling, Vdd and Vss as reference, Frc
clock and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
MOVLW    B'10101111' ;right justify, Frc,
MOVWF    ADCON2      ; & 12 TAD ACQ time
MOVLW    B'00000000' ;ADC ref = Vdd,Vss
MOVWF    ADCON1      ;
BSF      TRISA,0      ;Set RA0 to input
BSF      ANSEL,0      ;Set RA0 to analog
MOVLW    B'00000001' ;AN0, ADC on
MOVWF    ADCON0       ;
BSF      ADCON0,GO    ;Start conversion
ADCPoll:
BTFSCL   ADCON0,GO    ;Is conversion done?
BRA      ADCPoll      ;No, test again
; Result is complete - store 2 MSbits in
; RESULTHI and 8 LSbits in RESULTLO
MOVFF    ADRESH,RESULTHI
MOVFF    ADRESL,RESULTLO
```

Example Application



Example Barometric Measurement

The SenSym ASCX30AN Pressure Sensor

- The range of barometric pressure is between 28 to 32 **in-Hg** or 948 to 1083.8 **mbar**.
- The ASCX30AN output voltage would range from 2.06 V to 2.36 V.

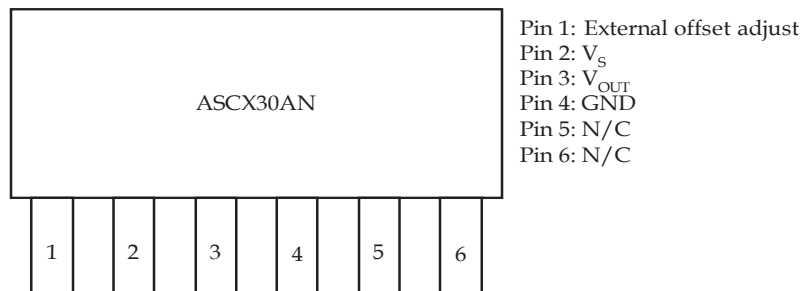
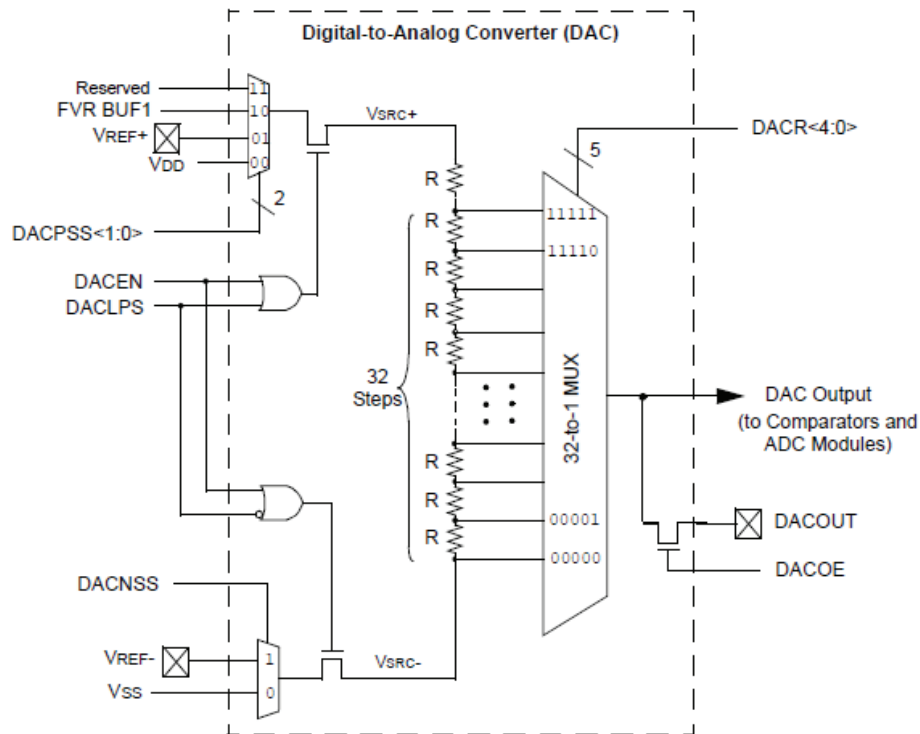


Figure 12.18 ASCX30AN pin assignment

The PIC18 D/A Converter

- The PIC1845K22 has a 5-bit D/A converter.



It is driven by registers VREFCON1

REGISTER 22-1: VREFCON1: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0
DACEN	DACLPS	DACOE	—	DACPSS<1:0>	—	DACNSS	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	DACEN: DAC Enable bit 1 = DAC is enabled 0 = DAC is disabled
bit 6	DACLPS: DAC Low-Power Voltage Source Select bit 1 = DAC Positive reference source selected 0 = DAC Negative reference source selected
bit 5	DACOE: DAC Voltage Output Enable bit 1 = DAC voltage level is also an output on the DACOUT pin 0 = DAC voltage level is disconnected from the DACOUT pin
bit 4	Unimplemented: Read as '0'
bit 3-2	DACPSS<1:0>: DAC Positive Source Select bits 00 = VDD 01 = VREF+ 10 = FVR BUF1 output 11 = Reserved, do not use
bit 1	Unimplemented: Read as '0'
bit 0	DACNSS: DAC Negative Source Select bits 1 = VREF- 0 = VSS

... and VREFCON2

REGISTER 22-2: VREFCON2: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DACR<4:0>				
bit 7			bit 0				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-5 **Unimplemented:** Read as '0'

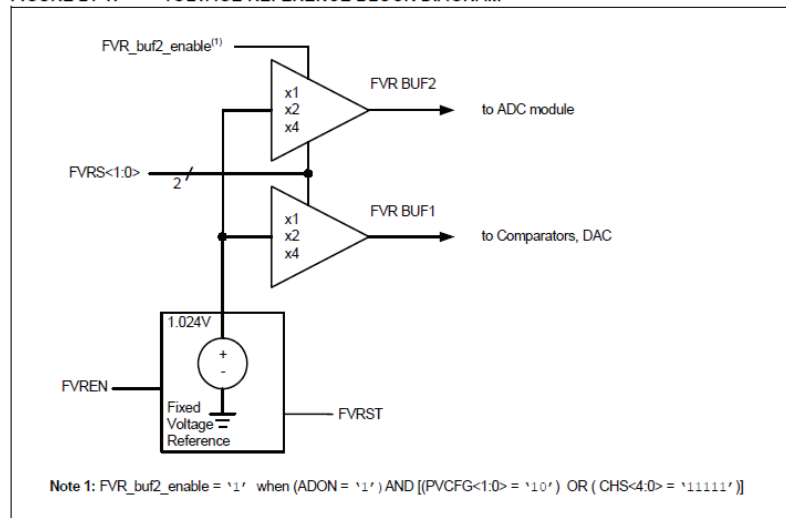
bit 4-0 **DACR<4:0>:** DAC Voltage Output Select bits

$$V_{OUT} = ((V_{SRC+}) - (V_{SRC-})) * (DACR<4:0> / (2^5)) + V_{SRC-}$$

The PIC18 Fixed Voltage Reference

- FVR1 and FVR2 are used in ADC and DAC modules
- These voltages are independent on supply voltage (VDD) and can be used as an absolute reference system.

FIGURE 21-1: VOLTAGE REFERENCE BLOCK DIAGRAM



Register VREFCON0 drives the FVR module

- FVRST bit is set when the circuitry reaches a stable output.

REGISTER 21-1: VREFCON0: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-1	U-0	U-0	U-0	U-0
FVREN	FVRST	FVRS<1:0>	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7 **FVREN:** Fixed Voltage Reference Enable bit
0 = Fixed Voltage Reference is disabled
1 = Fixed Voltage Reference is enabled
- bit 6 **FVRST:** Fixed Voltage Reference Ready Flag bit
0 = Fixed Voltage Reference output is not ready or not enabled
1 = Fixed Voltage Reference output is ready for use
- bit 5-4 **FVRS<1:0>:** Fixed Voltage Reference Selection bits
00 = Fixed Voltage Reference Peripheral output is off
01 = Fixed Voltage Reference Peripheral output is 1x (1.024V)
10 = Fixed Voltage Reference Peripheral output is 2x (2.048V)⁽¹⁾
11 = Fixed Voltage Reference Peripheral output is 4x (4.096V)⁽¹⁾
- bit 3-2 **Reserved:** Read as '0'. Maintain these bits clear.
- bit 1-0 **Unimplemented:** Read as '0'.

Note 1: Fixed Voltage Reference output cannot exceed V_{DD}.