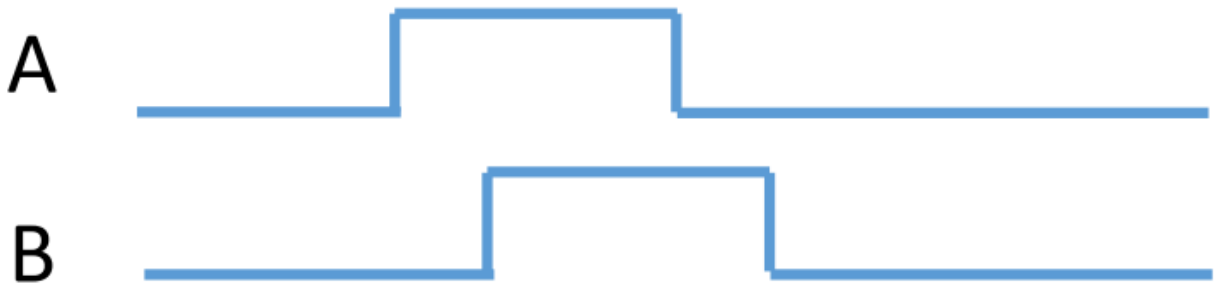
Project 2 (Due date: September 14, 2020)

The basic goal of this lab is to design logic to design a state machine for a parking lot car counter. The lot has a gate through which only one car at a time may enter or leave. There are two detectors, A and B, mounted on the gate. Each detector produces a '1' output when a car passes by the detector. The detectors are arranged such that a car entering the lot must first pass by detector A and then B. In other words, when a car enters the lot, the front of the car triggers A and then triggers B as shown in the timing diagram below. When the car has advanced sufficiently, detector A will turn off, followed by B. The process is reversed when a car leaves the lot. Note that a car may partially enter or leave the lot and then reverse meaning that you may get A on and A off without B ever going on – or A on then B on, and then B going off before A going off. The sensors are close enough such that it is impossible for a car to be between the two sensors.



Submit a report including group member names, the state machine design, VHDL code, and simulation screenshot. One submission per group.

(You are encouraged to test your code using the switches/pushbuttons/leds on DE0-Nano/DE2 boards and demo your project during the office hour)