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Single-source SYCL C++ on Xilinx FPGA

Xilinx Research Labs

Khronos booth @SC17 2017/11/12—19

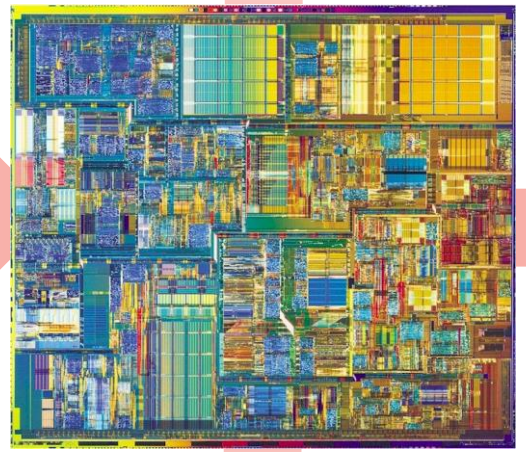
Khronos standards for heterogeneous systems

Connecting Software to Silicon

COLLADA

3D for the Web
- Real-time apps and games in-browser
- Efficiently delivering runtime 3D assets

WebGL glTF



NNEF OpenVX

Vision and Neural Networks
- Tracking and odometry
- Scene analysis/understanding
- Neural Network inferencing

Parallel Computation
- Machine Learning acceleration
- Embedded vision processing
- High Performance Computing (HPC)

OpenCL SPIR SYCL

OpenGL SC OpenVG OpenGL ES Vulkan OpenGL OpenXR

Real-time 2D/3D
- Virtual and Augmented Reality
- Cross-platform gaming and UI
- CG Visual Effects
- CAD and Product Design
- Safety-critical displays

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PROMOTER MEMBERS

KHRONOS GROUP

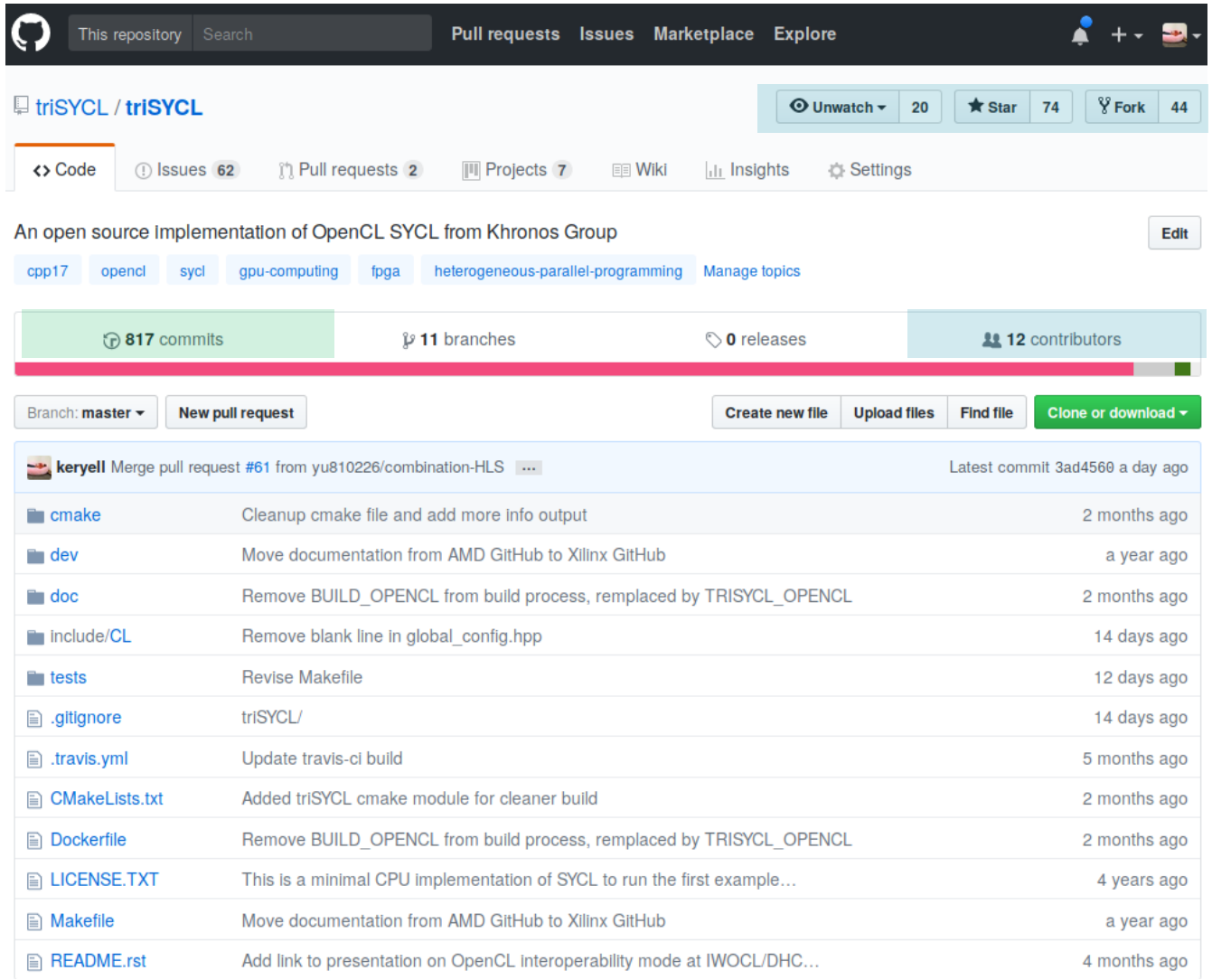
Over 100 members worldwide
Any company is welcome to join

Complete example of matrix addition in OpenCL SYCL

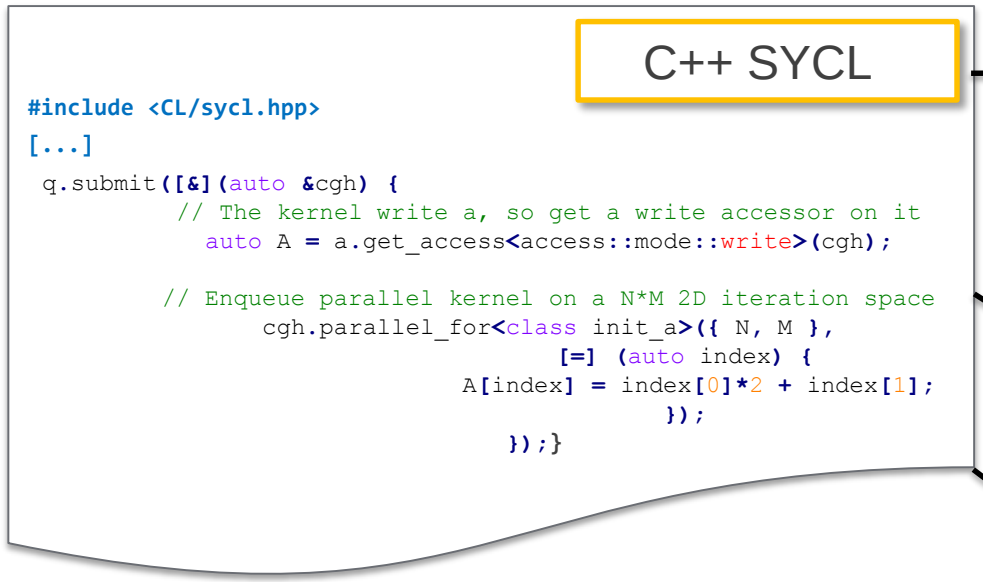
```
#include <CL/sycl.hpp>
#include <iostream>
using namespace cl::sycl;
constexpr size_t N = 2;
constexpr size_t M = 3;
using Matrix = float[N][M];

// Compute sum of matrices a and b into c
int main() {
 Matrix a = { { 1, 2, 3 }, { 4, 5, 6 } };
 Matrix b = { { 2, 3, 4 }, { 5, 6, 7 } };

 Matrix c;

 {// Create a queue to work on default device
  queue q;
  // Wrap some buffers around our data
  buffer A { &a[0][0], range { N, M } };
  buffer B { &b[0][0], range { N, M } };
  buffer C { &c[0][0], range { N, M } };
  // Enqueue some computation kernel task
  q.submit([&](handler& cgh) {
   // Define the data used/produced
   auto ka = A.get_access<access::mode::read>(cgh);
   auto kb = B.get_access<access::mode::read>(cgh);
   auto kc = C.get_access<access::mode::write>(cgh);
   // Create & call kernel named "mat_add"
   cgh.parallel_for<class mat_add>(range { N, M },
      [=](id<2> i) { kc[i] = ka[i] + kb[i]; }
   );
  }); // End of our commands for this queue
 } // End scope, so wait for the buffers to be released
 // Copy back the buffer data with RAII behaviour.
 std::cout << "c[0][2] = " << c[0][2] << std::endl;
 return 0;
}
```

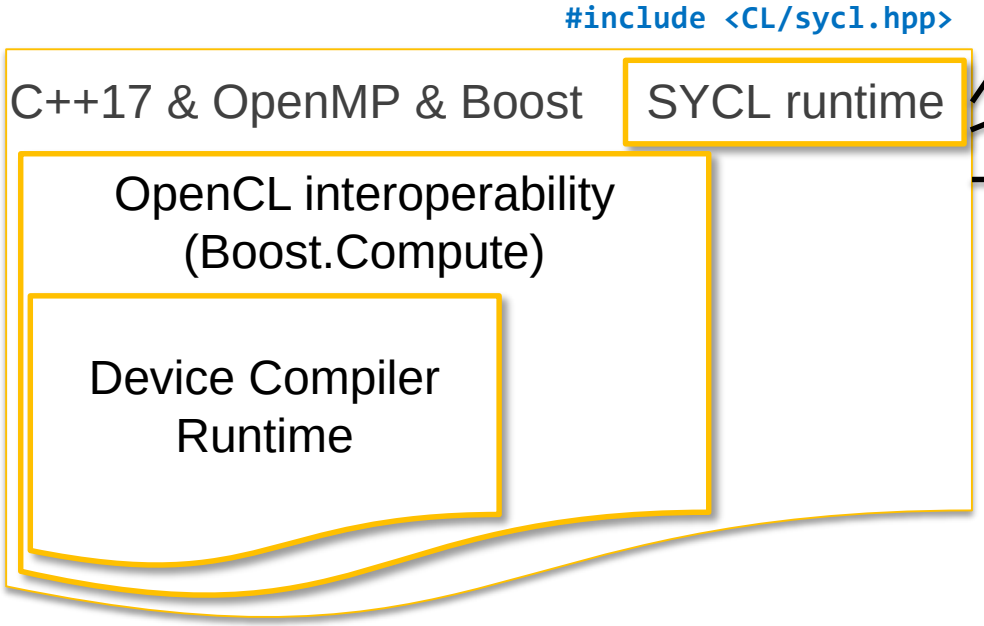
triSYCL

- Open Source SYCL 1.2/2.2
- Uses C++17 templated classes
- Used by Khronos to define the SYCL and OpenCL C++ standard
  - Languages are now too complex to be defined without implementing...
- On-going implementation started at AMD and now led by Xilinx
- https://github.com/triSYCL/triSYCL
- OpenMP for host parallelism
- Boost.Compute for OpenCL interaction
- Prototype of device compiler for Xilinx FPGA



https://github.com/triSYCL/triSYCL architecture





Unmodified host compiler
(gcc/clang/vs/icc)

OpenMP
CPU
executable

For OpenCL interoperability

libOpenCL.so

Clang/LLVM
Host & kernel caller

OpenMP
CPU
executable

Clang/LLVM
device compiler

kernels.bin

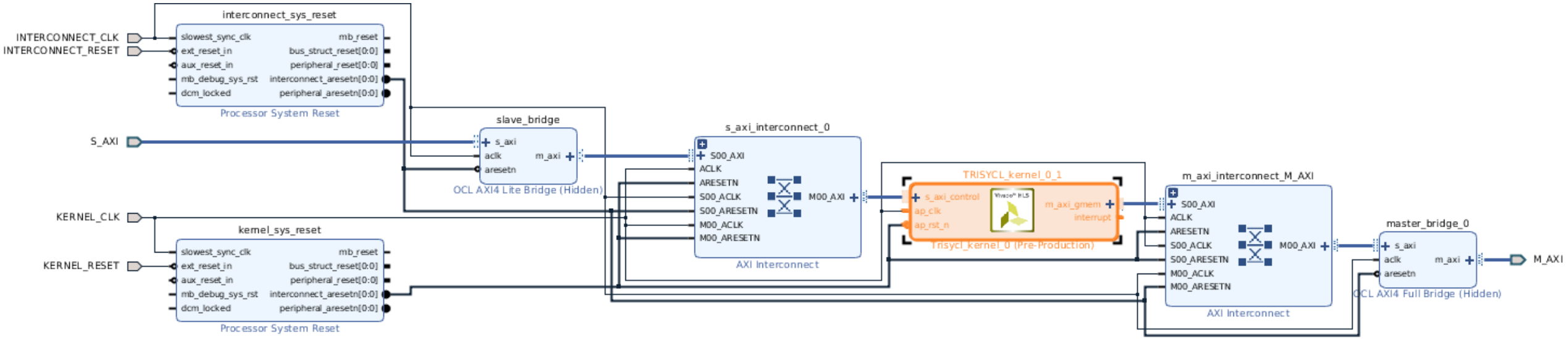
SPIR 2.0
“de facto”

Vendor OpenCL
device compiler

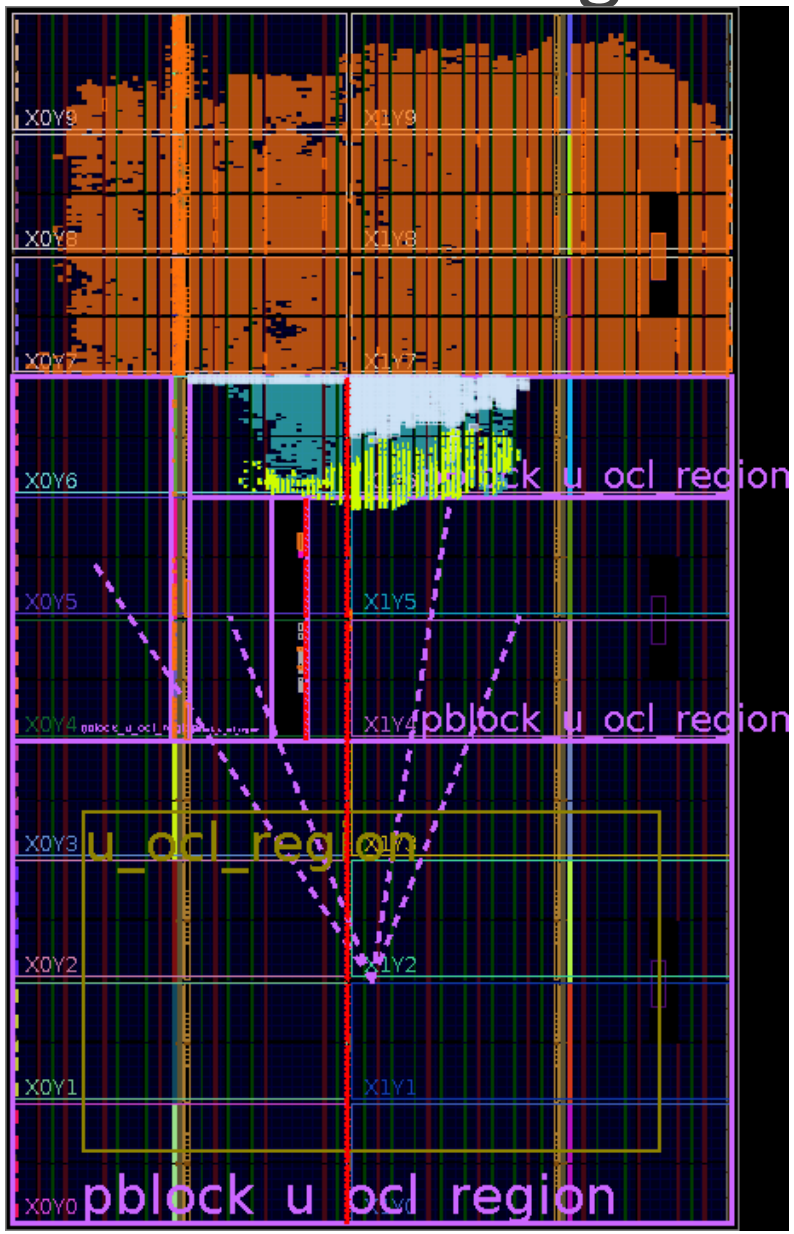
SPIR 2.0 “de facto” output with Clang 3.9.1

```
using; ModuleID = 'device_compiler/single_task_vector_add_drt.kernel.bc'

source_filename = "device_compiler/single_task_vector_add_drt.cpp"

target datalayout = "e-m:e-i64:64-f80:128-n8:16:32:64-S128"

target triple = "spir64"


declare i32 @__gxx_personality_v0(...)


; Function Attrs: noinline norecurse nounwind uwtable

define spir_kernel void @TRISYCL_kernel_0(i32 addrspace(1)* %f.0.0.0.val, i32 addrspace(1)*
%f.0.1.0.val, i32 addrspace(1)* %f.0.2.0.val) unnamed_addr #0 !kernel_arg_addr_space !3
!kernel_arg_type !4 !kernel_arg_base_type !4 !kernel_arg_type_qual !5 !kernel_arg_access_qual !6 {

entry:

  br label %for.body.i


for.body.i:                                       ; preds = %for.body.i, %entry

  %indvars.iv.i = phi i64 [ 0, %entry ], [ %indvars.iv.next.i, %for.body.i ]

  %arrayidx.i.i = getelementptr inbounds i32, i32 addrspace(1)* %f.0.1.0.val, i64 %indvars.iv.i

  %0 = load i32, i32 addrspace(1)* %arrayidx.i.i, align 4, !tbaa !7

  %arrayidx.i15.i = getelementptr inbounds i32, i32 addrspace(1)* %f.0.2.0.val, i64 %indvars.iv.i

  %1 = load i32, i32 addrspace(1)* %arrayidx.i15.i, align 4, !tbaa !7

  %add.i = add nsw i32 %1, %0

  %arrayidx.i13.i = getelementptr inbounds i32, i32 addrspace(1)* %f.0.0.0.val, i64 %indvars.iv.i

  store i32 %add.i, i32 addrspace(1)* %arrayidx.i13.i, align 4, !tbaa !7

  %indvars.iv.next.i = add nuw nsw i64 %indvars.iv.i, 1

  %exitcond.i = icmp eq i64 %indvars.iv.next.i, 300

  br i1 %exitcond.i, label %"_ZZZ9test_mainiPPcENK3$_1clERN2cl4sycl7handlerEENKUlvE_clEv.exit",
label %for.body.i

"_ZZZ9test_mainiPPcENK3$_1clERN2cl4sycl7handlerEENKUlvE_clEv.exit": ; preds = %for.body.i

  ret void

}


attributes #0 = { noinline norecurse nounwind uwtable "disable-tail-calls"="false" "less-precise-
fpmad"="false" "no-frame-pointer-elim"="false" "no-infs-fp-math"="false" "no-jump-tables"="false"
"no-nans-fp-math"="false" "no-signed-zeros-fp-math"="false" "stack-protector-buffer-size"="8"
"target-cpu"="x86-64" "target-features"="+fxsr,+mmx,+sse,+sse2,+x87" "unsafe-fp-math"="false"
"use-soft-float"="false" }


!llvm.ident = !{!0}

!opencl.spir.version = !{!1}

!opencl.ocl.version = !{!2}


!0 = !{!"clang version 3.9.1 "}

!1 = !{i32 2, i32 0}

!2 = !{i32 1, i32 2}

!3 = !{i32 1, i32 1, i32 1}

!4 = !{!"int *", !"int *", !"int *"}

!5 = !{!"", !"", !""}

!6 = !{!"read_write", !"read_write", !"read_write"}

!7 = !{!8, !8, i64 0}

!8 = !{!"int", !9, i64 0}

!9 = !{!"omnipotent char", !10, i64 0}

!10 = !{!"Simple C++ TBAA"}
```

After Xilinx SDx 2017.2 xocc ingestion…



After Xilinx SDx 2017.2 xocc ingestion… FPGA layout!



Code execution on real FPGA

```
rkeryell@xirjoant40:~/Xilinx/Projects/OpenCL/SYCL/triSYCL/branch/device/tests (device)$
device_compiler/single_task_vector_add_drt.kernel_caller
binary_size = 5978794
task::add_prelude
task::add_prelude
task::add_prelude
accessor(Accessor &a) : &a = 0x7ffd39395f40
 &buffer =0x7ffd39395f50
accessor(Accessor &a) : &a = 0x7ffd39395f30
 &buffer =0x7ffd39395f60
accessor(Accessor &a) : &a = 0x7ffd39395f20
 &buffer =0x7ffd39395f70
single_task &f = 0x7ffd39395f50
task::prelude
schedule_kernel &k = 0x1516060
Setting up
_ZN2cl4sycl6detail18instantiate_kernelIZZ9test_mainiPPcENK3$_1clERNS0_7handlerEE3addZZ9test_mainiS4_ENKS5_clES7_EUlvE_EEvT0_
 aka TRISYCL_kernel_0
Name device xilinx_adm-pcie-7v3_1ddr_3_0
serialize_accessor_arg index =0, size = 4, arg = 0
serialize_accessor_arg index =1, size = 4, arg = 0x1
serialize_accessor_arg index =2, size = 4, arg = 0x2

**** no errors detected
```