HW 4: Global Placement

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Homework Concepts

使用 C++完成可使提供之 legalizer 順利運作成功的 global placer。

Compile & Execute

How to compile:

Go to src/ directory and type "make " command

[vlsipda14@ic29 src] make

How to execute:

Go to src/ directory and type the following command

[vlsipda14@ic29 src]./place –aux <inputFile.aux>

Option :

-h: show the usage of executable binary

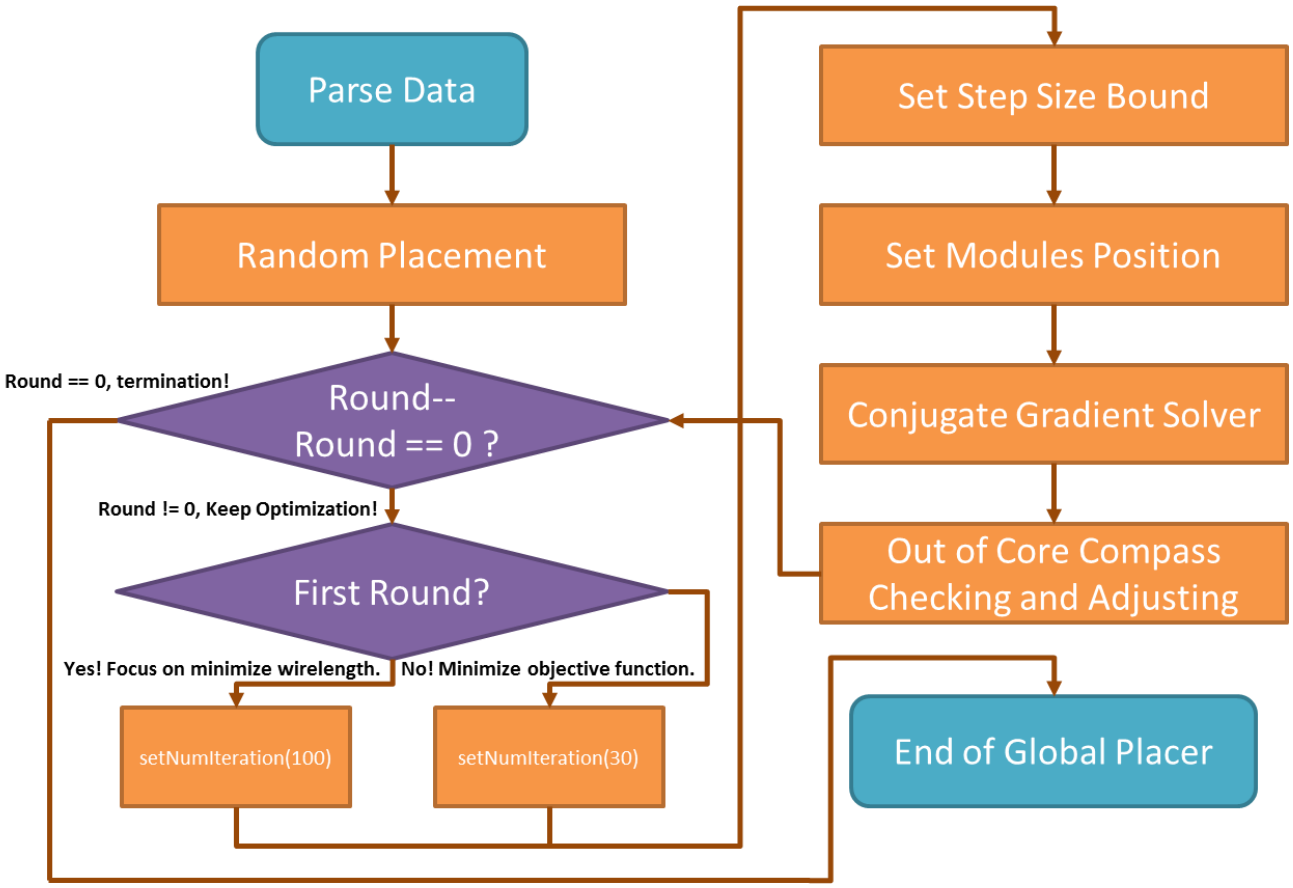
```
[vlsipda14@ic30 placement]$ ./place -h
Usage: ./place -aux benchmark.aux
```

Time Measurement

時間量測為程式本身 built-in，程式使用<time.h> library 的 time<NULL>來取得時間，精度以秒為單位。

Case	ibm01		ibm05	
Sol.	TWL	CPU	TWL	CPU
Global HPWL	60823799	183.0 sec	12976627	468.0 sec
Legal HPWL	102416926	0.0 sec	14066975	1.0 sec
Detail HPWL	75447703	3.0 sec	12610042	5.0 sec
HPWL	75447703	186.0 sec	12610042	474.0 sec
TWL: total wirelength CPU: runtime in seconds				

Algorithm Flow (Global Placer)



Pseudocode (Global Placer)

Input: a set of modules, a set of nets, and a set of pins for each module,

Output: a set of position of modules which can legalize succcessfully

begin

Parse book-shelf format

Use random place as initial placement result (place inside the floor plan region is the unique constraint)

while(round--) { // the numerical optimizer iteration is user-specified

    set parameters for gradient solver in each round

    check and adjust modules position prevent out of core compass

    set the new modules position

}

Result Comparison (compare with Top 3 result from last year)

Case	ibm01		ibm05	
Sol.	TWL	CPU	TWL	CPU
1st	66871608	85.0 sec	10985372	426.0 sec
2nd	70747994	69.0 sec	11687597	161.0 sec
3rd	68633081	111.0 sec	14948987	156.0 sec
Me	75447703	186.0 sec	12610042	474.0 sec
TWL: total wirelength CPU: runtime in seconds				

這次無論在執行時間還是品質上與去年結果相比皆相形失色，但比起使用 simulated annealing 的方法相信應該已經會有比較好的 wire length 了，去年的參數使用上非常完美令我望塵莫及。

Homework Review

雖說這次助教說是最簡單的一次 program assignment，但我覺得整體寫來簡單歸簡單，程式碼也沒有之前多行，但牽扯到的相關公式與概念都是好幾篇 paper 累積起來的結果，即使最後了解 model 該怎麼做並且實做出來，但其更深層的概念意義尚還需要吸收消化，對於自己這次的作業產生的無力感非常多，自己幾乎是躺著被 carry，令我自嘆不如，期許自己能再多努力一點吧。