HW 1: APR Tool Practice

105062600 Yi-Cheng, Chao 10:30, March 8, 2017

Homework Concepts

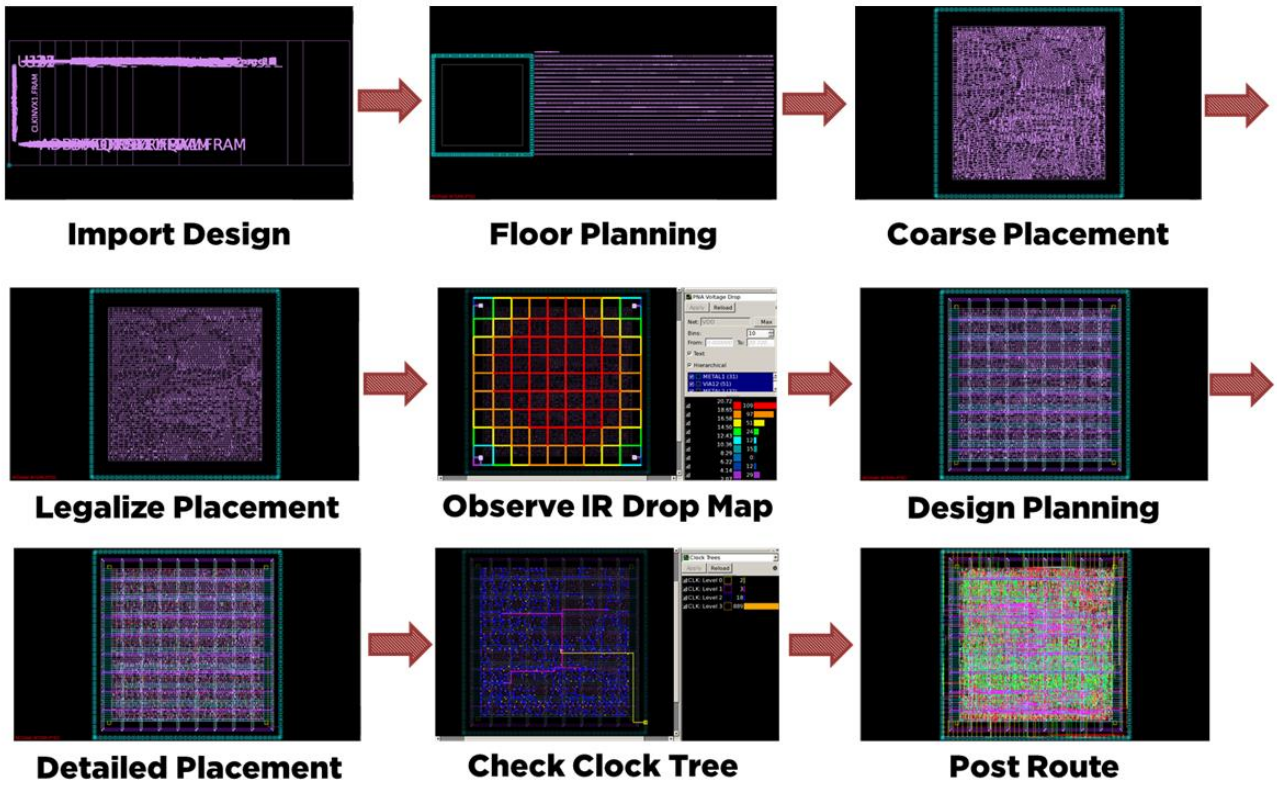
使用 Synopsys APR tool “IC compiler” 完成 Post-Route，藉以熟悉 APR 流程並觀察各個階段參數所影響的結果差異。

Prepared Data

APR 需使用已合成完的 Gate level code，以下為本次要進行 APR 的 design data。
Gate level netlist: aes_core_syv.v
Timing constraint file: aes_core_SYN.sdc

APR Flow

[vlsipda14@ic29] source /tools/linux/synopsys/CIC/icc.cshrc
在開始使用 ICC 進行 APR 前呼叫使用已設定好之 ICC 作業環境變數，之後便可依照 Tutorial 步驟完成 Layout，每個主要步驟後的完成圖如下圖所示：



Experiment Result

以下參數對於可調動的 effort 參數皆使用 hign 選項，其餘參數分別在表格上方顯示。

Parameter Set A

{Clock Period, Core Utilization, Core Area} = {30, 0.7, 101015}

	(congestion-driven, timing-driven)			
	(off, off)	(on, off)	(off, on)	(on, on)
slack	19.01	18.51	18.81	18.92
total cell area	68569.866285	68529.128683	68615.696086	68534.220887
total wire length	238475 micron	237807 micron	239524 micron	238691 micron
utilization ratio	0.6781	0.6778	0.6785	0.6778
via count	49140	48193	49663	49271

Parameter Set B

{Clock Period, Core Utilization, Core Area} = {10, 0.95, 74610}

	(congestion-driven, timing-driven)			
	(off, off)	(on, off)	(off, on)	(on, on)
slack	0.04	0.02	0.02	0.01
total cell area	68474.811883	68518.944283	68474.811880	68500.272890
total wire length	219076 micron	218645 micron	218074 micron	218775 micron
utilization ratio	0.9175	0.9181	0.9175	0.9179
via count	51529	51411	51582	51801

For set A:
Slack: (on, off) < (off, on) < (on, on) < (off, off)
Total cell area: (on, off) < (on, on) < (off, off) < (off, on)
Total wire length: (on, off) < (off, off) < (on, on) < (off, on)
Via count: (on, off) < (off, off) < (on, on) < (off, on)

For set B:
Slack: (on, on) < (off, on) = (on, off) < (off, off)
Total cell area: (off, on) = (off, off) < (on, on) < (on, off)
Total wire length: (off, on) < (on, off) < (on, on) < (off, off)
Via count: (on, off) < (off, off) < (on, on) < (off, on)

Experiment Analysis & Question/Answer

Q1: The different between timing- and congestion driven placement.

Timing-driven placement: The placement of standard cells will be done in such a way that the cells belonging to a critical path will be placed close together.

Congestion-driven placement: The placement is driven to facilitate the routing. Hence, the separation between standard cells will be increased to take into account the routing.

Timing-driven placement 也就是會盡可能的讓有溝通的 cells 擺的靠近一點，因此很顯然的可以知道有可能會有 congestion ratio 上升的 overhead; 另一方面，congestion 則是盡可能的分散叫壅擠的部分，使 routing 能更順利進行，然而因此也會有 timing 上升的 overhead，因此可以在上述結果中看到，兩者在不同的規格下都有各自的優劣，並沒辦法說誰好，甚至兩者皆勾選 on 去做 placement 因為在抉擇 timing 與 congestion，因此都呈現較中庸的結果，兩者優劣取決於今天使用者的面向，大部分的情況下，timing-driven 將會是比較好的選擇，然而 timing-driven 卻有可能造成過度的壅擠，而使 routing failed，是特別需要注意的地方。

Reference:

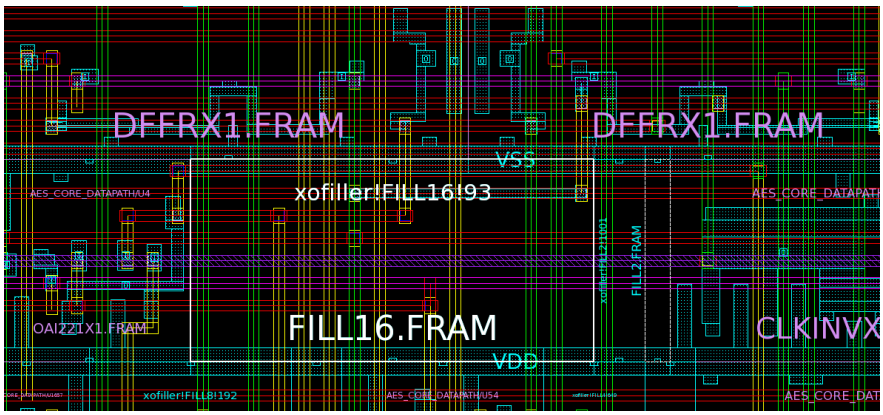
Timing driven and congestion driven- http://www.edaboard.com/thread108810.html

What is timing driven- http://www.edaboard.com/thread278474.html

Q2: Why do we insert filler cells?

For better yield, density of the chip needs to be uniform. In standard cells APR flow, the cells in the design are placed on the row. To make sure that each cells gets power and ground connection, the cells are abutted together so that the VDD and VSS terminal of neighboring cells short together. This makes it possible to tap power only at one point anywhere in the row. But it is virtually impossible to fill 100% of the die area with regular cells. So we use filler cells to fill these spaces between regular library cells to route power rails. Filler cells are used for connecting the gaps between the cells after placement.

下圖便可以看到 Filler Cell (白色方框部分)來連接 VSS 和 VDD 的空白 Gap!



Reference:

Use filler cells for N-well continuity-

https://www.quora.com/Why-do-we-use-filler-cells-for-N-well-continuity

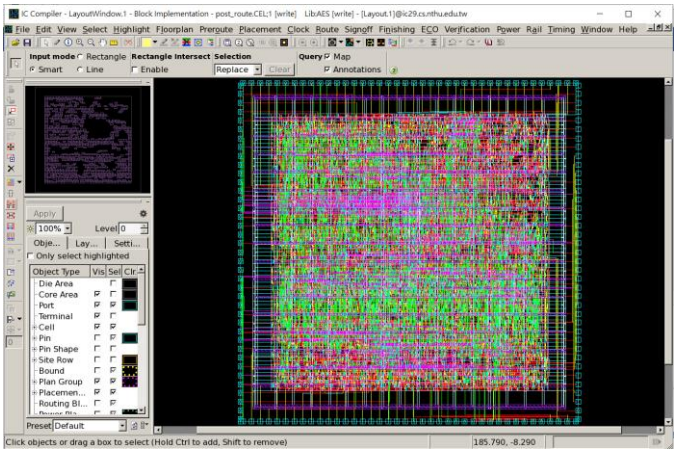
Best Layout

Use cost function: F(x) = #via count + wire length + core area (for all slack is positive)

Choose the minimum cost in set B→{Congestion-driven, Timing-driven} = {off, on}

Corresponding Data

Core utilization = 0.95
Clock period = 10ns
Slack = 0.02 ns
Core area = 74610 site
Total cell area = 68474.8 site
Total wire length = 218074 micron
Via count = 51582



Difficulty Encounter

上學期已經學習如何使用 Cadence 的 APR Tool Encounter，因此大部分 ICC 上的操作都能對應到 Encounter 上，網路上也可以很容易地找到不少資訊，遇到的困難幾乎沒有，唯有繁瑣的調整參數，但都是體力活，只要花時間就可以完成，希望之後 Homework 也能這麼簡單就好了。

Homework Review

兩個 Tool 的差別在使用上我比較喜歡 IC Compiler 的檔案管理方式，在版本管理上可以做非常多的索引以及版本控制，在 APR 的過程中也可以調整非常多的參數，網路上的評價是，ICC 在 placement 的質量遠在 Encounter 上，Encounter 則在規模大的 chip 上做 Floorplan 比較方便，兩者互有優劣，總之又學到了一個 Tool 的使用，只是對於一些細節參數調整仍沒有辦法完全的理解功用，大概是之前沒去 CIC 上課的業障吧 XD