

DSD #
納入仕様書番号 : 1012090323

Data Sheet #
データシート番号 : bq8050 1/4/2010

Please refer to the Data sheets on below Definition.
データシートについては、下記対象項目をご参照ください。

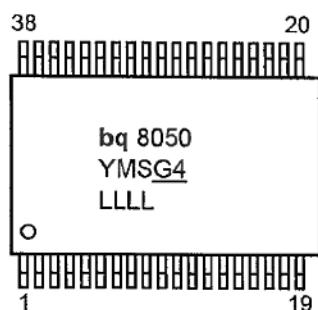
Effective Device
該当製品名 : BQ8050DBTR

Effective Package
該当パッケージ : DBT Package (Please refer to MECHANICAL DATA.)
パッケージ(外形寸法図をご参照ください。)

Effective Grade
該当グレード : -

Symbolization Specification 捺印仕様

(TOP VIEW)



bq : BQ LOGO (LOWER CASE)
8050 : DEVICE CODE
Y : YEAR CODE (1, 2, 3, 4, 5, 6, 7, 8, 9, 0)
M : MONTH CODE (1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C)
S : ASSEMBLY SITE CODE
G4 : TI-GREEN MARKING STANDARD
LLLL : LOT TRACE CODE

CoolRISC™ Programmable Battery Manager

FEATURES

- Fully Integrated 2, 3 and 4 Series Li-Ion or Li-Polymer Cell Battery Pack Manager
- Low-Power 8-Bit RISC CPU Core Operating at Up to 4-MHz
- Fully Integrated Internal Clock Synthesizer Generating Frequencies up to 4 MHz with no external components required
- Flexible Memory Architecture with Integrated Flash Memory
 - 24k x 22 Program Flash EPROM
 - 6k x 22 Program Mask ROM
 - 2k x 8 Data Flash EPROM
 - 1.25k x 8 Data RAM
- Supports Two-Wire SMBus v1.1 Interface with accelerated 400kHz programming option
- N-CH High Side Protection FET Drive
- SHA-1 Authentication Responder
 - Runs the SHA-1 Block Cipher with Secure Memory Locations
 - 2 x 64 bit keys are used for Maximum Key Security
- Reduced Power Modes (Typical Battery Pack Operating Range Conditions)
 - Low Power: < 500 µA
 - Sleep: < 50 µA
- High-Accuracy Analog Front End With Two Independent ADCs
 - High-Resolution Integrator for Coulomb Counting
 - 15-Bit Delta-Sigma ADC With a 16-Channel Multiplexer for Voltage, Current, and Temperature

FEATURES (CONT)

- Programmable Current Protection
 - Over Current in Discharge
 - Short Circuit in Charge
 - 2 Levels of Short Circuit in Discharge
 - Load Removal Detection Support
- Integrated Pre-Charge function utilizing an external current limit resistor
- General Purpose Open Drain Pre Charge Output
- Package: 38-Pin TSSOP

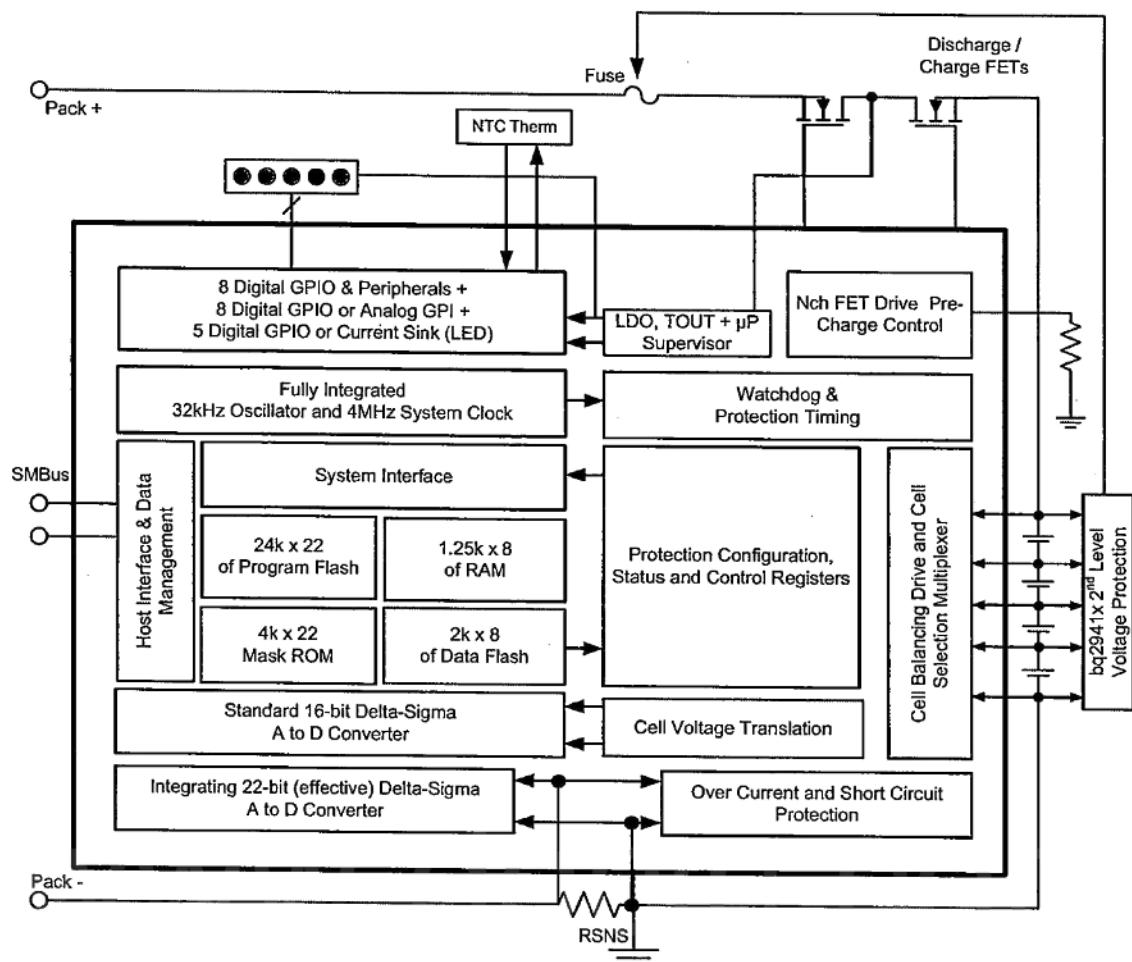
DESCRIPTION

The Texas Instruments bq8050 Battery Manager is a fully integrated pack-based solution that provides a flash programmable reduced instruction-set (RISC) CPU, protection and authentication for 2, 3 or 4 series cell Li-Ion battery packs in a single TSSOP package.

The bq8050 communicates via an SMBus 1.1 compatible interface and combines a low-power high-speed RISC processor, high-accuracy analog measurement capabilities, integrated flash memory, an array of peripheral and communication ports, N-CH FET drive, and SHA-1 Authentication transform responder.

The bq8050 also provides hardware based over current in discharge, short circuit in charge and discharge protection and can also provide over voltage, under voltage and over temperature protection through firmware interaction.

1 TYPICAL IMPLEMENTATION



2 PIN DETAILS

2.1 External

PIN NAME	#	I/O	DESCRIPTION
RC3/AD3	10	I/O,IA	Port C.3 digital push-pull I/O pin or selectable as an input, AD3, to the over-sampled ADC
RC4/AD4	12	I/O,IA	Port C.4 digital push-pull I/O pin or selectable as an input, AD4, to the over-sampled ADC
RC5/AD5	14	I/O,IA	Port C.5 digital push-pull I/O pin or selectable as an input, AD5, to the over-sampled ADC
RC6/AD6	15	I/O,IA	Port C.6 digital push-pull I/O pin or selectable as an input, AD6, to the over-sampled ADC
RC7/AD7	16	I/O,IA	Port C.7 digital push-pull I/O pin or selectable as an input, AD7, to the over-sampled ADC
RA3/EV	21	I/OD	Port A.3 digital open-drain I/O pin or selectable as a configurable external event input to wake the controller from a halt state
RA4/SMBD	17	I/OD	Port A.4 digital open-drain I/O pin or SMBus data pin
RA5/INT1	18	I/OD	Port A.5 digital open-drain I/O pin OR edge triggered interrupt
RA6/SMBC	19	I/OD	Port A.6 digital open-drain I/O pin or SMBus clock pin
RA7/INT2/VOUT	20	I/OD	Port A.7 digital open-drain I/O pin with pull-up capable of driving power for an external device OR edge triggered Interrupt
RB0/CS0	26	I/OD	Port B.0 digital open-drain I/O pin OR Programmable Current Sink
RB1/CS1	25	I/OD	Port B.1 digital open-drain I/O pin OR Programmable Current Sink
RB2/CS2	24	I/OD	Port B.2 digital open-drain I/O pin OR Programmable Current Sink
RB3/CS3	23	I/OD	Port B.3 digital open-drain I/O pin OR Programmable Current Sink
RB4/CS4	22	I/OD	Port B.4 digital open-drain I/O pin OR Programmable Current Sink
PTC	32	IA	Safety Thermistor input for use with PTC Thermistor
FUSE	33	O	Push-Pull Fuse Drive
SRP	11	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRP is the top of the sense resistor. SRP can also be selected as an input to the over-sampled ADC.
SRN	13	IA	Analog input pin connected to the internal coulomb-counter peripheral for integrating a small voltage between SRP and SRN where SRN is the bottom of the sense resistor. SRN can also be selected as an input to the over-sampled ADC.
RBI	27	P	RAM backup pin to provide backup potential to the internal DATA RAM if VCC is momentarily shorted, by using a capacitor attached between RBI and VSS.
VC4	7	IA	Sense voltage input terminal for least positive cell, balance current input for least positive cell, and return balance current for third most positive cell
VC3	6	IA	Sense voltage input terminal for third most positive cell, balance current input for third most positive cell, and return balance current for second most positive cell.
VC2	5	IA	Sense voltage input terminal for second most positive cell, balance current input for second most positive cell, and return balance current for most positive cell.
VC1	4	IA	Sense voltage input terminal for most positive cell, balance current input for most positive cell, and battery stack measurement input
BAT	3	P	Alternative power source
CHG	1	O	N-CH FET Drive
DSG	38	O	N-CH FET Drive
PACK	37	P	PACK positive terminal and alternative power source
GPOD	36	OD	N-CH FET open-drain output
PCHGIN	34	I	Pre-charge circuit input
PCR	2	O	Pre-charge load resistor connection
VCC	35	P	Power supply voltage
REG33	31	P	Internal power supply bias and 3.3V supply output
REG25	28	P	Internal power supply 2.5V bias output

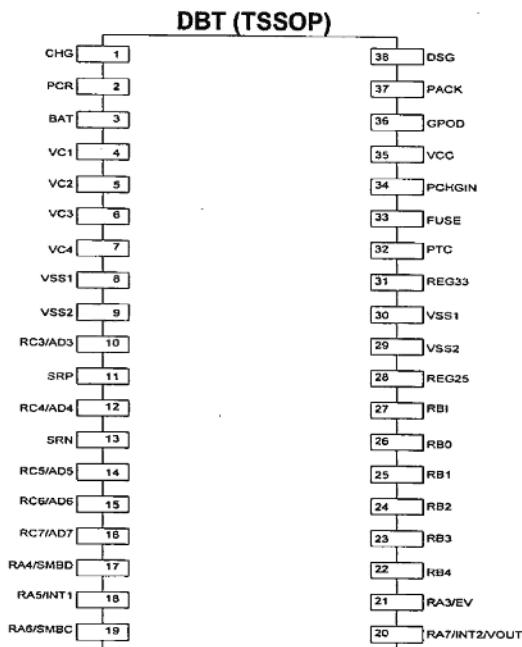
PIN NAME	#	I/O	DESCRIPTION
VSS1	8,30	P	Device ground ⁽¹⁾
VSS2	9,29	P	Device ground ⁽¹⁾

(1) For maximum thermal efficiency VSS1 and VSS2 should be connected to separate ground planes and connected together at the sense resistor node.

2.2 Internal

PIN NAME	I/O	DESCRIPTION
RC0/AD0 [CELL+]	IA	Port C.0 AD0 input to the over-sampled ADC and CELL+ translation output of translation amplifier
RC1/AD1 [CELL-]	IA	Port C.1 AD1 input to the over-sampled ADC and CELL- translation output of translation amplifier
RC2/CLKOUT [WDI]	O	Port C.2 digital push-pull output pin that drives a 32-kHz square-wave to the AFE
RA0 [XALERT]	I	Port A.0 digital push-pull input to the AGG
RA1 [SCLK]	O	Port A.1 digital push-pull output pin driving the inter-device communication clock to the AFE.
RA2 [SDATA]	I/O	Port A.2digital open-drain I/O pin used for inter-device communication data to and from the AFE. AGG and AFE are both enabled with 20kΩ pull-ups
XRST [XRST]	I	Master reset pin with integrated pull up used to force the device into reset when held low. Must be held high for normal operation. The XRST output is open drain.

2.3 Pin Out Diagrams





bq8050

2.4 Package Power Dissipation Ratings

Care should be taken to ensure that the power dissipation of the configured solution does not exceed the maximum power dissipation ratings shown below.

Theta JA	Derating factor (mW/°C)	Power Rating (W)		
		T _A <25°C	T _A =70°C	T _A =85°C
78	12.82	1.282 W	0.705	0.512

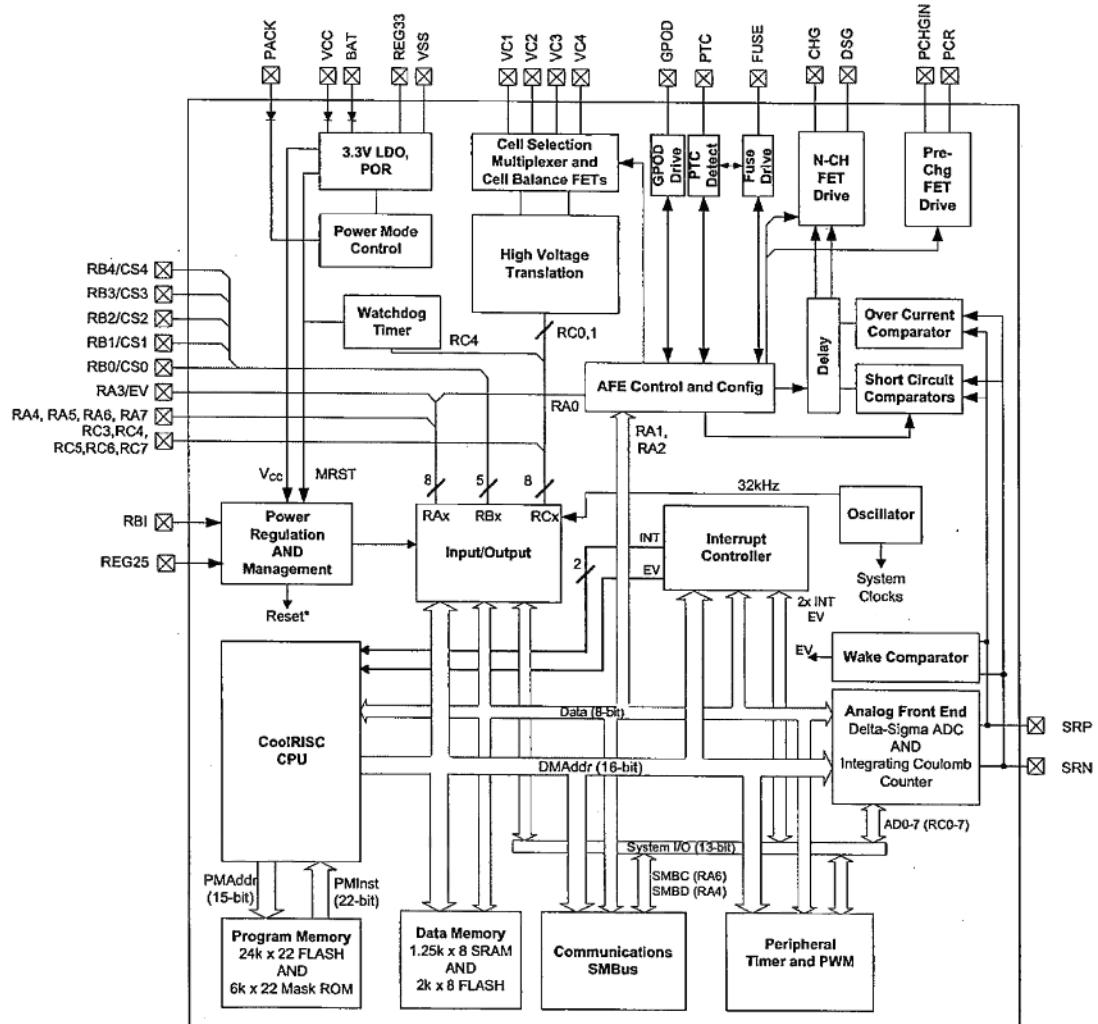
Careful consideration of the power dissipation should be made when developing firmware for the bq8050. Higher power features such as Flash updates, LEDs, Internal Pre-charge and cell balancing should be carefully used when the bq8050 is in higher Ambient temperatures. For example, reducing the LED power to 3mA rather than the full 5mA at higher temperatures should be considered. Also, simultaneous flash updates and full LED display activity should be avoided.

3 ORDERING INFORMATION

PMS Option	PACKAGE TSSOP(DBT)
Bond Tied to VSS (0)	bq8050DBT ⁽¹⁾

- (1) The bq8050 can be ordered in tape and reel by adding the suffix R to the orderable part number, i.e., bq8050DBTR.

4 FUNCTIONAL BLOCK DIAGRAM



5 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[†]

DESCRIPTION	PINS	VALUE
Supply voltage range, V _{MAX}	VCC, PCHGIN, PCR, PTC, PACK w.r.t. V _{SS}	-0.3 to 34V
	VC1, BAT	V _{VC2} -0.3 to V _{VC2} +8.5 or 34V which ever is lower
	VC2	V _{VC3} -0.3 to V _{VC3} +8.5V
	VC3	V _{VC4} -0.3 to V _{VC4} +8.5V
	VC4	V _{SRP} -0.3 to V _{SRP} +8.5V
	SRP, SRN	-0.3 to V _{REG25} V
	General Purpose open-drain I/O pins, RA4..RA6, RBx	V _{SS} -0.3 V to 6.0 V
	General Purpose push-pull I/O pins, RCx, RA7	-0.3 V to V _{REG25} + 0.3 V
	Input voltage range to all other pins, V _{IN} relative to V _{SS} , /XRST	-0.3 V to V _{REG25} + 0.3 V
	DSG	-0.3 to V _{PACK} +20V or V _{SS} + 34V which ever is lower
	CHG	-0.3 to V _{BAT} + 20V or V _{SS} + 34V which ever is lower
	GPOD, FUSE	-0.3 to 34V
	CELL	-0.3 to V _{REG25} +0.3V
	RBI, REG25	-0.3 to 2.75V
	REG33	-0.3 to 5.0V
Maximum V _{SS} current, I _{SS}		50mA
Current for cell balancing, I _{CB}		10mA
Functional Temperature, T _{FUNC}		-40 to 110°C
Storage temperature range, T _{STG}		-65 to 150°C
Lead temperature (soldering, 10 s), T _{SOLDER}		300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6 RECOMMENDED OPERATING CONDITIONS

Typical values stated where T_A = 25°C and VCC = 14.4V, Min/Max values stated where T_A = -40°C to 85°C and VCC = 3.8V to 25V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	VCC, PACK, PCHGIN, PCR			25	V
	BAT	3.8		V _{VC2} +5.0	
V _{STARTUP}	Start up voltage at PACK	3.0		5.5	V
	VC1, BAT	V _{VC2}		V _{VC2} +5.0	
	VC2	V _{VC3}		V _{VC3} +5.0	
	VC3	V _{VC4}		V _{VC4} +5.0	
	VC4	V _{SRP}		V _{SRP} +5.0	
V _{IN}	VC _n – VC _(n+1) , (n=1, 2, 3, 4)	0		5.0	
	PACK			25	
	PTC	0		2	V
	SRP to SRN	-0.3		1.0	V
C _{REG33}	External 3.3V REG capacitor	1			µF
C _{REG25}	External 2.5V REG capacitor	1			µF
T _{OPR}	Operating temperature	-40		85	°C

6.1 High Voltage General Purpose I/O

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{PU_GPOD}	GPOD Pull Up Voltage			V_{CC}	V
V_{OL_GPOD}	GPOD Output Voltage Low	$I_{OL} = 1\text{mA}$	0.3		V

6.2 General Purpose I/O

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
V_{IH}	High-level input	RAx, RBx, RCx	2.0		V	
V_{IL}	Low-level input	RAx, RBx, RCx		0.8	V	
V_{OH}	Output voltage high	RAx, RBx, RCx, $I_L = -0.5\text{ mA}$	$V_{REG25}-0.5$		V	
V_{OL}	Low-level output voltage	RAx and RCx $I_L = 7\text{mA}$ RBx $I_L = 7\text{mA}$ with $CSx=00$		0.4	V	
C_{IN}	Input capacitance	RAx, RBx and RCx		5	pF	
I_{LKG}	Input leakage current	RAx, RBx and RCx		1	μA	
I_{WPU}	Weak Pull Up Current	RC[3 : 7], RC_WPU[x] = 1; RA7, RA_WPU[x] = 1; $V_{OH} = V_{CC}-0.5\text{V}$	60	120	μA	
$I_{(VOUT)}$	VOUT source currents	VOUT active, $VOUT = V_{REG25}-0.6\text{ V}$	-3		mA	
$I_{LKG(VOUT)}$	VOUT leakage current	VOUT inactive	-0.22	0.22	μA	
$R_{PD(SMBx)}$	SMBx Pull-Down	$T_A = -40$ to 100°C	550	775	1000	$\text{k}\Omega$
$V_{OH(FUSE)}$	High level FUSE output	$V_{CC} = 3.8\text{V}$ to 9V , $C_L = 1\text{nF}$	2.4	8.5	V	
		$V_{CC} = 9\text{V}$ to 25V , $C_L = 1\text{nF}$	7	8		
$V_{IH(FUSE)}$	High level FUSE input		2.8		V	
$t_{R(FUSE)}$	FUSE output rise time	$C_L = 1\text{nF}$, $V_{CC} = 9\text{V}$ to 25V , $V_{OH(FUSE)} = 0\text{V}$ to 5V		5	20	μs
$Z_{O(FUSE)}$	FUSE output impedance			2	5	$\text{k}\Omega$

6.3 General Purpose Current Sink

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{OL}	$V_{OL} = 0.4\text{ V}$, $CSx = 01$		3.5		mA
	$V_{OL} = 0.4\text{ V}$, $CSx = 10$		4.5		
	$V_{OL} = 0.4\text{ V}$, $CSx = 11$		5.5		
I_{CSA}	Current matching between CSx		0.1		mA

6.4 ESD Protected I/O

$T_A = 25^\circ\text{C}$, $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{CONTACT}$	Contact discharge ⁽¹⁾	RA3, RA4/SMBD, RA5, RA6/SMBC, RA7		12	kV
V_{AIR}	Air discharge	RA3, RA4/SMBD, RA5, RA6/SMBC, RA7		16	kV

Note: (1) This value is based on Texas Instruments evaluation module design and is highly application circuit dependent. Results may vary based on the end application design.

6.5 Supply Current

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{CC} AGG Normal Mode	CPU active HFO=LFO=CC=ADC=ON No flash writes, No I/O activity		1.0	2.0	mA
	CPU in HALT, HFO=LFO=CC=ADC=ON No flash writes, No I/O activity		300	380	μA
I_{CC} AFE Normal State	CHG=DSG=LDO=VCELL=ON, CB FETs = OFF, No communication	3.8V < Vcc < 5.0V	220	310	
		5.0V < Vcc	90	120	
I_{SLEEP} Sleep Mode	$T_A = 25^\circ\text{C}$, CPU = HALT, LFO = IWAKE = ON		14	17	μA
			14	27	
I_{SLEEP} AFE Sleep State ⁽¹⁾	CHG=DSG=LDO= ON, VCELL=CB FETs =OFF, No communication	3.8V < Vcc < 5.0V	220	310	μA
		5.0V < Vcc	90	120	
	LDO= ON, VCELL=CB FETs = CHG=DSG=OFF, No communication	3.8V < Vcc < 5.0V	100	120	μA
		5.0V < Vcc	80	95	
$I_{HIBERNATE}$ AGG Hibernate Mode	CPU=HALT, IWAKE=ON		7	18	μA
$I_{SHUTDOWN}$ AFE Shutdown Mode	$T_A = -40^\circ\text{C}$ to 110°C		3.0	3.7	μA

Note 1: AFE Sleep requires the AFE configuration to be set as described. It is not a fixed power mode.

6.6 Gas Gauge Power On Reset (POR)

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TR-} Negative-going voltage input	At REG25	1.9	2.0	2.1	V
V_{HYS} POR Hysteresis	At REG25	65	125	165	mV

6.7 AFE REG33 Power On Reset

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REG33IT-}$ Negative-going voltage input	At REG33	2.3	2.5	2.7	V
$V_{REG33IT+}$ Positive-going voltage input	At REG33	2.4	2.7	3.0	V



bq8050

6.8 AFE REG25 Power On Reset

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REG25T-}$	Negative-going voltage input At REG25	1.15	1.20	1.25	V
$V_{REG25IT+}$	Positive-going voltage input At REG25	2.25	2.35	2.40	V

6.9 AFE Watchdog Reset

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WDWT}	WDT detect time	185	330	475	μs
t_{WDRST}	WDT to reset time	300	560	920	ms
t_{RST}	XRST Active low time	200	340	540	μs
t_{OSC_DETECT}	Oscillator source detection	20	100	160	μs

6.10 RAM Backup

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	$V_{RB} > V_{(RB)MIN}, V_{CC} < V_{IT}$	20	1100	500	nA
	$V_{RB} > V_{(RB)MIN}, V_{CC} < V_{IT}, T_A = 0^\circ\text{C}$ to 70°C				
$V_{(RBI)}$	RBI data-retention voltage ⁽¹⁾	1			V

1 Assured by design. Not production tested.

6.11 Internal 3.3V LDO

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG33}	$3.8\text{V} < VCC \text{ or } BAT \leq 5\text{V}, I_{cc} \leq 4\text{mA}$	2.4	3.5	3.5	V
	$5\text{V} \leq VCC \text{ or } BAT \leq 6.8\text{V}, I_{cc} \leq 13\text{mA}$	3.1	3.3		
	$6.8\text{V} \leq VCC \text{ or } BAT \leq 20\text{V}, I_{cc} \leq 30\text{mA}$				
I_{REG33}	$3.8\text{V} < VCC \text{ or } BAT \leq 5\text{V}$	4		mA	
	$5\text{V} \leq VCC \text{ or } BAT \leq 6.8\text{V}$	13			
	$T_A = -40^\circ\text{C}$ to 70°C	30			
	$T_A = 70^\circ\text{C}$ to 85°C	15			
	$T_A = 85^\circ\text{C}$ to 110°C	500			
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature $VCC \text{ or } BAT = 14.4\text{V}, I_{REG33} = 2\text{mA}$	$T_A = -40^\circ\text{C}$ to 110°C	$\pm 0.2\%$		
$\Delta V_{(VDDLINE)}$	Line regulation $5\text{V} \leq VCC \text{ or } BAT \leq 20\text{V}, I_{REG33} = 2\text{mA}$	$T_A = -40^\circ\text{C}$ to 110°C	1	13	mV
$\Delta V_{(VDDLOAD)}$	Load regulation $VCC \text{ or } BAT = 14.4\text{V}, 0.2\text{mA} \leq I_{REG33} \leq 2\text{mA}$	$T_A = -40^\circ\text{C}$ to 110°C	5	18	mV
	$VCC \text{ or } BAT = 14.4\text{V}, 0.2\text{mA} \leq I_{REG33} \leq 25\text{mA}$		50	110	
$I_{(REG33MAX)}$	Current limit $VCC \text{ or } BAT = 14.4\text{V}, V_{REG33} = 3\text{V}$	$T_A = -40^\circ\text{C}$ to 110°C	70	mA	
	$VCC \text{ or } BAT = 14.4\text{V}, V_{REG33} = 0\text{V}$		33		

6.12 Internal 2.5V LDO

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage $V_{REG33} = 3.1\text{V}$ to 3.5V , $I_{REG25} = 10\text{mA}$	2.35	2.50	2.55	V
I_{REG25}	3.8 V < VCC or $BAT \leq 5\text{V}$	$T_A = -40^\circ\text{C}$ to 110°C	3		mA
	5 V < VCC or $BAT \leq 6.8\text{V}$		12		
	$V_{REG33} = 3.0\text{V}$ to 3.6V , $6.8\text{V} < VCC$ or $BAT \leq 20\text{V}$	$T_A = -40^\circ\text{C}$ to 70°C	16		
		$T_A = 70^\circ\text{C}$ to 85°C	3		
$\Delta V_{(REG25TEMP)}$	Regulator output change with temperature $V_{REG33} = 3.2\text{V}$ to 3.5V , $I_{REG25} = 10\text{mA}$		$\pm 0.25\%$		
$\Delta V_{(REG25LINE)}$	Line regulation $V_{REG33} = 3.2\text{V}$ to 3.5V , $I_{REG25} = 10\text{mA}$	-4	± 1	4	mV
$\Delta V_{(REG25LOAD)}$	Load regulation $V_{REG33} = 3.3\text{V}$, $I_{REG25} = 0.2$ to 10mA	-40	± 20	40	mV
$I_{(REG25MAX)}$	Current limit $V_{REG33} = 3.2\text{V}$ to 3.5V , $V_{REG25} = 2.3\text{V}$			65	mA
	$V_{REG33} = 3.2\text{V}$ to 3.5V , $V_{REG25} = 0\text{V}$			23	mA

6.13 Internal Pre-Charge Limiting

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PCHGMAX}$	Maximum Pre-charge current 3-cell and 4-cell configuration			100	mA
R_{PCHG_RDSON}	$V_{DS(PRECHG)} \geq 1\text{V}$, $VCC < 8.4\text{V}$	30	55	85	Ω
	$V_{DS(PRECHG)} \geq 1\text{V}$, $VCC \geq 8.4\text{V}$	15	30	55	

6.14 SRx Wake From Sleep

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{WAKE}	$V_{WAKE} = 1.2\text{mV}$	0.2	1.2	2.0	mV
	$V_{WAKE} = 2.4\text{mV}$	0.4	2.4	3.6	
	$V_{WAKE} = 5\text{mV}$	2.0	5.0	6.8	
	$V_{WAKE} = 10\text{mV}$	5.3	10	13	
V_{WAKE_TCO}	Temperature drift of V_{WAKE} accuracy			0.5	$\%/\text{ }^\circ\text{C}$
t_{WAKE}	Time from application of current and wake of bq8050			0.2	1
					ms



bq8050

6.15 Coulomb Counter

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range		-0.20		0.25	V
Conversion time	Single conversion		250		ms
Effective resolution	Single conversion	15			Bits
Integral nonlinearity			±0.008	±0.034	%FSR
Offset error ⁽¹⁾			10		µV
Offset error drift			0.3	0.5	µV/°C
Full-scale error		-0.8%	0.2%	0.8%	
Full-scale error drift				150	PPM/°C
Effective input resistance		2.5			MΩ

Notes: (1) Post Calibration Performance

6.16 ADC

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input voltage range	Internal Vref	-0.2		1	V
	External Vref	-0.2	0.8×V _{REG25}		
Conversion time	SPEEDx = 00		31.5		ms
	SPEEDx = 01		16		
	SPEEDx = 10		8		
	SPEEDx = 11		2		
Resolution (no missing codes)	SPEEDx = 00	16			Bits
Effective resolution	SPEEDx = 00	14	15		Bits
	SPEEDx = 01	13	14		
	SPEEDx = 10	11	12		
	SPEEDx = 11	9	10		
Integral nonlinearity	SPEEDx = 00, -0.1 V to 0.8 × Vref		±0.010		%FSR
	SPEEDx = 00, -0.2 V to -0.1 V		±0.020		
	SPEEDx = 01, -0.1 V to 0.8 × Vref		±0.010		
	SPEEDx = 01, -0.2 V to -0.1 V		±0.020		
	SPEEDx = 10, -0.1 V to 0.8 × Vref		±0.020		
	SPEEDx = 10, -0.2 V to -0.1 V		±0.030		
	SPEEDx = 11, -0.1 V to 0.8 × Vref		±0.030		
	SPEEDx = 11, -0.2 V to -0.1 V		±0.050		
Offset error ⁽¹⁾	SPEEDx = 00	70	160		µV
Offset error drift	SPEEDx = 00		1	4	µV/°C
Full-scale error	V _{IN} = 1V	-0.8%	±0.2%	0.4%	
	V _{IN} = -0.2V	-0.9%	±0.2%	0.9%	

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Full -scale error drift	SPEEDx = 00			150	PPM/°C
Effective input resistance		8			MΩ

Note1: Chanel to Chanel Offset

6.17 Cell Voltage Monitor

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
K CELL scale factor	Cell 1, 2, 3 and 4: $\text{VCELL}_+ - \text{VCELL}_-)/(V_{ci} - V_{ci+1})$ when $i=1, 2, 3, 4$ and $V_{ci} - V_{ci+1} = 1\text{V}$ to 5V	0.117	0.119	0.121	
	FUNCTION_CONTROL[BAT] = 1	0.048	0.049	0.051	
	FUNCTION_CONTROL[PACK] = 1	0.048	0.049	0.051	
$V_{(\text{CELLSLEW})}$ CELL output rise	Min to Max 10% to 90%			9	μs
$R_{(\text{BAL})}$ Cell balance internal resistance	$R_{\text{DS(ON)}}$ for internal FET switch at $VDS \geq 2\text{V}$	200	310	430	Ω
	$R_{\text{DS(ON)}}$ for internal FET switch at $VDS \geq 4\text{V}$	60	125	230	

6.18 Internal Temperature Sensor

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{(\text{TEMP})}$ Temperature sensor voltage		-1.9	-2.0	-2.1	mV/°C

6.19 Thermistor Measurement Support

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R Internal resistor		16.5	17.5	19.0	kΩ
R_{DRIFT} Internal Resistor Drift from 25°C				200	PPM/°C
R_{PAD} Internal pin pad resistance		84			Ω

Notes: (1) Post TI calibration and requires firmware to achieve. This has been established as a design goal. This accuracy does not include the ADC as the selection of ADC sampling will affect accuracy

6.20 Internal Thermal Shutdown

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER ⁽¹⁾	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{MAX1} Maximum PCHG temperature		110		150	
T_{MAX2} Maximum REG33 temperature		125		175	°C
T_{RECOVER} Recovery hysteresis temperature				10	°C
t_{PROTECT} Protection time				5	μs

Note 1: Assured by design. Not production tested.



bq8050

6.21 Safety Thermistor Support,

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{PTC} PTC	$V_{PTC} = 0$ to 2V , $T_A = -40^\circ\text{C}$ to 110°C	1.3	2	2.7	$\text{M}\Omega$
$I_{O(PTC)}$ PTC	$V_{PTC} = 0$ to 2V , $T_A = -40^\circ\text{C}$ to 110°C	-450	-370	-230	nA
t_{PTC} PTC Blanking Delay	$T_A = -40^\circ\text{C}$ to 110°C	60	80	110	ms

6.22 High Frequency Oscillator

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc} Operating frequency of CPU Clock			4.194		MHz
$f_{(EO)}$ Frequency error ₍₁₎₍₂₎	$T_A = -20^\circ\text{C}$ to 70°C	-2%	$\pm 0.25\%$	2%	
	$T_A = -40^\circ\text{C}$ to 85°C	-3%	$\pm 0.25\%$	3%	
$t_{(Sxo)}$ Start-up time ₍₃₎	$T_A = -25^\circ\text{C}$ to 85°C		3	6	ms

(1) The frequency error is measured from 4.194 MHz.

(2) The frequency drift is included and measured from the trimmed frequency at $Vcc = 2.5\text{V}$, $T_A = 25^\circ\text{C}$

(3) The startup time is defined as the time it takes for the oscillator output frequency to be $\pm 3\%$ when the device is already powered.

6.23 Low Frequency Oscillator

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(Losc)}$ Operating frequency			32.768		kHz
$f_{(LEO)}$ Frequency error ₍₁₎₍₃₎	$T_A = -20^\circ\text{C}$ to 70°C	-1.5%	$\pm 0.25\%$	1.5%	
	$T_A = -40^\circ\text{C}$ to 85°C	-2.5%	$\pm 0.25\%$	2.5%	
$t_{(Lxo)}$ Start-up time ₍₂₎	$T_A = -25^\circ\text{C}$ to 85°C			100	μs

(1) The frequency drift is included and measured from the trimmed frequency at $VCC = 2.5\text{V}$, $T_A = 25^\circ\text{C}$

(2) The startup time is defined as the time it takes for the oscillator output frequency to be $\pm 3\%$

(3) The frequency error is measured from 32.768 kHz.

6.24 Voltage Reference

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF} Internal Reference Voltage		1.215	1.225	1.230	V
V_{REF_DRIFT} Internal Reference Voltage Drift	$T_A = -25^\circ\text{C}$ to 85°C		± 80		PPM/ $^\circ\text{C}$
	$T_A = 0^\circ\text{C}$ to 60°C		± 50		PPM/ $^\circ\text{C}$

6.25 Flash

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER ⁽¹⁾	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data retention		10			Years
Flash programming write-cycles		20k			Cycles
$t_{WORDPROG}$	Word programming time $T_A = -40^\circ\text{C}$ to 85°C			100	μs
$t_{ROWPROG}$	Row programming time $T_A = -40^\circ\text{C}$ to 85°C			2	ms
$t_{MASSERASE}$	Mass-erase time $T_A = -40^\circ\text{C}$ to 85°C			250	ms
$t_{PAGEERASE}$	Page-erase time $T_A = -40^\circ\text{C}$ to 85°C			25	ms
$I_{CC(PROG_IF)}$	Instruction Flash-write supply current $T_A = -40^\circ\text{C}$ to 85°C		4	6	mA
$I_{CC(PROG_DF)}$	Data Flash-write supply current $T_A = -40^\circ\text{C}$ to 85°C		3	4	mA
$I_{CC(ERASE_IF)}$	Instruction Flash-erase supply current $T_A = -40^\circ\text{C}$ to 85°C		3	18	mA
$I_{CC(ERASE_DF)}$	Data Flash-erase supply current $T_A = -40^\circ\text{C}$ to 85°C		3	18	mA

1: Assured by design. Not production tested

6.26 Current Protection Thresholds

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OCD)}$	$RSNS = 0$	50		200	mV
	$RSNS = 1$	25		100	
$\Delta V_{(OCD)}$	$RSNS = 0$		10		mV
	$RSNS = 1$		5		
$V_{(SCC)}$	$RSNS = 0$	-100		-300	mV
	$RSNS = 1$	-50		-225	
$\Delta V_{(SCC)}$	$RSNS = 0$		-50		mV
	$RSNS = 1$		-25		
$V_{(SCD1)}$	$RSNS = 0$	100		450	mV
	$RSNS = 1$	50		225	
$\Delta V_{(SCD1)}$	$RSNS = 0$		50		mV
	$RSNS = 1$		25		
$V_{(SCD2)}$	$RSNS = 0$	100		450	mV
	$RSNS = 1$	50		225	
$\Delta V_{(SCD2)}$	$RSNS = 0$		50		mV
	$RSNS = 1$		25		
$V_{(OFFSET)}$	SCDx and OCD offset		-10	10	mV
$V_{(Scale_Err)}$	SCDx and OCD scale error		-10%	10%	

6.27 Current Protection Timing

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OCDD}	Over Current in Discharge Delay		1	31	ms
t_{OCDD_STEP}	OCDD Step options		2		ms
t_{SCD1D}	Short Circuit in Discharge Delay AFE.STATE_CNTL[SCDDx2] = 0	0		915	μs
		0		1830	μs
t_{SCD1D_STEP}	SCD1D Step options AFE.STATE_CNTL[SCDDx2] = 0		61		μs
			122		μs
t_{SCD2D}	Short Circuit in Discharge 2 Delay AFE.STATE_CNTL[SCDDx2] = 0	0		458	μs
		0		915	μs
t_{SCD2D_STEP}	SCD2D Step options AFE.STATE_CNTL[SCDDx2] = 0		30.5		μs
			61		μs
t_{SCCD}	Short Circuit in Charge Delay		0	915	μs
t_{SCCD_STEP}	SCCD Step options		61		μs
t_{DETECT}	Current fault detect time $V_{SRP-SRN} = V_{THRESH} + 12.5\text{mV}$, $T_A = -40^\circ\text{C}$ to 85°C			160	μs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time with WDI active	-20%	20%	
		Accuracy of typical delay time with no WDI input	-50%	50%	

6.28 Over Current, Short Circuit Latch Release Support,

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$R_{(RECOVERY)}$	OCD/SCD Recovery detection Register selectable	7		55	kΩ



bq8050

6.29 N-CH FET Drive

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON)}$ Output voltage, charge, and discharge FETs on	$V_{O(FETOND SG)} = V_{(DSG)} - V_{PACK}$, V_{GS} connect $10\text{M}\Omega$, $T_A = -40$ to 85°C	$V_{CC} 3.8 \text{ to } \leq 8.4$	8.0	9.7	12
	$V_{O(FETONCHG)} = V_{(CHG)} - V_{BAT}$, V_{GS} connect $10\text{M}\Omega$, $T_A = -40$ to 85°C	$V_{CC} > 8.4$	9.0	11	12
	$V_{O(FETONCHG)} = V_{(CHG)} - V_{BAT}$, V_{GS} connect $10\text{M}\Omega$, $T_A = -40$ to 85°C	$V_{CC} 3.8 \text{ to } \leq 8.4$	8.0	9.7	12
$V_{(FETOFF)}$ Output voltage, charge and discharge FETs off	$V_{O(FETOFFD SG)} = V_{(DSG)} - V_{PACK}$, $T_A = -40^\circ\text{C}$ to 85°C		-0.4	0.4	V
	$V_{O(FETOFFCHG)} = V_{(CHG)} - V_{BAT}$, $T_A = -40^\circ\text{C}$ to 85°C		-0.4	0.4	
t_r Rise time	$C_L = 4700 \text{ pF}$ $R_G = 5.1\text{k}\Omega$ $V_{CC} < 8.4$	$V_{DSG}: V_{BAT} \geq V_{BAT} + 4 \text{ V}$ $V_{CHG}: V_{PACK} \geq V_{PACK} + 4 \text{ V}$	800	1400	μs
	$C_L = 4700 \text{ pF}$ $R_G = 5.1\text{k}\Omega$ $V_{CC} \geq 8.4$	$V_{DSG}: V_{BAT} \geq V_{BAT} + 4 \text{ V}$ $V_{CHG}: V_{PACK} \geq V_{PACK} + 4 \text{ V}$	200	500	
t_f Fall time	$C_L = 4700 \text{ pF}$ $R_G = 5.1\text{k}\Omega$	$V_{DSG}: V_{C1} + V_{O(FETOND SG)} \geq V_{C1} + 1 \text{ V}$ $V_{CHG}: V_{PACK} + V_{O(FETONCHG)} \geq V_{PACK} + 1 \text{ V}$	80	200	μs
			80	200	

6.30 SMBus

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{CC} = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $V_{CC} = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10	100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2	kHz
t_{BUF}	Bus free time between start and stop		4.7		μs
$t_{HD:STA}$	Hold time after (repeated) start		4.0		μs
$t_{SU:STA}$	Repeated start setup time		4.7		μs
$t_{SU:STO}$	Stop setup time		4.0		μs
$t_{HD:DAT}$	Data hold time		300		ns
$t_{SU:DAT}$	Data setup time		250		ns
$t_{TIMEOUT}$	Error signal/detect	See ⁽¹⁾	25	35	ms
t_{LOW}	Clock low period		4.7		μs
t_{HIGH}	Clock high period	See ⁽²⁾	4.0	50	μs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See ⁽³⁾		25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See ⁽⁴⁾		10	ms
t_F	Clock/data fall time	See ⁽⁵⁾		300	ns
t_R	Clock/data rise time	See ⁽⁶⁾		1000	ns

1. The bq8050 times out when any clock low exceeds $t_{TIMEOUT}$

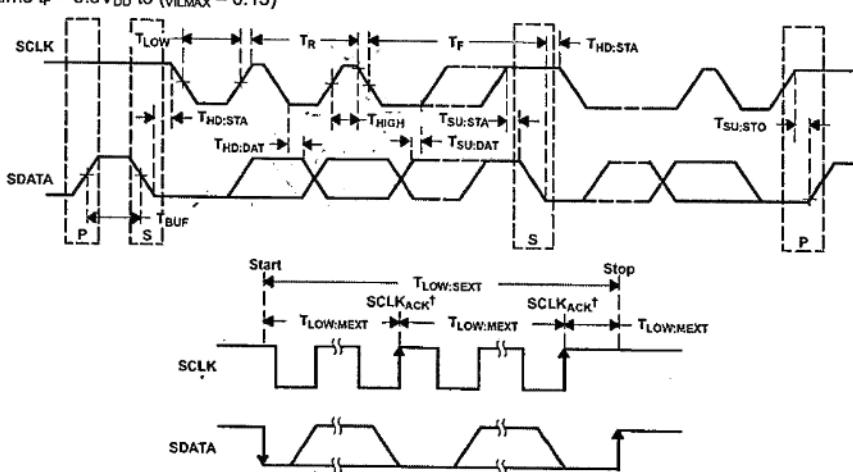
2. t_{HIGH} , Max, is the minimum bus idle time. SMBC = 1 for $t > 50 \mu\text{s}$ causes reset of any transaction involving bq8050 that is in progress. This specification is valid when the THIGH_VAL=0. If THIGH_VAL = 1 then the value of T_{HIGH} is set by THIGH_1,2 and the timeout is not SMBus standard.

3. $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

4. $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.

5. Rise time $t_R = V_{ILMAX} - 0.15$ to $(V_{IHMIN} + 0.15)$

6. Fall time $t_F = 0.9V_{DD}$ to $(V_{ILMAX} - 0.15)$



A. SCLKACK is the acknowledge-related clock pulse generated by the master.



bq8050

6.30.1 SMBus XL

Typical values stated where $T_A = 25^\circ\text{C}$ and $VCC = 14.4\text{V}$, Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C and $VCC = 3.8\text{V}$ to 25V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMBXL}	SMBus XL operating frequency	Slave mode	40	400	kHz
t_{BUF}	Bus free time between start and stop		4.7		μs
$t_{HOLD STA}$	Hold time after (repeated) start		4.0		μs
$t_{SUS STA}$	Repeated start setup time		4.7		μs
$t_{STOP STA}$	Stop setup time		4.0		μs
$t_{TIMEOUT}$	Error signal/detect	See ⁽¹⁾	5	20	ms
t_{LOW}	Clock low period			20	μs
t_{HIGH}	Clock high period	See ⁽²⁾		20	μs

1. The bq8050 times out when any clock low exceeds $t_{TIMEOUT}$

2. t_{HIGH} , Max, is the minimum bus idle time.

7 GENERAL OPERATIONAL OVERVIEW

The bq8050 is a fully integrated battery manager as shown in the functional block diagram. Together with the flash-based firmware, the bq8050 performs the necessary calculations and control for a fully functional battery management system. Each of the major component blocks within the bq8050 is outlined below.

7.1 RISC Processor

The bq8050's flexible architecture allows easy development of numerous battery-management solutions. Based on a RISC processor featuring a Harvard architecture, the bq8050 operates at frequencies up to 4 MHz. The clock frequency is synthesized from an on-chip oscillator. Using a three-stage instruction pipeline, the RISC processor can execute one instruction every clock cycle. With a 22-bit instruction width, the bq8050 can manipulate complex data with a single line of code.

7.2 Data and Program Memory

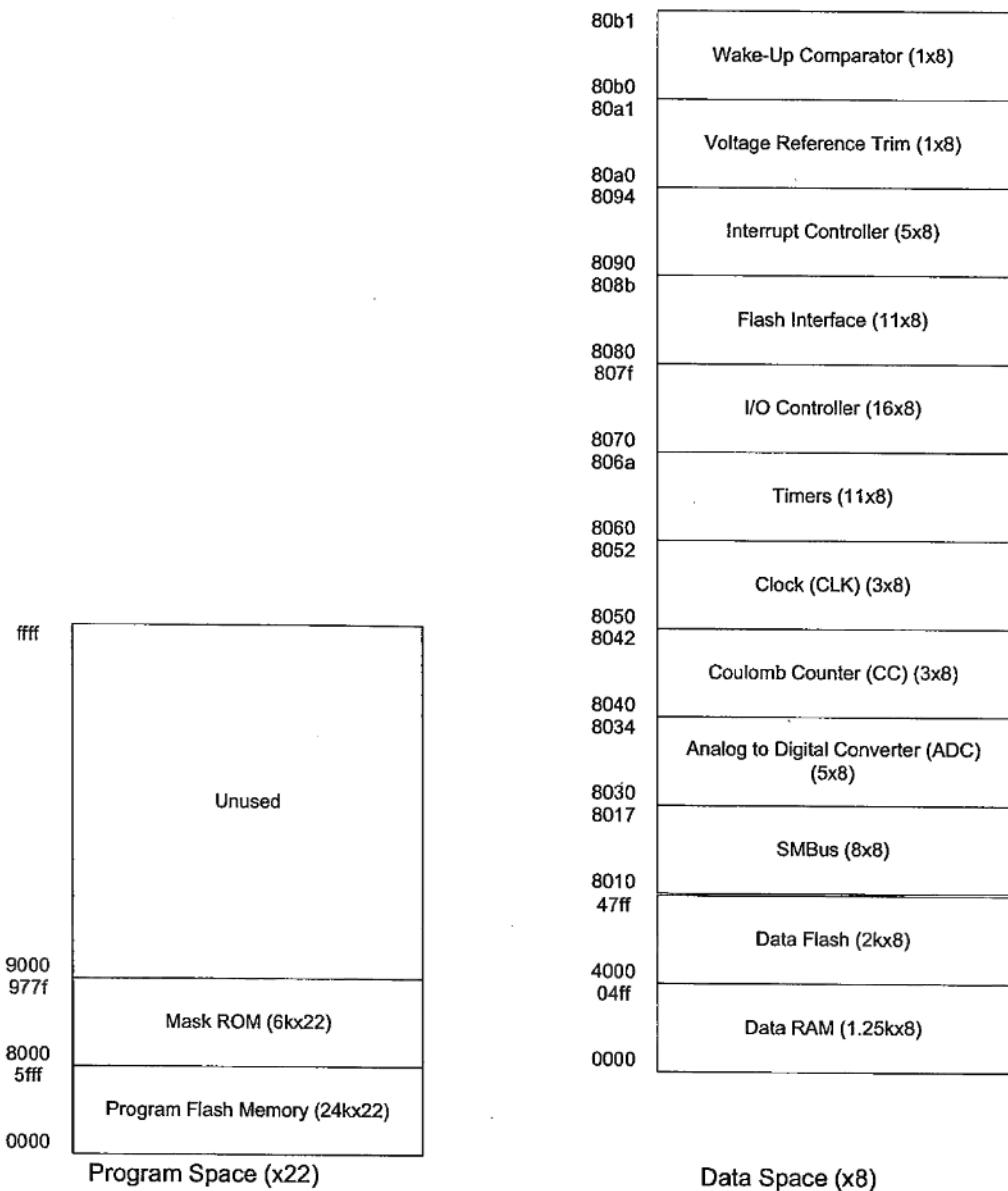
To improve performance and reduce operating power, the bq8050 uses separate data and program memory address busses, providing ample program and data-storage capability.

The bq8050 provides 1280 bytes of data RAM on five 256-byte pages and another 2048 bytes of flash EPROM on another eight 256-byte pages. The flash EPROM is available to store user specific static data, such as serial numbers and system operational data, without modifying the program memory and is erased in 64 byte blocks (2 x 32-byte Words) and programmed in 32 byte blocks (1 Word). The bq8050 provides flexible instruction memory for implementing a wide-variety of battery management functions. For better flash EPROM utilization, the bq8050 instruction memory is separated into two blocks. The first block is a 24k x 22 flash EPROM for custom user programs and the second block is a 6k x 22 mask ROM containing common programs such as the math and battery-management libraries, communication, and power-on reset routines. Refer to the bq8050 Mask ROM description for further details.

In addition, the 1280 bytes of general-purpose SRAM can be powered by the RBI pin of the bq8050 if power is lost. Typically, a capacitor provides the necessary voltage to the SRAM array during inadvertent momentary power loss.



bq8050



7.3 Coulomb Counter

The first ADC is an integrating converter designed specifically for coulomb counting. The converter resolution is a function of how many samples are integrated: 16 samples for $2.5\mu V$ resolution.

7.4 High Voltage Translation

The voltage translation circuit takes the respective voltage inputs of VC1, VC2, VC3, VC4, BAT and PACK and translates them to an analog output suitable for measurement by the ADC. The cell voltages can then be calculated from these input voltages. The voltage is nominally scaled per the following table however, when the device leaves Texas Instruments the calibrated values for each VCx input (K1, K2, K3 and K4), BAT and PACK are stored in the Information Block.

7.5 ADC

The second converter is a 15-bit delta sigma ADC for general-purpose measurements. This converter can be connected to one of eight RC port multiple-purpose I/O pins, an internal temperature sensor, the current sense inputs (SRP and SRN), or the negative power supply (Vss). The converter can also be configured to perform single-ended or fully-differential measurements. In any conversion speed mode, a full 24 bits are returned from the converter for better averaging capability.

7.6 Internal Temperature Sensor

An internal temperature sensor is available on the bq8050 to reduce the cost, power, and size of the external components necessary to measure temperature. Scaled to $-58.6 \text{ LSB}/^{\circ}\text{C}$ in the ADC data registers, the internal temperature sensor is ideal for determining pack temperature during storage and the IC temperature during operations.

7.7 External Temperature Sensor Support

Each of the RC port pins can selected and be enabled with an $18k\Omega$ (typ) linearization pull-up resistor to support the use of a $10k\Omega @ 25^{\circ}\text{C}$ (103) NTC external thermistor such as a Semitec 103AT. One or more thermistors could be connected between VSS and the individual RCx pin. The analog measurement is then taken via the ADC through its input multiplexer. If a different thermistor type is required then external support components are required.

7.8 Safety Thermistor Support

A $4.7M\Omega$ PTC thermistor is connected between PTC pin and Vss. The bq8050 compares this input and will drive the push-pull FUSE pin to V_{FUSE} . If the threshold is exceeded for more than t_{PTC} then the AFE:STATUS[PTC] bit will be set. The PTC bit is cleared through POR only. If the PTC input is not used then it should be connected to VSS via a resistor although this is not required for normal device operation.

7.9 Power On Reset

The bq8050 AFE will reset when the voltage at REG33 falls below $V_{REG33IT-}$ and exits reset when REG33 rises above $V_{REG33IT+}$. The bq8050 AGG will enter reset through the AFE XRST output when REG25 falls below $V_{REG25IT-}$ and will exit reset when REG25 rises above $V_{REG25IT+}$.

7.10 Wake Comparator Operation

The low-power wake comparator peripheral may be used to wake the bq8050 from the sleep state (as long as the low frequency oscillator is enabled, OSC_EN=1) when the voltage across the sense resistor, SRP to SRN, is detected to have exceeded a user selectable threshold. The user also selects the threshold and whether charge current, discharge current or either will wake the part from sleep. This feature can be used when the coulomb counter is enabled.

RSNS1	RSNS0	IWAKE	Vth(SRP-SRN)
0	0	0	Disabled
0	0	1	Disabled
0	1	0	+1.2mV or -1.2mV
0	1	1	+2.mV or -2.mV
1	0	0	+2.4mV or -2.4mV
1	0	1	+5mV or -5mV
1	1	0	+5mV or -5mV
1	1	1	+10mV or -10mV

The wake comparator, when enabled, will continuously sample the sense resistor voltage to determine the level of battery current. Either the WK_CHGF or WK_DSGF flag (see PFLAG2, address 8093h) is set when 6 of 8 sense resistor voltage samples are determined to exceed the selected threshold in either the charge or discharge direction. If the associated event enable bit, WKCEVE for WK_CHGF or WKDEVE for WK_DSGF (see PIE2, address 8094h), is also set, the bq8050 will wake from the sleep state.

7.11 Protection FET Drive

The bq8050 controls 2 external N-CH MOSFETs in a back-to-back configuration for battery protection. The charge (CHG) and discharge (DSG) FETs are automatically turned OFF as a result of appropriate safety controls and can also be turned OFF via command control. The bq8050 can enable a circuit to assist the recover from current based-faults (OCD, SCD1 and SCD2).

7.12 Auto Calibration

The bq8050 can automatically calibrate its offset between the A to D converter and the output of the high voltage translation circuit. Also, the coulomb counter offset can be automatically calibrated for maximum coulomb measurement accuracy.

7.13 Specialized I/O Functions

The bq8050 provides a total of 21 memory-mapped I/O lines in three ports (Ax8, Bx5 and Cx8). These ports are used for data conversion, communication, external-device power interface, external interrupt or wake, and general-purpose control functions. Some pins port pins are hard wired and are internal signals only.

7.13.1 System Interface

The bq8050 provides an SMBus interface (SMBC and SMBD, dual function with RA4 and RA6). Together with the proper firmware, it is compatible with the SMBus v1.1 protocol supporting packet error check (PEC) if enabled. The SMBD and SMBC pins can be enabled with internal pull downs. I²C communication is supported through the ROM and can be applied to any of the GPIO.

7.13.2 High ESD Robust Interface Pins

In conjunction with a 100Ω series resistor the SMBD (RA4), SMBC (RA6) and 3 GPIO (RA3, RA5, RA7) are capable of withstanding Electro-Static Discharge (ESD) events under IEC61000-4-2 (TI QSS 009-010) defined conditions using the TI PCB reference design up to the level of 8kV contact discharge and 15kV air discharge.

With this additional resistance the RA3, RA4, RA5 and RA6 pins are also capable of withstanding a short to the PACK+ pin. RA7 will require extra protection to meet this same level when its integrated weak pull up is used.

7.13.3 Interrupts/Events

The interrupt pins (dual function with RA5 and RA7) provides a hardware means of interrupting the bq8050 during operation. The event pin (dual function with RA3) provides a hardware means of waking the bq8050 during sleep or hibernate modes. The inputs, if enabled, signal the CPU to resume from a HALT state and/or service an interrupt.

7.13.4 High Voltage GPIO

The General Purpose Open Drain (GPOD) output has 1-mA current source drive with a maximum recommended output voltage of 25 V. The GPOD output is enabled or disabled via a register and has a default state of OFF. GPOD is turned OFF under all current fault conditions.

7.13.5 RC Port Pull Ups

The RC port allows for either a strong or weak pull up to be used with each individual RC pin. The strong pull ups are enabled through RC_PUP and the weak pull ups can be enabled through RC_WKPU.

7.13.6 VOUT

VOUT (Dual function with RA7) is a switch power supply of up to 5 mA to an external device under bq8050 firmware control.

7.13.7 PWM

A programmable PWM output is available (Dual function with RC6).

7.14 Internal Interface

7.14.1 Internal device Reset Interface

The AFE XRST output is open drain and is used to drive the /XRST pin of the AGG. The /XRST input has an integrated weak pull-up to ensure a component-free reset interface between the two devices.

7.14.2 Internal Inter-Device Serial Interface

The SCLK and SDATA pins of the respective die are connected. The Inter-Device Communication protocol used is detailed in Inter-Device Interaction

7.14.3 Interrupt Interface

The XALERT pin of the AFE is connected to the INT pin of the AGG allowing the AFE to wake or interrupt the AGG to service a fault condition. XALERT is also triggered when the bq8050 AFE exits POR.

7.14.4 Watchdog Interface

The WDI pin of the AFE is connected to the CLKOUT pin of the AGG allowing the AGG to control the AFE timing more accurately and provide a watchdog timing source. Further details are in Watchdog Reset.

8 Analog-to-Digital Converter (ADC) Operation

The ADC peripheral on the bq8050 consists of an analog multiplexer and a delta-sigma converter. The multiplexer can be configured to connect one of sixteen different signals to the converter. Of these sixteen signals, four are differential configurations for improved noise reduction. For low-power operating modes, the ADC can be turned off under software control by clearing the CONV bit. Typical operation requires only a single write to the ADCTL0 register to simultaneously configure the ADC and issue a convert command.

Configuring the ADC includes selecting the desired voltage reference (VRVDD), conversion speed (SPEED1:SPEED0), and multiplexer channel (CHAN3:CHAN0). The conversion starts on the rising edge of CONV. CONV must be held high until the conversion is complete and data has been read from ADC data registers (ADHI:ADMID:ADLO). The ADC_DRDY bit (bit 0 in ADCTL1 register) is asserted upon completion of a conversion, signaling that valid data is available in the ADC data registers. The ADF flag bit in the PFLAG register is also asserted when ADC_DRDY goes to a one. An interrupt may be generated on the rising edge of ADC_DRDY; see the interrupt control section for details. CONV must be set to a zero before performing additional conversions. This will clear ADC_DRDY, reset the ADC data registers to 800000h, and reset the converter. Once CONV is cleared, the converter is ready to perform additional conversions, or for the setup to change. The data in the ADC data registers is stored in 2s complement format. Full scale (7FFFFFFh) is referred to the reference voltage (Vref) when using the internal reference; or VDD using the external reference. Even though the effective number of bits for a single conversion is 10 bits when SPEED=11, and 15 bits when SPEED=00, a 24-bit result is still provided. Better resolution can be obtained by averaging this 24-bit result across multiple conversions. If 15-bit accuracy is sufficient, reading ADLO is not necessary and should be skipped to simplify mathematical computation.

NOTE: For the specified accuracy, the ADC input range is limited to 80% of the ADC voltage reference input, either V_{DD} or internal V_{ref}.

8.1 ADCTL0 (address 8030h): ADC Control Register

ADCTL0 REGISTER (ADDRESS 8030h)								
	7(MSB)	6	5	4	3	2	1	0
Name	CONV	VRVDD	SPEED1	SPEED2	CHAN3	CHAN2	CHAN1	CHAN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CONV (bit 7): Convert command bit. This bit is used to start a conversion.

1 = Conversion started on the rising edge of CONV; CONV is held high until after valid data are read from ADLO and ADHI (ADC_DRDY =1). ADC is powered on.
 0 = ADC is reset and powered off; ADC_DRDY =0 and ADLO = 00h, ADHI = 80h, ADMID=00h.

VRVDD (bit 6): Voltage reference selection bit. This bit selects which voltage reference (either V_{DD} or internal V_{REF}) is used by the ADC.

1 = Selects V_{DD} as the ADC reference voltage for ratiometric conversions
 0 = Selects the internal V_{REF} as the ADC reference voltage

SPEED1:SPEED0 (bits 5-4)	FILTER LENGTH	CONVERSION TIME
00	8192	31.25 ms
01	4096	16 ms
10	2048	8 ms
11	512	1.95 ms

CHAN3:CHAN0 (bits3-0)	ADC INPUT CHANNEL
0000	RC0
0001	RC1
0010	N/A
0011	RC3
0100	RC4
0101	RC5
0110	RC6
0111	RC7
1000	SRP
1001	SRN
1010	VTEMP
1011	RC0-RC1
1100	RC3-RC4
1101	RC5-RC6
1110	SRP-SRN
1111	VSS

8.2 ADCTL1 (address 8031h): ADC Control Register 1

This register signals when data is ready from the ADC peripheral and controls the ground reference selection.

ADCTL1 REGISTER (ADDRESS 8031h)								
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	GND_SEL	ADC_DRDY
Access	-	-	-	-	-	-	R/W	R
Reset	1	0	0	0	0	0	0	0

Reserved (bits 7:2): Do not use.

GND_SEL (bit 1): Ground select control. This signal controls which ground reference is used in the single-ended conversions.

- 1 = SRN
- 0 = VSS (default)

ADC_DRDY (bit 0): Data ready flag. This read-only bit signals when valid data are ready in ADLO, ADHI and ADMID.

- 1 = Valid data are ready
- 0 = Conversion in progress or ADC held in reset, ADC_DRDY goes low on the falling edge of CONV These store the result of the ADC data after conversion is complete. ADR0 is the LSB and ADR23 is the MSB.

8.3 ADHI, ADMID, ADLO (address 8032h, 8033h, 8034h): ADC Data Registers

ADHI REGISTER (ADDRESS 8032h)								
	7(MSB)	6	5	4	3	2	1	0
Name	ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
Access	R	R	R	R	R	R	R	R
Reset	1	0	0	0	0	0	0	0

ADMID REGISTER (ADDRESS 8033h)



bq8050

	7(MSB)	6	5	4	3	2	1	0
Name	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

	ADL0 REGISTER (ADDRESS 8034h)							
	7(MSB)	6	5	4	3	2	1	0
Name	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

9 Coulomb Counter Operation

The coulomb counter peripheral is a single-channel, over-sampled converter with continuous sampling and is optimized for tracking charge and discharge activity of a rechargeable battery. The coulomb counter (CC) in normal operation is configured to convert the differential voltage across pins SRP and SRN. The coulomb counter design allows the integration of successive samples with no loss or corruption of data.

This integration further reduces quantization error over time, thereby increasing system resolution. The coulomb counter can be turned on or off under firmware control, enabling greater power efficiency. Coulombs are counted by integrating the voltage across a sense resistor placed in series with the negative terminal of a battery. After a power-on reset, the default state of the CC peripheral is off. The CC peripheral is enabled by setting the CC_ON bit to one in the CCCTL register. The CC inputs, SRP and SRN, are configured for normal operation by writing CC_CAL to a zero in the CCCTL register. The conversions begins automatically after CC_ON is set to a one. The converter asserts the CCF flag bit in the PFLAGS register once every 250 ms. An interrupt is generated when CCF is set, assuming CCIE = PIE = GIE = 1. CCLO and CCHI are then read and CCF cleared before another 250 ms have elapsed, avoiding corruption or data loss when the registers are updated following the next conversion.

The data in CCHI-CCLO are stored in 2's complement format. Positive Full scale corresponds to 7FFFh, and negative Full scale corresponds to 8000h. Full scale is referred to approximately VREF divided by four. For a typical Vref of 1.225 V, the complete input range extends from +306 mV to -306mV. However, in order to preserve the specified accuracy, this range is limited to less than 80% of its overall span. Thus the allowable range of voltages for SRN and SRP is - 0.25 V to 0.25 V, and the differential voltage between the two inputs is limited to less than 0.25 V. The least significant bit (LSB) for a simple conversion is $9.35\mu\text{V}$ or 0.65 nVh . The charge LSB is determined by dividing 0.654 nVh by the value of the sense resistor. Resolution is improved by summing (integrating) consecutive samples since no information is lost between conversions.

Calibration cycles can be performed at any time. To perform calibration if the coulomb counter is off, set CC_CAL and CC_ON to one. If the coulomb counter is on, and the conversion result is desired, wait until the conversion is complete and then read the data in CCLO and CCHI. After the data are read, turn the coulomb counter off by writing CC_ON to zero. This ensures that the converter is reset, and another calibration cycle can then be performed by setting CC_CAL and CC_ON to one. If the coulomb counter is on and the conversion result is not wanted, simply turn off the coulomb counter by writing CC_ON to zero.

Calibrations are then performed by setting CC_CAL and CC_ON to one. Averaging of successive conversion results improves the offset resolution and better cancels the offset. One of several offset cancellation algorithms is chosen, depending upon the required performance and operating conditions. A conversion can start immediately after waking from sleep. For dc inputs, a conversion error less than one LSB can be achieved. To save power, turn the converter off by setting CC_ON to a logic zero.



bq8050

9.1 CCCTL (address 8040h): Coulomb Counter Control Register

	CCTL REGISTER (ADDRESS 8040h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CC_ON	CC_CAL
Access	-	-	-	-	-	-	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Reserved (bits 7:2): Do not use.

CC_ON (bit 1): Coulomb counter enable. This bit enables power to the coulomb counter peripheral.

1 = Coulomb counter power turned on

0 = Coulomb counter power turned off and SRP and SRN inputs are high-impedance state

CC_CAL (bit 0): Coulomb counter calibration input control bit. This bit controls the differential input to the coulomb counter.

1 = Both inputs to the coulomb counter driven from SRN for calibration

0 = Coulomb counter inputs driven differentially from pins SRP and SRN for normal operation.

9.2 CCHI, CCLO (address 8041h, 8042h): Coulomb Counter Data Register

Coulomb counter register pair stores the result of the coulomb counter operation in two 8-bit registers, CCLO and CCHI, in 2s complement format where CCR0 is the LSB and CCR15 is the MSB.

	CCHI REGISTER (ADDRESS 8041h)							
	7(MSB)	6	5	4	3	2	1	0
Name	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10	CCR9	CCR8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

	CCLO REGISTER (ADDRESS 8042h)							
	7(MSB)	6	5	4	3	2	1	0
Name	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

10 Clock Generator Peripheral

The clock generator peripheral contains all of the necessary circuitry to generate the internal clocks for the bq8050. The peripheral is composed of an internal high frequency oscillator, internal low frequency oscillator and non-overlapping clock circuit. The nominal clock frequency used by the bq8050 is 4.194 MHz, while the analog circuitry is clocked at 262.144 kHz. The peripheral also provides a 1.049-MHz clock for the SMB engine and a 32.768-kHz clock for the internal timers.

10.1 Low Frequency Oscillator Operation

The 32 kHz clock is generated from a fully integrated oscillator and is trimmed in the factory.

10.2 High Frequency Oscillator Operation

The bq8050 synthesizes the 4.194MHz high frequency clock internally, without the need for external components. Using the more accurate 32.768 kHz clock as a reference, the high frequency clock is adjusted until it is determined to be within the desired operating range. The synthesis circuit continues to monitor and adjust the 4.194 MHz clock as needed. Due to the nature of the synthesis algorithm, some small changes may be noticed in the 4.194MHz clock as it is adjusted based upon operating conditions and the 32.768 kHz reference clock. During the initial startup period the peripherals that require the HFO are held in reset.

10.3 CLKCTL (address 8050h): Clock Control Register

This register contains the clock configuration bits for the bq8050.

	CLKCTL REGISTER (ADDRESS 8050h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	SMB_XL	RSVD	OSC_EN	HF_EN
Access	R	R	R	R	R	R	R/W	R/W
During Reset	0	0	0	0	0	0	0	0
After Reset	0	0	0	0	0	NA	1	1
During and After WD Reset	NA	NA	NA	NA	NA	NA	Prior State	1
WAKE	0	0	0	0	0	NA	1	1

RSVD The RSVD bits are reserved for future revisions.

SMB_XL The SMB_XL bit enables the accelerated SMBus communication.

- 1 = Accelerated SMBus communication is enabled
- 0 = Accelerated SMBus communication is disabled

OSC_EN The OSC_EN bit powers up the internal oscillator circuitry.

- 1 = Internal oscillator is turned on.
- 0 = Internal oscillator is turned off when a halt is issued by the microprocessor.

Note: After an SMBus BUS_LOW timeout has occurred a subsequent transition of SMBC or SMBD from Low to High will automatically enable the internal oscillator.

HF_EN High Frequency Oscillator (HFO) power control bit. This bit enables power to the HFO. This signal is also used to control power to the bias circuitry. When the HFO is enabled, it takes ~4.0 ms until the 1.049-MHz clock comes up.

- 1 = The HFO is turned on.
- 0 = The HFO is turned off when a halt is issued by the microprocessor.

Note: After an SMBus BUS_LOW timeout has occurred a subsequent transition of SMBC or SMBD from Low to High will automatically enable the HFO.

10.4 Timers

There are five timers on the bq8050: an interrupt timer, a bus-low timer, a watchdog timer, PWM timer and a general-purpose 8-bit timer. The reference oscillator operates the interrupt, bus-low, and watchdog timers, so if the reference oscillator is disabled, these timers do not function. The interrupt timer provides a method to schedule tasks via processor interrupts. The bus-low timer is used to detect when the battery pack has been removed from the system. The watchdog timer provides a method for processor reset if processor execution becomes errant. The general purpose timer is used for general purpose firmware tasks and the PWM timer is used to configure the PWM output when enabled.

10.4.1 Interrupt Timer

The interrupt timer is free-running and has a period of 7.8125 ms. When the TIMIE bit (bit 3) is enabled in the PIE register, the interrupt controller requests interrupt servicing at every interrupt timer clock period.

10.4.2 Watchdog and Wake Timer

The watchdog timer provides a method for periodic system reset in the case of errant processor execution. If the WDEN bit in the timer control register is set, and the value in the 16 bit count-up watchdog counter equals the value in the timer program register (concatenated with FFh in the lower byte), a LEVEL 1 reset is generated.

TMRCTLW (address: 8060h): Timer Control Register

	TMRCTLW REGISTER (ADDRESS 8060h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	WDF	WDEN	WKEN	WDRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
After WD Reset	0	0	0	0	1	0	0	0
During Other Reset	0	0	0	0	0	0	0	1
After Other Reset	0	0	0	0	0	0	0	0

RSVD The RSVD bits are reserved and must not be modified by firmware to ensure compatibility with future silicon revisions. These bits are forced to a logic zero.

WDF The WDF bit (bit 3) indicates a watchdog reset has occurred

- 1 = The watchdog reset occurred
- 0 = The watchdog reset has not occurred

WDEN The WDEN bit (bit 2) enables the watchdog timer reset circuit

- 1 = The watchdog reset enabled
- 0 = The watchdog reset disabled

WKEN The WKEN bit (bit 1) enables the wake timer signal.

- 1 = The timer issues a wake signal.
- 0 = No wake signal is provided.

WDRST The WDRST bit (bit 0) clears both the watchdog and wake counter, and must be periodically set by firmware to avoid a watchdog reset. This bit is automatically cleared by the watchdog circuitry after the internal watchdog counter is reset.

- 1 = The watchdog counter is reset
- 0 = Watchdog counting if enabled

If the bq8050 enters hibernation mode (the reference oscillator is stopped), the registers are preserved throughout hibernation if Vcc is above minimum operating voltage, and remains in this state when the bq8050 exits hibernation. If WDEN is high, the watchdog counter is stopped when the reference oscillator is stopped. It resumes counting from the previous point when the reference oscillator starts again.

TMRPERW (address: 8061h): Watchdog and Wake Timer Program Register

TMRPERW REGISTER (ADDRESS 8061h)								
	7(MSB)	6	5	4	3	2	1	0
Name	PERW7	PERW6	PERW5	PERW4	PERW3	PERW2	PERW1	PERW0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

The timer program register sets the wake and watchdog reset time. The minimum wake time is 3.90625 ms when the register is set to 01h. The maximum wake time is 996.09 ms when the program register is set to FFh. The program register allows the user to program the time between the minimum and maximum values in 3.90625 ms steps. The wake and watchdog timer is disabled when TMRPERW is set to 00h.

The program register also sets the watchdog reset time to twice the wake time. Therefore, the minimum watchdog reset time is 7.8125 ms and the maximum reset time is 1.9922 seconds. The programming step size is 7.8125 ms. The watchdog timer can also be programmed to provide a wake signal, which is a processor event to allow the CPU to resume from the HALT state.

Clearing the watchdog timer clears both the watchdog reset signal and the wake signal. The timer control and program registers are only reset by the LEVEL 0 RESET (POR and XRST). The LEVEL 1 RESET (watchdog timer reset) has no effect on these registers. The timer program register does not count down when the wake or watchdog timers are enabled. When programmed, the timer register will maintain its value unless reprogrammed or a LEVEL 0 RESET has occurred.

Since both the wake signal and watchdog reset are operated from the same counter, care must be used when enabling each signal. Enabling one signal while the other signal is already enabled does not reset the state of the counter. To ensure proper operation in this situation the user should clear the counter before enabling the second signal. Clearing can be accomplished by writing 0 to both WDEN and WKEN bits in the TMR_CTLW register followed by setting both enable bits to 1.

10.4.3 GP Timer

The general purpose timer provides a method for a periodic programmable timer for various uses by firmware. This hardware timer has a base period of 122µs, and can be programmed to expire anywhere from 122µs to 31.2ms depending on the value programmed into the GP Timer Period (TMRPERGP) Register. This timer supports both a firmware polling algorithm and a hardware interrupt to the CPU. The firmware polling can be accomplished by periodically reading bit 0 of the Peripheral Flag (PLAG) Register. When bit 0 of the PFLAG register has been set, the timer has expired. A hardware interrupt to the embedded CPU can be enabled by setting bit 0 of the Peripheral Interrupt Enable (PIE) Register. When bit 0 of the PIE register is set, the CPU will be interrupted, and will begin processing an interrupt handler routine. The interrupt handler routine can check the status of bit 0 of the PFLAG to determine whether the GP Timer has expired and is the source of the interrupt. The GP timer supports an automatic reload of the timer. When bit 1 of the GP Timer Control (TMRCTLGP) Register is set, the timer will automatically reload and begin counting down again. In this mode, firmware can utilize this timer as a regular periodic timer, and is not required to re-enable the timer. When operating the GP Timer with the automatic reload enabled, firmware should insure that it can handle servicing of the hardware interrupt prior to subsequent expiration of the timer.

TMRCTLGP (address: 8062h): GP Timer Control Register

	TMRCTLGP REGISTER (ADDRESS 8062h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	GPLOAD	GOPEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RSVD The RSVD bits are reserved and must not be modified by firmware to ensure compatibility with future silicon revisions. These bits are forced to a logic zero.

GPLOAD The GPLOAD bit (bit 1) enables an automatic reload of the timer.

1 = The GP timer will automatically reload, and begin counting down again following expiration of the timer. An interrupt signal will be sent to the interrupt controller each time the timer expires.

0 = The GP timer will countdown until it expires, will send a timer expire signal to the interrupt controller, and will automatically clear the GOPEN bit. Firmware must set the GOPEN bit to re-enable the timer

GOPEN The GOPEN bit (bit 0) enables the GP timer signal.

1 = The GP Timer is enabled. The TMRPERGP register should always be loaded with a valid value prior to setting this bit.

0 = The GP Timer is disabled

TMRPERGP (address: 8063h):GP Timer Period Register

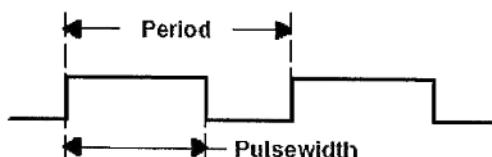
	TMRPERGP REGISTER (ADDRESS 8063h)							
	7(MSB)	6	5	4	3	2	1	0
Name	GPPer7	GPPer6	GPPer5	GPPer4	GPPer3	GPPer2	GPPer1	GPPer0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

GPPer The GPPer bits determine the programmable length of time prior to the timer expiration. The GP timer has a base period of 122us. A value of 00 will equate to 122us GP timer expiration, and a value of FFh will equate to a 31.2ms GP timer expiration.

10.4.4 PWM Mode

A pulse width modulation (PWM) mode is offered where the PWM output is available via RC6 using the 4MHz system clock as reference.

The figure below illustrates a PWM output waveform. A write to the period register (PWMPER) sets the time base, t_{osc} , for this waveform, and a write to the duty cycle register (TMRPWGP defines the output high time.





bq8050

PWMPER (address: 8064h): PWM Period Register

	PWMPER REGISTER (ADDRESS 806xh)							
	7(MSB)	6	5	4	3	2	1	0
Name	PWMPER7	PWMPER6	PWMPER5	PWMPER4	PWMPER3	PWMPER2	PWMPER1	PWMPER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

PWMPER The PWMPER bits determine the programmable length of time prior to the timer expiration where the base frequency (f_{osc}) is 4.194MHz.

$$f_{PWM} = f_{osc} / PWMPER0...7$$

PWMPW (address: 8065h): PWM Pulse Width Register

	PWMPW REGISTER (806xh)							
	7(MSB)	6	5	4	3	2	1	0
Name	PWMPW7	PWMPW 6	PWMPW 5	PWMPW 4	PWMPW 3	PWMPW 2	PWMPW 1	PWMPW 0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

PWMPW0..7 The PWMPWx bits determine the high time (t_{WIDTH}) of the period of the PWM waveform where $t_{WIDTH} = t_{OSCPERIOD} \times PWMPW0..7$

The pulse width register can be written at any time, but this 8-bit value is not used until after a match between the timer count register and the respective period register (PWMPW) occurs, signifying the completion of a period. If the PWM pulse width value exceeds the PWM period, the PWM pin will never be forced low.

When used as a PWM output, the internal pull-up for RC6/PWM is enabled by setting RCPUP6. Writing to the RCOUT6 bits must be avoided during PWM operation, to prevent corrupting the PWM output signal.

11 Mask ROM Functions

The bq8050 default-state is with the flash EPROM erased to all 1s. Upon powering up the bq8050 for the first time, the initialization routine is executed from the mask ROM. After initialization, the bq8050 defaults as an SMBus slave (address 16h). From this point, the flash instruction memory may be programmed. Once the flash programming is complete and the proper commands initiated, the bq8050 executes its program from the flash memory. During normal operation, the library commands in the mask ROM are still available for use.

Access to the ROM is controlled via the ROMGuard feature. This feature requires that a security key is sent to the bq8050 via a command to enable the bq8050 to enter the boot ROM mode. If the command is sent but the key is incorrect the program and data flash is erased and the device reset.

Note: Register bits indicated with a '-' will return a 0 when read and cannot be written (written data is ignored)

Addr.	Symbol	Name	Read/ Write	Bit fields							
				7 (MSB)	6	5	4	3	2	1	0 (LSB)
8010h	SMBMA	SMBus master mode	Write	SMBMA7	SMBMA6	SMBMA5	SMBMA4	SMBMA3	SMBMA2	SMBMA1	R/W_B
8011h	SMBDA	SMBus data	R/W	SMBD7	SMBD6	SMBD5	SMBD4	SMBD3	SMBD2	SMBD1	SMBDO
8012h	SMBACK	SMBus acknowledge	Write	-	-	-	-	-	-	-	ACK
8013h	SMBSTA	SMBus status	Read	BUS_LOW	D_REQ	D_RDY	SA_RDY	NACKED	BUS_FREE	BUSY	MASTER
8014h	SMBCTL	SMBus control	R/W	THIGH_VAL	BLI_EDGE	BLI_EN	PEC_OFF	BFI_EN	SMB_RST	ISOLATE	SA_EN
8015h	SMBPEC	SMBus packet error check	R/W	-	-	-	-	-	PEC_SND	PEC_CHK	PEC_VLD
8016h	SMBTAR	SMB target slave address	R/W	SMBT7	SMBT6	SMBT5	SMBT4	SMBT3	SMBT2	SMBT1	SMBTO
8017h	SMBTOUT	SMB Timeouts	R/W	-	-	-	THIGH_1	THIGH_0	BUSLO_2	BUSLO_1	BUSLO_0
8030h	ADCTL0	ADC control register 0	R/W	CONV	VRVDD	SPEED1	SPEED0	CHAN3	CHAN2	CHAN1	CHAN0
8031h	ADCTL1	ADC control register 1	R/W	-	-	-	-	-	-	-	GND_SEL ADC_DRDY
8032h	ADHI	ADC data register hi byte	Read	ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
8033h	ADMID	ADC data register mid byte	Read	ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
8034h	ADLO	ADC data register low byte	Read	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
8040h	CCCTL	Coulomb counter control register	R/W	-	-	-	-	-	-	CC_ON	CC_CAL
8041h	CCHI	Coulomb counter data high byte	Read	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10	CCR9	CCR8
8042h	CCLO	Coulomb counter data low byte	Read	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
8050h	CLKCTL	Clock control register	R/W	-	-	-	-	SMB_XL	-	OSC_EN	HF_EN
8060h	TMRCTLW	Timer control register	R/W	-	-	-	-	WDF	WDEN	WKEN	WDRST

Addr.	Symbol	Name	Read/ Write	Bit fields							
				7 (MSB)	6	5	4	3	2	1	0 (LSB)
8061h	TMRPERV	Timer program register	R/W	PERW7	PERW6	PERW5	PERW4	PERW3	PERW2	PERW1	PERW0
8062h	TMRCTLGP	GP Timer control	R/W	—	—	—	—	—	PWMEN	GPIOLOAD	GPEN
8063h	TMRPERGP	GP Timer period	R/W	GPPER7	GPPER6	GPPER5	GPPER4	GPPER3	GPPER2	GPPER1	GPPER0
8064h	PWMPER	PWM Period	R/W	PWMPER7	PWMPER6	PWMPER5	PWMPER4	PWMPER3	PWMPER2	PWMPER1	PWMPER0
8065h	PWMPW	PWM Pulse width	R/W	PWMPPW7	PWMPPW6	PWMPPW5	PWMPPW4	PWMPPW3	PWMPPW2	PWMPPW1	PWMPPW0
8070h	RA_OUT	RA output register	R/W	RAOUT7	RAOUT6	RAOUT5	RAOUT4	RAOUT3	RAOUT2	RAOUT1	RAOUT0
8071h	RB_OUT	RB output register	R/W	—	—	—	RBOUT4	RBOUT3	RBOUT2	RBOUT1	RBOUT0
8072h	RC_OUT	RC output register	R/W	RCOUT7	RCOUT6	RCOUT5	RCOUT4	RCOUT3	RCOUT2	RCOUT1	RCOUT0
8073h	RA_IN	Status of RA register inputs	Read	RAIN7	RAIN6	RAIN5	RAIN4	RAIN3	RAIN2	RAIN1	RAIN0
8074h	RB_IN	Status of RB register inputs	Read	—	—	—	RBIN4	RBIN3	RBIN2	RBIN1	RBIN0
8075h	RC_IN	Status of RC register inputs	Read	RCIN7	RCIN6	RCIN5	RCIN4	RCIN3	RCIN2	RCIN1	RCIN0
8076h	RA_IEN	Enable RA input register	R/W	RAIEN7	RAIEN6	RAIEN5	RAIEN4	RAIEN3	RAIEN2	RAIEN1	RAIEN0
8077h	RB_IEN	Enable RC input register	R/W	—	—	—	RBLEN4	RBLEN3	RBLEN2	RBLEN1	RBLEN0
8078h	RC_IEN	Enable RC input register	R/W	RCIEN7	RCIEN6	RCIEN5	RCIEN4	RCIEN3	RCIEN2	RCIEN1	RCIEN0
8079h	IOCTL	IO control register	R/W	32K_OUT	PWMEN	XEVEN	XINTEN2	XINTEN1	SMBEN	—	VOUTEN
807Ah	IOCTL2	IO control register	R/W	—	—	—	CTM_EN	—	—	—	—
807Bh	RA_WKPU	RC Weak Pull-up Enable	R/W	RA_WKPU7	—	—	—	—	—	—	—
807Ch	RC_PUP	RC pullup register	R/W	RCPUP7	RCPUP6	RCPUP5	RCPUP4	RCPUP3	RCPUP2	RCPUP1	RCPUP0

Addr.	Symbol	Name	Read/ Write	Bit fields							
				7 (MSB)	6	5	4	3	2	1	0 (LSB)
807Dh	RC_WKPU	RC Weak Pull-up Enable	R/W	RC_WKPU7	RC_WKPU6	RC_WKPU5	RC_WKPU4	RC_WKPU3	RC_WKPU2	RC_WKPU1	RC_WKPU0
807Eh	CS_HIGH	Current Source Control – Upper	R/W	—	—	—	—	—	—	—	CS4[0]
807Fh	CS_LOW	Current Source Control – Lower	R/W	CS3[1]	CS3[0]	CS2[1]	CS2[0]	CS1[1]	CS1[0]	CS0[1]	CS0[0]
8090h	PFLAG	Peripheral flag register	R/W	SMBF	—	ADF	CCF	TIMF	WKF	—	GPF
8091h	PIE	Peripheral interrupt enable	R/W	SMBIE	—	ADIE	CCIE	TIME	WKEVE	—	TMGIE
8092h	PCTL	Peripheral control	R/W	—	—	—	—	—	—	XIN_EDG	XEV_EDG
8093h	PFLAG2	Peripheral Flag Register	R/W	—	—	—	—	XINT2F	XINTF	WK_CHGF	WK_DSGF
8094h	PIE2	Peripheral Interrupt Enable	R/W	—	—	—	—	—	—	WKCEVE	WKDEVE
80D0h	RCTHERM	RC Thermistor Support Enable	R/W	RCTHERM7	RCTHERM6	RCTHERM5	RCTHERM4	RCTHERM3	RCTHERM2	RCTHERM1	RCTHERM0
80D1h	CUST_TM	Customer Test Mode	R/W	—	—	—	WDI	XRST	XALERT	SCLK	SDATA

12 System Management Bus (SMBus) Peripheral and Operation Interface

The bq8050 system management bus peripheral (SMB) implements the two-wire bidirectional interface and protocol specified in the system management bus v1.1 specification. The SMB peripheral interfaces to the bq8050 CPU via interrupts or register polling. This peripheral can transmit and receive data as either an SMBus master or SMBus slave. The slave address for the bq8050 can be configured to respond automatically to a single slave address, or to multiple addresses if programmed into the bq8050 firmware. The SMBus interface to the bq8050 CPU consists of seven registers and four possible types of interrupts.

12.1 SMB Interrupts

D_RDY (Data Ready)

This indicates that serial data have been received and are available to be read by the bq8050 CPU. This interrupt is asserted before the SMBus acknowledge clock (ACK clock is stretched).

D_REQ (Data Request)

This indicates that the SMB peripheral is ready for data to be sent on the SMBus. The bq8050 CPU must supply these data via a register write. This interrupt is asserted after previous ACK clock (clock after previous ACK is stretched).

BUS_FREE

This indicates that the SMBus is not active.

SA_RDY (Slave Address Ready)

This indicates that a slave address has been received and must be checked by the bq8050 CPU to determine whether the SMB peripheral acknowledges the address. While this event is not typical for SMBus peripherals, this interrupt allows the bq8050 to respond to multiple slave addresses if necessary. The interrupt occurs before ACK clock (ACK clock is stretched).

12.2 Operating as a Slave

Automatic acknowledgement of a slave address requires SA_EN to be set to 0 in the SMB control register (8014h). In this mode, the SMB peripheral monitors the SMBus pins, watching for the slave address programmed in SMBTAR register. When this address has been received, the SMB peripheral ACKs the address and prepares to receive the ensuing command byte. If SA_EN is set to 1, firmware is required to examine the address and determine whether to ACK the address. After this command byte has been received, D_RDY is asserted, signaling the CPU that a command has been successfully received and is available to be read from SMBDA. The CPU must then decode this command and decide whether to ACK or NACK the command by writing to the SMBACK register (8012h), clearing D_RDY. For valid commands that may be either reads or writes, the CPU cannot determine whether to prepare to send data or receive it at this point. To determine whether the command is an SMB read or write:

- If the next SMBus activity consists of a repeated start followed by the repeated target address with LSB = 1, the transaction is a slave read. The SMB ACKs the repeated address and assert D_REQ, signaling the CPU that a slave read is in progress.
- If a repeated start is not received, the SMB is prepared to continue receiving data. Upon reception of eight more bits of data, D_RDY is asserted, signaling the CPU that a slave write is in progress.

12.2.1 For a Slave Read

In response to D_REQ, the CPU must write the required data to the SMBDA register (8011h), clearing D_REQ.

NOTE: The only way to abort the transaction at this point is to not clear D_REQ, causing the SMB to eventually time-out the SMBus and reset.

Upon each succeeding assertion of D_REQ, the status of the master's ACK or NACK of the preceding transmitted byte is checked by reading the NACKED bit. Ordinarily the final data byte is NACKed by the master, indicating the master is finished receiving data. If the expected final data byte is ACKed by the master, this indicates a PEC byte is to be sent. In this case, the PEC_SND bit in the SMBPEC register (8014h) is set in response to D_REQ. This setting clears D_REQ and instructs the SMB peripheral to send a PEC byte; SMBDA should not be written. In response to the final D_REQ with NACKED = 1, the CPU should write a 0 to SMBACK to clear D_REQ.

12.2.2 For a Slave Write

The SMB peripheral is receiving data sent from the master. After each byte of received data, D_RDY is asserted, signaling the CPU that the data byte is ready to be read from SMBDA. The CPU needs to ACK or NACK the byte by writing to the SMBACK register, clearing D_RDY. If a data byte is to be checked as a PEC byte, the PEC_VLD bit in the SMBPEC register is checked after assertion of the final D_RDY and before writing the final ACK (or NACK).

12.3 Operating as a Master

The CPU must first verify that the SMBus is not currently active. Verification is by either polling the BUS_FREE bit in the SMBSTA register or setting the BFI_EN bit in the SMBCTL register. Once the bus is verified inactive, the CPU may then write the address of the slave device it wishes to communicate with to the SMBMA register. If the transaction is a read from the slave, the LSB of this register is written as a 1.

Otherwise, if the transaction is a write to the slave, the LSB is written as a 0. After transmitting the slave address, the SMB peripheral asserts a D_REQ. Then, successful acknowledgment of the address by the slave is indicated by the bit NACKED = 0. If NACKED = 1, the CPU may abort the transaction by writing a 0 to SMBACK. This action clears D_REQ and a stop condition is sent to free the bus. Otherwise, with NACKED = 0, the transaction is continued with the CPU writing the required SMBus command to SMBDA. This clears D_REQ and instructs the SMB peripheral to send the contents of SMBDA on the SMBus. D_REQ is asserted again after the command has been ACKed or NACKed by the slave. If ACKed, the next step is dependent on the LSB of SMBMA.

12.4 SMBMA Register for an LSB = 1: (R/W_B = 1), Master Read

D_REQ is cleared by writing a 1 to SMBACK, causing the SMB peripheral to send a repeated start followed by the repeated SLAVE address with its LSB = 1. This repeated address is ACKed or NACKed by the slave, and is verified by reading the NACKED bit after the next assertion of D_REQ. The D_REQ is cleared by writing a 1 to SMBACK. Then data are sent to the SMB peripheral from the slave device. After each byte of received data, D_RDY is asserted signaling the CPU that the data bit is ready to be read from SMBDA. The CPU then ACKs or NACKs the byte by writing to SMBACK, clearing D_RDY. If a data byte is to be checked as a PEC byte, the PEC_VLD bit is checked after assertion of the final D_RDY and before writing the final NACK. The final data byte to be read, or the PEC byte, is NACKed, which signals the SMB to end the master read and send a stop.

12.5 SMBMA Register for an LSB = 0: (R/W_B = 0), Master Write

D_REQ signals the request for data to be sent to the slave and is cleared by writing the requested data to the SMBDA register. Upon each assertion of D_REQ, the status of the slave's ACK or NACK of the preceding byte is checked by reading the NACKED bit. If a PEC byte is to be sent, PEC_SND is set in response to the D_REQ preceding the byte to be considered a PEC byte. Writing to PEC_SND clears D_REQ; the SMBDA register should not be written. If no more data are to be sent, the CPU should write a 0 to the SMBACK register in response to the final D_REQ, which clears D_REQ and sends a stop.

12.6 SMB Register Details (address 8010h-8017h)

The following is a description of the SMBus registers.

12.6.1 SMBMA (address 8010h): SMBus Master Address Register

A write to this register by the CPU initiates an SMBus master transaction, sets the desired SLAVE address, and signifies the type of SMB master transaction.

	SMBMA REGISTER (ADDRESS 8010h)							
	7(MSB)	6	5	4	3	2	1	0
Name	SMBMA7	SMBMA6	SMBMA5	SMBMA4	SMBMA3	SMBMA2	SMBMA1	R/W_B
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

SMBMA7–1 (bits 7:1): The SMB address of the slave device to be accessed in master mode.

R/W_B (bit 0): SMB master-mode direction control bit. This bit controls the direction of the master-mode transaction

- 1 = Master-mode read transaction from slave
- 0 = Master-mode write transaction to slave

12.6.2 SMBDA (address 8011h): SMBus Data Register

This is the register the CPU uses to transmit data to or receive data from the SMBus where SMBD0 is the LSB and SMBD7 is the MSB.

	SMBDA REGISTER (ADDRESS 8011h)							
	7(MSB)	6	5	4	3	2	1	0
Name	SMBD7	SMBD6	SMBD5	SMBD4	SMBD3	SMBD2	SMBD1	SMBD0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

12.6.3 SMBACK (address 8012h): SMBus Acknowledge Register

This register is used by the CPU to ACK/NACK the previously received data, to send stop condition in master mode, or to reset the SMB engine in response to errors detected on the SMBus.

	SMBACK REGISTER (ADDRESS 8012h)							
	7(MSB)	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	ACK
Access	-	-	-	-	-	-	-	W
Reset	-	-	-	-	-	-	-	0

Reserved (bits 7:1): Do not use.

ACK (bit 0): Acknowledge bit.

- 1 = Acknowledge previous data, send ACK
- 0 = Do not acknowledge previous data, send NACK and reset; send stop if in master mode

12.6.4 SMBSTA (address 8013h): SMBus Status Register

This read-only register reports the status of the SMBus peripheral and SMBus interface.

	SMBSTA REGISTER (ADDRESS 8013h)							
	7(MSB)	6	5	4	3	2	1	0
Name	BUS_LOW	D_REQ	D_RDY	SA_RDY	NACKED	BUS_FREE	UNIT_BUSY	MASTER
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	1	0

BUS_LOW (bit 7): SMBus Low bit. Indicates current state of BUS_LOW flag.

- 1 = BUS_LOW asserted, indicating a bus low timeout had occurred
- 0 = BUS_LOW not asserted

D_REQ (bit 6): Data request bit. This bit indicates current state of D_REQ interrupt.

- 1 = D_REQ asserted
- 0 = D_REQ not asserted

D_RDY (bit 5): Data ready bit. This bit indicates current state of D_RDY interrupt.

- 1 = D_RDY asserted
- 0 = D_RDY not asserted

SA_RDY (bit 4): Slave address ready bit. This bit indicates current state of SA_RDY interrupt.

- 1 = SA_RDY asserted
- 0 = SA_RDY not asserted

NACKED (bit 3): Not acknowledged bit. This bit indicates state of previously sent data's acknowledgment by the destination device (also indicates lost arbitration as a master).

- 1 = Previous data NACKed, or SMB has lost arbitration while operating as a master
- 0 = Previous data successfully ACKed

BUS_FREE (bit 2): Bus free bit. This bit indicates active state of the SMBus.

- 1 = SMBus inactive
- 0 = Activity detected on the SMBus

UNIT_BUSY (bit 1): SMB peripheral busy bit. This bit indicates active state of SMB engine.

- 1 = SMB engine processing an SMBus transaction as either a master or slave
- 0 = SMB engine idle

MASTER (bit 0): Master bit. This bit indicates whether or not the SMB engine is currently operating as an SMBus master.

- 1 = SMB engine has successfully attained master mode
- 0 = SMB engine is not currently operating as an SMBus master

12.6.5 SMBCTL (address 8014h): SMBus Control Register

This read-write register controls the operation of the SMBus peripheral.

	SMBCTL REGISTER (ADDRESS 8014h)							
	7(MSB)	6	5	4	3	2	1	0
Name	THIGH_VAL	BLI_EDGE	BLI_EN	PEC_DIS	BFI_EN	SMB_RST	ISOLATE	SA_EN
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	0	0	0

THIGH_VAL (bit 7): SMBus high time timeout enable extended t_{HIGH} time bit. This bit enables the THIGH1 and THIGH0 bits to configure the t_{HIGH} value.

1 = SMBus high time timeout is configured by SMBTOUT [THIGH1, THIGH0]

0 = SMBus high time standard timeout enabled, conforms to SMBus specifications

BLI_EDGE (bit 6): Bus low interrupt polarity bit. This bit determines whether to generate an interrupt when BUS_LOW goes active, or when BUS_LOW goes inactive. BLI_EN must be set to trigger a bus low interrupt. BLI_EDGE should only be set if BUS_LOW is already active.

1 = If BLI_EN=1, generates an interrupt when BUS_LOW goes inactive.

0 = If BLI_EN=1, generates an interrupt when BUS_LOW goes active.

BLI_EN (bit 5): Bus low interrupt enable bit. This bit is used to enable SMB bus low timeout detection, and will generate an SMB interrupt if the SMBus clock and data lines have both been low for a time exceeding the programmable SMB bus low timeout (SMBBUSLO register, default=2s). This bit can be used to implement the charger broadcast re-enable function as described in the Smart Battery Data specification.

1 = Enable SMB bus low detection.

0 = Disable SMB bus low detection.

PEC_DIS (bit 4): Packet error checking engine disable bit. This bit disables PEC engine to conserve power if PEC checking or generation is not required.

1 = PEC engine disabled

0 = PEC engine enabled

BFI_EN (bit 3): Bus free interrupt enable bit. This bit enables interrupt when BUS_FREE is set.

1 = Assert interrupt in response to BUS_FREE assertion

0 = Mask assertion of interrupt in response to BUS_FREE assertion; BUS_FREE must be polled to determine active state of SMBus

SMB_RST (bit 2): SMB engine software reset bit.

1 = Reset SMB engine

0 = SMB normal operation

ISOLATE (bit 1) : SMBus isolation bit. This bit isolates SMB peripheral from SMBus.

1= Disconnect SMB peripheral from SMBus

0 = SMB normal operation

SA_EN (bit 0): Slave address detection enable bit. This bit enables assertion of SA_RDY to allow the device to respond to multiple slave addresses.

1 = SA_RDY asserted in response to any slave address detected on SMBus; CPU required to ACK or NACK address via SMBACK

0 = SMB normal operation; SMB engine ACKs address programmed in SMBTAR without CPU intervention



bq8050

12.6.6 SMBPEC (address 8015h): SMBus Packet Error Check Register

This register manages the PEC generation and control for SMBus transactions.

	SMBPEC REGISTER (ADDRESS 8015h)							
	7(MSB)	6	5	4	3	2	1	0
Name	-	-	-	-	-	PEC_SND	PEC_CHK	PEC_VLD
Access	-	-	-	-	-	R/W	R/W	R/W
Reset	-	-	-	-	-	0	0	0

Reserved (bits 7:3): Do not use.

PEC_SND (bit 2): PEC send bit. This bit instructs SMB engine to send calculated PEC byte of previously transmitted SMBus data; it is set in response to a DATA_REQ assertion.

1 = Send PEC byte (cleared by hardware)

0 = Do not send PEC byte

PEC_CHK (bit 1): PEC check bit. This bit instructs SMB engine to expect calculated PEC byte of previously transmitted SMBus data, or successful non-PEC termination of proceeding transaction; it is set in response to a D_RDY assertion.

1 = Check PEC byte (cleared by hardware)

0 = Do not check PEC byte

PEC_VLD (bit 0): PEC valid bit. This bit indicates validity of previously received PEC byte or successful non-PEC termination of previous SMBus transaction; it is read only in response to a D_RDY assertion.

1 = PEC byte was valid or a valid stop was received for a non-PEC transaction

0 = PEC byte was not valid

12.6.7 SMBTAR (address 8016h): SMBus Target Slave Register

This register contains the slave address that the SMB engine responds to where SMBT0 is the LSB and SMBT7 is the MSB.

	SMBTAR REGISTER (ADDRESS 8016h)							
	7(MSB)	6	5	4	3	2	1	0
Name	SMBT7	SMBT6	SMBT5	SMBT4	SMBT3	SMBT2	SMBT2	SMBT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	1	1	0



bq8050

12.6.8 SMBTOUT (address 8017h): SMBus Timeout Program Register

This register is used to adjust the length of time before an SMB bus high or low timeout violation occurs.

NOTE: Adjusting this register from the default value will violate the SMBus spec for BUS LOW or t_{HIGH} timeout.

SMBTOUT REGISTER (ADDRESS 8017h)								
	7(MSB)	6	5	4	3	2	1	0
Name	-	-	-	THIGH_1	THIGH_0	BUSLO_2	BUSLO_1	BUSLO_0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset	-	-	-	0	0	1	0	0

Reserved (bits 7:5): Do not use.

THIGH_[1:0]: SMBus t_{HIGH} timeout select. These bits select timeout period for t_{HIGH} to be asserted:

- 00 = never (default value)
- 01 = 512µs
- 10 = 1ms
- 11 = 15ms

BUSLO_[2:0]: SMBus bus low timer select. These bits select timeout period for BUS_LOW to be asserted:

- 000 = never
- 001 = 0.075s
- 010 = 1.0 s
- 011 = 1.5 s
- 100 = 2.0 s (default reset value)
- 101 = 2.5 s
- 110 = 3.0 s
- 111 = 3.5 s

13 I/O Pin Controller

The I/O controller manages the operation of the three general-purpose data ports on the bq8050. These three ports, pins RA[x:0], RB[x:0] and RC[x:0] function independently as digital input pins, digital open-drain output pins, or both. In addition, the pins of the RC port can be selected as analog inputs to the analog-to-digital converter peripheral (ADC) and can be programmed to enable internal pull-ups to provide full push-pull digital output functionality. Also, the pins of the RB port can be selected as programmable current sinks. Several of the RA and RC pins have predefined functionality providing communication interfaces for the serial communication peripheral, and providing external interrupt/event conditions to the RISC processor. The predefined functions can be disabled on the basis of the user program. The predefined pins are:

RA0 – Interrupt pin
RA7 – Interrupt pin with internal weak pull-up
RA3 – External event pin
RA4 – SMBus data pin
RA6 – SMBus clock pin
RA7 – VOUT pin (voltage supply output)
RC2/CLKOUT – 32kHz Output pin
RC3...7 – External Thermistor Inputs
RC6 – PWM output

13.1 RA_OUT (address 8070h): RA Output Register

The RA output register controls the output state of the RA pins.

	RA_OUT REGISTER (ADDRESS 8070h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RAOUT7	RAOUT6	RAOUT5	RAOUT4	RAOUT3	RAOUT2	RAOUT1	RAOUT0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	1	1	1	1	1	1	0	1

RAOUT7 (bit 7):

- 1 = Drive pin RA7/VOUT to a logic 1 if VOUTEN=1; otherwise, RA7 is open-drain 3-state
- 0 = Drive pin RA7 to a logic 0

RAOUT6 (bit 6):

- 1 = Do not drive pin RA6 (open drain 3-state); required state for using SMBC
- 0 = Drive pin RA6 to a logic 0

RAOUT5 (bit 5):

- 1 = Do not drive pin RA5 (open drain 3-state);
- 0 = Drive pin RA5 to a logic 0

RAOUT4 (bit 4):

- 1 = Do not drive pin RA4 (open drain 3-state); required state for using SMBD
- 0 = Drive pin RA4 to a logic 0

RAOUT3 (bit 3):

- 1 = Do not drive pin RA3 (open drain 3-state); required state for using EVENT
- 0 = Drive pin RA3 to a logic 0

RAOUT2 (bit 2):

- 1 = Do not drive pin RA2 (open drain 3-state);
- 0 = Drive pin RA2 to a logic 0

RAOUT1 (bit 1):

- 1 = Do not drive pin RA1 (open drain 3-state);
- 0 = Drive pin RA1 to a logic 0

RAOUT (bit 0) = 1 as RA0 can not be configured as an output.

13.2 RB_OUT (address 8071h): RB Output Register

The RB output register controls the output state of the RB pins.

	RB_OUT REGISTER (ADDRESS 8071h)							
	7(MSB)	6	5	4	3	2	1	0
Name	-	-	-	RBOUT4	RBOUT3	RBOUT2	RBOUT1	RBOUT0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

RBOUT7...5 (bit 7...5): Not Used

RBOUT4 (bit 4):

- 1 = Do not drive pin RB4 (open drain 3-state)
- 0 = Drive pin RB4 to a logic 0

RBOUT3 (bit 3):

- 1 = Do not drive pin RB3 (open drain 3-state)
- 0 = Drive pin RB3 to a logic 0

RBOUT2 (bit 2):

- 1 = Do not drive pin RB2 (open drain 3-state)
- 0 = Drive pin RB2 to a logic 0

RBOUT1 (bit 1):

- 1 = Drive pin RB1 (open drain 3-state)
- 0 = Drive pin RB1 to a logic 0

RBOUT0 (bit 0):

- 1 = Drive pin RB0 (open drain 3-state)
- 0 = Drive pin RB0 to a logic 0

13.3 RC_OUT (address 8072h): RC Output Register

This register controls the output state of the RC pins.

	RC_OUT REGISTER (ADDRESS 8072h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RCOUT7	RCOUT6	RCOUT5	RCOUT4	RCOUT3	RCOUT2	RCOUT1	RCOUT0
Access	R/W	R/W	R/W	R/W	R/W	R	R	R
Reset	1	1	1	1	1	0	1	1

RCOUT7 (bit 7):

- 1 = If RCPUP7=1, drive pin RC7 to a logic 1. If RC_WKPU7=1, drive pin RC7 to a weak
- 1. If RCPUP7=RC_WKPU7=0, do not drive pin RC7 (open-drain 3-state)
- 0 = Drive pin RC7 to a logic 0

RCOUT6 (bit 6):

- 1 = If RCPUP6=1, drive pin RC6 to a logic 1. If RC_WKPU6=1, drive pin RC6 to a weak
- 1. If RCPUP6=RC_WKPU6=0, do not drive pin RC6 (open-drain 3-state)
- 0 = Drive pin RC6 to a logic 0

RCOUT5 (bit 5):

- 1 = If RCPUP5=1, drive pin RC5 to a logic 1. If RC_WKPU5=1, drive pin RC5 to a weak
- 1. If RCPUP5=RC_WKPU5=0, do not drive pin RC5 (open-drain 3-state)
- 0 = Drive pin RC5 to a logic 0

RCOUT4 (bit 4):

- 1 = If RCPUP4=1, drive pin RC4 to a logic 1. If RC_WKPU4=1, drive pin RC4 to a weak
- 1. If RCPUP4=RC_WKPU4=0, do not drive pin RC4 (open-drain 3-state)
- 0 = Drive pin RC4 to a logic 0

RCOUT3 (bit 3):

- 1 = If RCPUP3=1, drive pin RC3 to a logic 1. If RC_WKPU3=1, drive pin RC3 to a weak
- 1. If RCPUP3=RC_WKPU3=0, do not drive pin RC3 (open-drain 3-state)
- 0 = Drive pin RC3 to a logic 0

RC_OUT (bit 2): This is used for a 32kHz output only.

RC_OUT (bit 0,1): are analog inputs only and can not be selected as outputs.

13.4 RA_IN (address 8073h): RA Input Status Register

This register controls the output state of the RA pins.

	RA_IN REGISTER (ADDRESS 8073h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RAIN7	RAIN6	RAIN5	RAIN4	RAIN3	RAIN2	RAIN1	RAIN0
Access	R	R	R	R	R	R	R	R
Reset	0	0	1	0	0	0	0	1

RAIN7 (bit 7):

- 1 = Logic value driven on pin RA7 if RAIEN7=1
- 0 = Logic 0 value driven on pin RA7

RAIN6 (bit 6):

- 1 = Logic value driven on pin RA6 if RAIEN6=1
- 0 = Logic 0 value driven on pin RA6

RAIN5 (bit 5):

- 1 = Logic value driven on pin RA5 if RAIEN5=1
- 0 = Logic 0 value driven on pin RA5

RAIN4 (bit 4):

- 1 = Logic value driven on pin RA4 if RAIEN4=1
- 0 = Logic 0 value driven on pin RA4

RAIN3 (bit 3):

- 1 = Logic value driven on pin RA3 if RAIEN3=1
- 0 = Logic 0 value driven on pin RA3

RAIN2 (bit 2):

- 1 = Logic value driven on pin RA2 if RAIEN2=1
- 0 = Logic 0 value driven on pin RA2

RAIN1 (bit 1):

Is in only an output and can not be configured as an input.

RAIN0 (bit 0):

- 1 = Logic value driven on pin RA0 if RAIEN0=1
- 0 = Logic 0 value driven on pin RA0

13.5 RB_IN (address 8074h): RB Input Status Register

This register controls the output state of the RB pins.

	RB_IN REGISTER (ADDRESS 8074h)							
	7(MSB)	6	5	4	3	2	1	0
Name	-	-	-	RBIN4	RBIN3	RBIN2	RBIN1	RBIN0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

RBIN7...5 (bit 7...5): Not Used

RBIN4 (bit 4):

- 1 = Logic value driven on pin RB4 if RBIEN4=1
- 0 = Logic 0 value driven on pin RB4

RBIN3 (bit 3):

- 1 = Logic value driven on pin RB3 if RBIEN3=1
- 0 = Logic 0 value driven on pin RB3

RBIN2 (bit 2):

- 1 = Logic value driven on pin RB2 if RBIEN2=1
- 0 = Logic 0 value driven on pin RB2

RBIN1 (bit 1):

- 1 = Logic value driven on pin RB1 if RBIEN1=1
- 0 = Logic 0 value driven on pin RB1

RBIN0 (bit 0):

- 1 = Logic value driven on pin RB0 if RBIEN0=1
- 0 = Logic 0 value driven on pin RB0

13.6 RC_IN (address 8075h): RC Input Status Register

This register controls the output state of the RC pins.

	RC_IN REGISTER (ADDRESS 8075h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RCIN7	RCIN6	RCIN5	RCIN4	RCIN3	RCIN4	RCIN2	RCIN0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

RCIN7 (bit 7):

- 1 = Logic value driven on pin RC7 if RCIEN7=1
- 0 = Logic 0 value driven on pin RC7

RCIN6 (bit 6):

- 1 = Logic value driven on pin RC6 if RCIEN6=1
- 0 = Logic 0 value driven on pin RC6

RCIN5 (bit 5):

- 1 = Logic value driven on pin RC5 if RCIEN5=1
- 0 = Logic 0 value driven on pin RC5

RCIN4 (bit 4):

- 1 = Logic value driven on pin RC4 if RCIEN4=1
- 0 = Logic 0 value driven on pin RC4

RCIN3 (bit 3):

- 1 = Logic value driven on pin RC3 if RCIEN3=1
- 0 = Logic 0 value driven on pin RC3

RCIN2 (bit 2): This is used for 32kHz output only

RCIN1,0 (bit1, 0): These bits are analog inputs only and cannot be configured as outputs.

13.7 RA_IEN (address 8076h): RA Input Enable Register

This register enables the RA register as an input.

	RA_IEN REGISTER (ADDRESS 8076h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RAIEN7	RAIEN6	RAIEN5	RAIEN4	RAIEN3	RAIEN2	RAIEN1	RAIENO
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

RAIEN7 (bit 7):

- 1 = Enable reading of logic value on pin RA7 via RAIN7
- 0 = Disable reading of logic value and guard against floating input levels on pin RA7

RAIEN6 (bit 6):

- 1 = Enable reading of logic value on pin RA6 via RAIN6
- 0 = Disable reading of logic value and guard against floating input levels on pin RA6

RAIEN5 (bit 5):

- 1 = Enable reading of logic value on pin RA5 via RAIN5
- 0 = Disable reading of logic value and guard against floating input levels on pin RA5

RAIEN4 (bit 4):

- 1 = Enable reading of logic value on pin RA4 via RAIN4
- 0 = Disable reading of logic value and guard against floating input levels on pin RA4

RAIEN3 (bit 3):

- 1 = Enable reading of logic value on pin RA3 via RAIN3
- 0 = Disable reading of logic value and guard against floating input levels on pin RA3

RAIEN2 (bit 2):

- 1 = Enable reading of logic value on pin RA2 via RAIN2
- 0 = Disable reading of logic value and guard against floating input levels on pin RA2

RAIEN1 (bit 1): This is only an output and can not be configured as an input.

RAIENO (bit 0):

- 1 = Enable reading of logic value on pin RA0 via RAIN0
- 0 = Disable reading of logic value and guard against floating input levels on pin RA0

13.8 RB_IEN (address 8077h): RB Input Enable Register

This register enables the RB pins as inputs.

RB_IEN REGISTER (ADDRESS 8077h)								
	7(MSB)	6	5	4	3	2	1	0
Name	-	-	-	RBIEN4	RBIEN3	RBIEN2	RBIEN1	RBIENO
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

RBIEN7...5 (bit 7...5): Not Used

RBIEN4 (bit 4):

- 1 = Enable reading of logic value on pin RB4 via RBIN4 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RB4

RBIEN3 (bit 3):

- 1 = Enable reading of logic value on pin RB3 via RBIN3 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RB3

RBIEN2 (bit 2):

- 1 = Enable reading of logic value on pin RB2 via RBIN2 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RB2

RBIEN1 (bit 1):

- 1 = Enable reading of logic value on pin RB1 via RBIN1 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RB1

RBIEN0 (bit 0):

- 1 = Enable reading of logic value on pin RB0 via RBIN0 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RB0

13.9 RC_IEN (address 8078h): RC Input Enable Register

This register enables the RC pins as inputs.

	RC_IEN REGISTER (ADDRESS 8078h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RCIEN7	RCIEN6	RCIEN5	RCIEN4	RCIEN3	RCIEN2	RCIEN1	RCIEN1
Access	R/W	R/W	R/W	R/W	R/W	R	R	R
Reset	0	0	0	0	0	0	0	0

RCIEN7 (bit 7):

- 1 = Enable reading of logic value on pin RC7 via RCIN7 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RC7

RCIEN6 (bit 6):

- 1 = Enable reading of logic value on pin RC6 via RCIN6 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RC6

RCIEN5 (bit 5):

- 1 = Enable reading of logic value on pin RC5 via RCIN5 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RC5

RCIEN4 (bit 4):

- 1 = Enable reading of logic value on pin RC4 via RCIN4 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RC4

RCIEN3 (bit 3):

- 1 = Enable reading of logic value on pin RC3 via RCIN3 bit
- 0 = Disable reading of logic value and guard against floating input levels on pin RC3

RCIEN2 (bit 2): This is used for 32kHz output only

RCIEN1,0 (bit1, 0): These are analog inputs only and can not be configured as digital inputs

13.10 IOCTL (address 8079h): Input/Output Control Register

This register enables the predefined pin functions for RA0, RA2, RA3, RA4, RA5, RA6, RA7, RC0, and RC4 pins.

	IOCTL REGISTER (ADDRESS 8079h)							
	7(MSB)	6	5	4	3	2	1	0
Name	32K_OUT	PWMEN	XEVENT	XINTEN2	XINTEN1	SMBEN	-	VOUTEN
Access	R/W	R/W	R	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	1	0	0

32K_OUT (bit 7): Enable 32.768kHz output

- 1 = Enable 32.768 kHz clock on RC2
- 0 = Disable 32.768 kHz output on RC2

PWMEN (bit 6): Enable Timer PWM output on RC6

- 1 = Enable PWM output on RC6
- 0 = Disable PWM output on RC6

XEVENT (bit 5): Enable external event pin

- 1 = Enable pin RA3 to function as CPU external event pin (RAIEN3 must also be set)
- 0 = Disable CPU external event functionality for pin RA3

XINT2EN (bit 4) : Enable external interrupt (INT2) pin

- 1 = Enable pin RA7 to function as CPU external interrupt pin (RAIEN7 must also be set)
- 0 = Disable CPU external interrupt functionality for pin RA7

XINT1EN (bit 3) : Enable external interrupt (INT1) pin

- 1 = Enable pin RA5 to function as CPU external interrupt pin (RAIEN5 must also be set)
- 0 = Disable CPU external interrupt functionality for pin RA5

SMBEN (bit 2): Enable SMBus pins

- 1 = Enable pins RA4 and RA6 to function as SMB data and SMB clock (RAIEN4 and RAIEN6 must also be set)
- 0 = Disable SMBus functionality for pins RA4 and RA6

Note: If Bit 4 **AND** bit 0 are set then bit 4 (INT2) takes priority

VOUTEN (bit 0): Enable VOUT pin

- 1 = Enable pin RA7 to function as the VOUT power source pin
- 0 = Disable VOUT function for pin RA7

13.11 IOCTL2 (address 807ah): Input/Output Control 2 Register

This register enables the predefined pin functions.

	IOCTL REGISTER (ADDRESS 8079h)							
	7(MSB)	6	5	4	3	2	1	0
Name	-	-	-	CTM_EN	-	-	-	-
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

CTM_EN (bit 4) Enables the Customer Test Mode

- 0 = Customer Test Mode interface disabled
- 1 = Customer Test Mode interface enabled

13.12 RA_WKPU (address 807Bh): RA Control Register

This register enables the internal weak pull-ups for the RA pins.

	RC_PUP REGISTER (ADDRESS 807Bh)							
	7(MSB)	6	5	4	3	2	1	0
Name	RAWKPU7	-	-	-	-	-	-	-
Access	R/W	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

RAWKPU7 (bit 7):

- 1 = Enable internal weak pull-up for pin RA7
- 0 = Disable internal weak pull-up for pin RA7

13.13 RC_PUP (address 807Ch): RC Control Register

This register enables the internal pull-ups for the RC pins.

	RC_PUP REGISTER (ADDRESS 807Ch)							
	7(MSB)	6	5	4	3	2	1	0
Name	RCPUP7	RCPUP6	RCPUP5	RCPUP4	RCPUP3	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R	R	R
Reset	0	0	0	0	0	0	0	0

RCPUP7 (bit 7):

- 1 = Enable internal pullup for pin RC7
- 0 = Disable internal pullup for pin RC7

RCPUP6 (bit 6):

- 1 = Enable internal pullup for pin RC6
- 0 = Disable internal pullup for pin RC6

RCPUP5 (bit 5):

- 1 = Enable internal pullup for pin RC5
- 0 = Disable internal pullup for pin RC5

RCPUP4 (bit 4):

- 1 = Enable internal pullup for pin RC4
- 0 = Disable internal pullup for pin RC4

RCPUP3 (bit 3):

- 1 = Enable internal pullup for pin RC3
- 0 = Disable internal pullup for pin RC3

RC_PUP (bit0, 1, 2): These are not used

13.14 RC_WKPU (address 807Dh): RC GPIO Weak Pull-Up Enable Register

This register enables the internal pull-ups for the RC pins. The pull-up is implemented as a weak PMOS transistor from the pin to VDD

	RC_WKPU REGISTER (ADDRESS 807Dh)							
	7(MSB)	6	5	4	3	2	1	0
Name	RC_WKPU7	RC_WKPU6	RC_WKPU5	RC_WKPU4	RC_WKPU3	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R	R	R
Reset	0	0	0	0	0	0	0	0

RCWKPU7 (bit 7):

- 1 = Enable weak internal pullup for pin RC7
- 0 = Disable weak internal pullup for pin RC7

RCWKPU6 (bit 6):

- 1 = Enable weak internal pullup for pin RC6
- 0 = Disable weak internal pullup for pin RC6

RCWKPU5 (bit 5):

- 1 = Enable weak internal pullup for pin RC5
- 0 = Disable weak internal pullup for pin RC5

RCWKPU4 (bit 4):

- 1 = Enable weak internal pullup for pin RC4
- 0 = Disable weak internal pullup for pin RC4

RCWKPU3 (bit 3):

- 1 = Enable weak internal pullup for pin RC3
- 0 = Disable weak internal pullup for pin RC3

RC_WKPU (bit0, 1, 2): These are not used

13.15 RC_THERM (address 80D0h): RC Thermistor Support Control Register

This register enables the 103AT Thermistor support for the RC pins. Only **ONE** input can be enabled with the thermistor support circuit at one time. If more than one bit is set in this register then the highest bit has the higher priority and will be used. This register should be modified between thermistor input reads to enable the additional internal circuitry to the next thermistor input prior to ADC conversion.

	RC_THERM REGISTER (ADDRESS 80D0h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RCPUP7	RCPUP6	RCPUP5	RCPUP4	RCPUP3	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R	R	R
Reset	0	0	0	0	0	0	0	0

RCTHERM7 (bit 7):

- 1 = Enable internal thermistor support for pin RC7 when selected to be measured by the ADC
- 0 = Disable internal thermistor support for pin RC7

RCTHERM6 (bit 6):

- 1 = Enable internal thermistor support for pin RC6 when selected to be measured by the ADC
- 0 = Disable internal thermistor support for pin RC6

RCTHERM5 (bit 5):

- 1 = Enable internal thermistor support for pin RC5 when selected to be measured by the ADC
- 0 = Disable internal thermistor support for pin RC5

RCTHERM4 (bit 4):

- 1 = Enable internal thermistor support for pin RC4 when selected to be measured by the ADC
- 0 = Disable internal thermistor support for pin RC4

RCTHERM3 (bit 3):

- 1 = Enable internal thermistor support for pin RC3 when selected to be measured by the ADC
- 0 = Disable internal thermistor support for pin RC3

RC_THERM (bit0, 1, 2): These are not used

13.16 RB GPIO and Programmable Current Sink Operation

The five channel RB GPIO port can be configured to operate as a digital input, a digital open drain output or a programmable analog current sink. Each pin can be configured independently. The analog current sinks can be used to drive external LED's and eliminate the need for current limiting resistors. The following table describes the operation of the RB/CS GPIO port:

OUTPUT	RBOUT	CSx[1:0]
Not driven (open drain 3-state)	1	X
Digital pull-down	0	00
3mA	0	01
4mA	0	10
5mA	0	11

Note: Care should be taken when configuring and enabling the current sinks to ensure that the maximum power dissipation of the package is not exceeded. This may include reducing the current levels as ambient temperature rises above normal operating levels, for example >65°C.

13.16.1 CS_HIGH (address 807Eh): Current Sink Control Register

This register controls the upper pins of the port.

	CS_HIGH REGISTER (ADDRESS 807Eh)							
	7(MSB)	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	CS4[1]	CS4[0]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CS7[1:0]...CS5[1:0] (bits 7...2): Not Used

CS4[1:0] (bits 1:0): Configures pin RB4/CS4

- 00 = Output is digital open-drain pull-down
- 01 = Output is 3 mA current sink
- 10 = Output is 4 mA current sink
- 11 = Output is 5 mA current sink

13.16.2 CS_LOW (address 807Fh): Current Sink Control Register

This register controls the lower pins of the port.

	CS_LOW REGISTER (ADDRESS 807Fh)							
	7(MSB)	6	5	4	3	2	1	0
Name	CS3[1]	CS3[0]	CS2[1]	CS2[0]	CS1[1]	CS1[0]	CS0[1]	CS0[0]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

CS3[1:0] (bits 7:6): Configures pin RB3/CS3

- 00 = Output is digital open-drain pull-down
- 01 = Output is 3 mA current sink
- 10 = Output is 4 mA current sink
- 11 = Output is 5 mA current sink

CS2[1:0] (bits 5:4): Configures pin RB2/CS2

- 00 = Output is digital open-drain pull-down
- 01 = Output is 3 mA current sink
- 10 = Output is 4 mA current sink
- 11 = Output is 5 mA current sink

CS1[1:0] (bits 3:2): Configures pin RB1/CS1

- 00 = Output is digital open-drain pull-down
- 01 = Output is 3 mA current sink
- 10 = Output is 4 mA current sink
- 11 = Output is 5 mA current sink

CS0[1:0] (bits 1:0): Configures pin RB0/CS0

- 00 = Output is digital open-drain pull-down
- 01 = Output is 3 mA current sink
- 10 = Output is 4 mA current sink
- 11 = Output is 5 mA current sink

14 Control Interrupts and Events

The bq8050 has five data registers (PFLAG, PFLAG2, PIE, PIE2, and PCTL) for interrupt status and control. The internal CPU STAT register controls the servicing of interrupts.

14.1.1 PFLAG (address 8090h): Peripheral Flag Register

This register signals the status of the various interrupt flags.

PFLAG REGISTER (ADDRESS 8090h)								
	7(MSB)	6	5	4	3	2	1	0
Name	SMBF	-	ADF	CCF	TIMF	WKF	-	GPF
Access	R/W	R	R/W	R/W	R/W	R/W	R	R
Reset	0	0	0	0	0	0	0	0

SMBF (bit 7): System management bus interrupt flag. This bit signals the SMBus circuit request for interrupt servicing. A controller interrupt to address vector (3h) is generated if SMBIE=GIE=1 when SMBF=1 (sets the CIN bit in the STAT register).

- 1 = SMBus circuit requests interrupt processing
- 0 = SMBus request did not occur

ADF (bit 5): ADC interrupt flag bit. This bit signals an ADC request for interrupt servicing at the end of a conversion. A controller interrupt to address vector (2h) is generated if DIE=PINE=GIE=1 when ADF=1 (sets the PIN bit in the STAT register).

- 1 = ADC circuit requests interrupt processing
- 0 = ADC request did not occur

CCF (bit 4): CC interrupt flag bit. This bit signals a coulomb counter request for interrupt servicing. A controller interrupt to address vector (2h) is generated if CCIE=PINE=GIE=1 when CCF=1 (sets the PIN bit in the STAT register).

- 1 = CC circuit requests interrupt processing
- 0 = CC request did not occur

TIMF (bit 3): Timer interrupt flag. This bit signals a timer request for interrupt servicing. A controller interrupt to address vector (2h) is generated if TIMIE=PINE=GIE=1 when TIMF=1 (sets the PIN bit in the STAT register).

- 1 = Timer circuit requests interrupt processing once every 7.8125ms (128 times per second)
- 0 = Timer request did not occur

WKF (bit 2): Wake timer flag bit. This bit indicates that a wake timer out has occurred.

- 1 = Wake timer elapsed
- 0 = Wake timer elapse did not occur

GPF (bit 0): General purpose timer flag. This bit enunciates a GP Timer request for interrupt servicing

- 1 = GP Timer circuit requests interrupt processing
- 0 = GP Timer request did not occur

Bits 1 and 6 are not used and will return a 0.

14.1.2 PIE (address 8091h): Peripheral Interrupt Enable Register

This register enables the PIE interrupt from the various registers.

PIE REGISTER (ADDRESS 8091h)								
	7(MSB)	6	5	4	3	2	1	0
Name	SMBIE	-	ADIE	CCIE	TIMIE	WKEVE	-	TMGIE
Access	R/W	R	R/W	R/W	R/W	R/W	R	R
Reset	0	0	0	0	0	0	0	0

SMBIE (bit 7): SMBus interrupt enable. This bit enables the SMBus interrupt flag to interrupt the controller. A controller interrupt to address vector (0003h) is generated if SMBF=GIE=1 when SMBIE=1 (sets the CIN bit in the STAT register).

- 1 = Enable SMBus circuit interrupt requests
- 0 = Disable SMBus circuit interrupt requests

ADIE (bit 5): ADC interrupt enable bit. This bit enables an ADC request for interrupt servicing at the end of a conversion. A controller interrupt to address vector (0002h) is generated if ADF=PINE=GIE=1 when ADIE=1 (sets the PIN bit in the STAT register).

- 1 = Enable ADC interrupt requests
- 0 = Disable ADC interrupt requests

CCIE (bit 4): CC interrupt enable bit. This bit enables a CC request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if CCF=PINE=GIE=1 when CCIE=1 (sets the PIN bit in the STAT register).

- 1 = Enable CC interrupt requests
- 0 = Disable CC interrupt requests

TIMIE (bit 3): Timer interrupt enable. This bit enables a timer request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if TIMF=PINE=GIE=1 when TIMIE=1 (sets the PIN bit in the STAT register).

- 1 = Enables timer interrupt requests
- 0 = Disables timer interrupt requests

WKEVE (bit 2): Wake timer event enable bit. This bit allows the wake timer event (not an interrupt) to restart the controller from the HALT.

- 1 = Enables a wake timer event to restart the controller from HALT
- 0 = Disables the wake timer event from restarting the controller from HALT

TMGIE (bit 0): GP Timer interrupt enable. This bit enables the General purpose timer request for interrupt servicing. A controller interrupt to address vector (0002h) is generated if GPF=PINE=GIE=1 when TMGIE=1 (sets the PIN bit in the STAT register).

- 1 = Enables GP timer interrupt requests
- 0 = Disables GP timer interrupt requests

14.1.3 PCTL (address 8092h): Peripheral External Input Control Register

This register enables control of the polarity of external inputs for interrupts and events.

	PCTL REGISTER (ADDRESS 8092h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	XIN2_EDG	XIN1_EDG	XEV_EDG
Access	R/W	R	R	R	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Reserved (bits 7:3): Do not use.

XIN2_EDG (bit 2): External interrupt (INT2) edge select bit. This bit selects the active edge, positive or negative, for the external interrupt input.

- 1 = The RA7 external interrupt is positive edge triggered.
- 0 = The RA7 external interrupt is negative edge triggered.

XIN1_EDG (bit 1): External interrupt (INT1) edge select bit. This bit selects the active edge, positive or negative, for the external interrupt input.

- 1 = The RA5 external interrupt is positive edge triggered.
- 0 = The RA5 external interrupt is negative edge triggered.

XEV_EDG (bit 0): External event edge select bit. This bit selects the active edge, positive or negative, for the external event input.

- 1 = The RA3 external event is positive edge triggered.
- 0 = The RA3 external event is negative edge triggered.

14.1.4 PFLAG2 (address 8093h): Peripheral Flag Register

This register enables the predefined pin functions.

	PFLAG2 REGISTER (ADDRESS 8093h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	XINT2F	XINT1F	WK_CHG	WK_DSG
Access	R/W	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Reserved (bits 7:4): Do not use.

XINT2F (bit 3) : External Interrupt (INT2) interrupts flag

- 1 = Interrupt received
- 0 = No Interrupt received

XINT1F (bit 2): External Interrupt (INT1) interrupts flag

- 1 = Interrupt received
- 0 = No Interrupt received

WKCHG (bit 1): Charge current wake event

- 1 = The wake function has detected a charge current wake event
- 0 = No event !

WKDSG (bit 0): Discharge current wake event

- 1 = The wake function has detected a discharge current wake event
- 0 = No event occurred



bq8050

14.1.5 PIE2 (address 8094h): Peripheral Interrupt Enable

This register enables interrupts of predefined pin functions.

	PIE2 REGISTER (ADDRESS 8094h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	IWAKE	WKCEVE	WKDEVE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Reserved (bits 7:2): Do not use.

WKCEVE (bit 1): Enable charge current wake event

- 1 = Enable charge current wake
- 0 = Disable charge current wake

WKDEVE (bit 0): Enable discharge current wake event

- 1 = Enable discharge current wake
- 0 = Disable discharge current wake

14.1.6 WKUPCMP (address 80B0h): Wake Up Comparator

This register configures the current wake threshold.

	WKUPCMP REGISTER (ADDRESS 80B0h)							
	7(MSB)	6	5	4	3	2	1	0
Name	RSVD	RSVD	RSVD	RSVD	RSVD	IWAKE	RSNS1	RSNS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Reserved (bits 7:3): Do not use.

IWAKE (bit 2): Wake current select bit. This bit selects the level of battery current that may wake the bq8050 from sleep.

- 1 = 1.0A
- 0 = 0.5A (default)

RSNS1-RSNS0 (bits 1:0): Sense resistor selection bits. These bits are used to enable and select the value of sense resistor used with the bq8050. In conjunction with the IWAKE bit, these will select the sense resistor voltage threshold. WK_CHGF will be set when the sense resistor voltage is determined to be more than the positive Vth(SRP-SRN) threshold and if WKCEVE is set the bq8050 will wake. Conversely, WK_DSGF will be set when the sense resistor voltage is determined to be more negative than the negative Vth(SRP-SRN) threshold and if WKDEVE is set the bq8050 will wake.

RSNS1:RSNS0	RSNS(mΩ)	IWAKE	Vth(SRP-SRN)
00	N/A	0 (+/-0.5mA)	Disabled
00	N/A	1 (+/-1.0mA)	Disabled
01	2.5	0 (+/-0.5mA)	+1.2mV or -1.2mV
01	2.5	1 (+/-1.0mA)	+2.4mV or -2.4mV
10	5	0 (+/-0.5mA)	+2.5mV or -2.5mV
10	5	1 (+/-1.0mA)	+5mV or -5mV
11	10	0 (+/-0.5mA)	+5mV or -5mV
11	10	1 (+/-1.0mA)	+10mV or -10mV

14.2 Customer Test Mode

The bq8050 allows the following inter-connect signals to be monitored via the RB port when in the Customer Test Mode: SDATA, SCLK, XALERT, XRST, and WDI. These are intended for debug purposes only and require external pull-ups. Customer Test Mode is enabled by setting IOCTL2 [CTM_EN]. A reset or clearing IOCTL2 [CTM_EN] will disable this feature.

14.2.1 Customer Test Mode Control Register

CUST_TM_CRTL REGISTER (0x80D1h)							
7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	WDI	SDATA	SCLK	XALERT	XRST

The CUST_TM_CRTL register allows the internal signals to mux to the package pins for observation.

WDI (bit 4): This bit controls if WDI can be observed at RB0

0 = WDI is not observable at RB0 (default)

1 = WDI is observable at RB0

SDATA (bit 3): This bit controls if SDATA can be observed at RB4

0 = SDATA is not observable at RB4 (default)

1 = SDATA is observable at RB4

SCLK (bit 2): This bit controls if SCLK can be observed at RB3

0 = SCLK is not observable at RB3 (default)

1 = SCLK is observable at RB3

XALERT (bit 1): This bit controls if XALERT can be observed at RB2

0 = XALERT is not observable at RB2 (default)

1 = XALERT is observable at RB2

XRST (bit 0): This bit controls if XRST can be observed at RB1

0 = XRST is not observable at RB1 (default)

1 = XRST is observable at RB1

14.3 Internal CPU STAT Register Description

The bq8050 has 16 internal CPU registers, one of these is the STST register. The status register is used in conjunction with several of the bq8050 peripherals and is included for ease of reference.

STAT (address Eh): Internal CPU Status Register

	STAT REGISTER (ADDRESS Eh)							
	7(MSB)	6	5	4	3	2	1	0
Name	PINE	XINE	GIE	PIN	XIN	CIN	XEV	WEV
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	-	0	-	-	-	-

PINE (bit 7): Peripheral interrupt enable bit. This bit enables a controller interrupt when PIN and GIE are asserted.

- 1 = PIN enabled to generate an interrupt if GIE=1
- 0 = PIN inhibited from generating an interrupt

XINE (bit 6): External interrupt enable bit. This bit enables a controller interrupt when XIN and GIE are asserted.

- 1 = XIN enabled to generate an interrupt if GIE=1
- 0 = XIN inhibited from generating an interrupt

GIE (bit 5): Global interrupt enable bit. This bit disables all interrupts when cleared. GIE is automatically cleared when an interrupt service routine is executed to prevent unwanted interrupt nesting.

- 1 = Allows PIN, XIN, and CIN interrupts to be processed by the controller
- 0 = Disables all interrupts

PIN (bit 4): Peripheral interrupt bit (lowest priority). This bit signals a peripheral circuit request for interrupt service.

- 1 = Peripheral circuit interrupt requested
- 0 = No peripheral interrupt service requested

XIN (bit 3): External interrupt bit (medium priority). This bit signals an external interrupt service request that was received via the INT1 or INT2 (RA0 or RA7) pin.

- 1 = External interrupt service requested
- 0 = No external interrupt service requested

CIN (bit 2): Communication interrupt bit (highest priority). This bit signals a communication circuit request for interrupt service.

- 1 = Communication circuit interrupt requested from the HDQ or SMBus
- 0 = No communication interrupt service requested

XEV (bit 1): External event bit. This bit signals that an external wake-timer event occurred via the EV (RA2) pin that can wake the controller from a HALT state.

- 1 = External event occurred
- 0 = External event has not occurred

WEV (bit 0): Wake event bit. This bit signals a wake timer event occurred that can wake the controller from a HALT state.

- 1 = Internal event occurred
- 0 = Internal wake timer event has not occurred

14.4 IFIB Data Storage

The bq8050 contains a memory space that stores various factory calibration data values that can be used by the firmware to enable very accurate voltage, current and temperature measurement accuracy. The values stored in this space are listed below but are detailed in other parts of the specification.

IFIB Offset	Factory Calibration Parameter	Units
0x1f	CC Offset with CAL=1	LSB
0x1e	ADC Offset	LSB
0x1c	VC4 K-Scale Factor ⁽²⁾	
0x1b	VC3 K-Scale Factor ⁽²⁾	
0x1a	VC2 K-Scale Factor ⁽²⁾	
0x19	VC1 K-Scale Factor ⁽²⁾	
0x18	RC_THERM Trim	Ω
0x17	Internal VREF	mV
0x16	VC1 Internal Resistance Delta ⁽³⁾	10 Ω
0x15	VC2 Internal Resistance Delta ⁽³⁾	10 Ω
0x14	VC3 Internal Resistance Delta ⁽³⁾	10 Ω
0x13	VC4 Internal Resistance Delta ⁽³⁾	10 Ω
0x12	RCx Pad Resistance	Ω

15 Hardware AFE Description

Internal to the bq8050 there is a high voltage front end which enables the bq8050 to directly interface to up to 4 series Li-Ion cells and provide dedicated current based protections for the battery.

15.1 Inter-Device Interaction

15.1.1 Device Status

The AFE status can be read through two registers. The AFE:STATUS register provides fault information and the AFE:OUTPUT_STATUS provides output pin status.

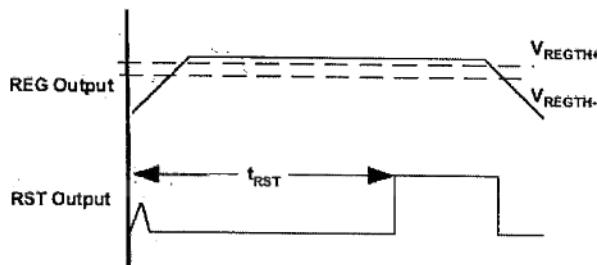
15.1.2 Latch Clear

When a protection fault, the state is latched. To clear the flag, toggle (from 0, set 1, then reset to 0) the LTCLR bit in the AFE:STATE_CONTROL register (bit 7). The OCD, SCC, SCD1, SCD2, FUSE and WDF bits are unlatched by this function if the fault is no longer present. The FETs can now be controlled by programming the AFE:OUTPUT_CONTROL register, and the XALERT output can be cleared by reading the AFE:STATUS register.

Note: The PTC Status is NOT cleared by the Latch Clear function and can only be cleared by a full device reset. (POR)

15.1.3 Power On Reset

The open drain XRST pin is activated by activation of the REG output. This holds the host in reset for the duration of the t_{RST} period, allowing the VREG to stabilize before the host is released from reset. When the regulator power is down, XRST is active below the regulator's minimum operating. Also, when a watchdog fault is detected, the XRST is also activated to ensure a valid reset of the battery management host.



15.1.4 Watchdog Reset

The AGG within the bq8050 provides a 32kHz clock into the AFE device for AFE device operation and protection timing. The AFE device monitors this input to provide some indication that the AGG is operating normally. The AFE can be enabled to turn OFF the FETs and even try to reset the AGG in situations where the 32kHz signal is not received correctly.

When a 32kHz signal is provided to the AFE then the AFE will use this signal for device operation and protection timing purposes. However, if this signal should fail then an oscillator internal to the AFE will start and provide the clock for device operation and protection timing.

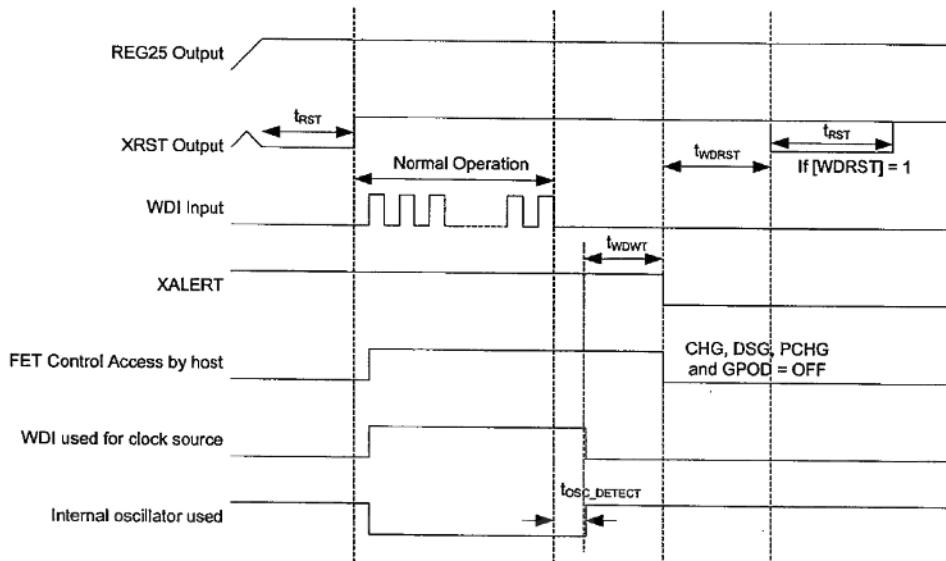
A watchdog timeout is detected when the WDI input does not toggle for more than t_{WDWT} AFTER it has at least toggled once (ie: Watchdog cannot timeout if the WDI never received a signal). The start of the t_{WDWT} is delayed by t_{RST} after a power on reset has occurred. If t_{WDWT} expires then the internal XALERT pin is triggered, the AFE.STATUS [WDF] bit is set, the CHG, DSG and PCHG FETs are turned OFF and the GPOD output is disabled.

Once a t_{osc_detect} period of no activity on WDI is detected then the AFE's internal oscillator begins operating.

If the WDI input does not transition for a further t_{WDRST} then the AFE can be enabled to trigger the internal XRST pin to reset the AGG. This is done by setting AFE.STATE_CONTROL [WDRST] prior to the watchdog fault occurring. The default state of [WDRST] is OFF. When XRST is Active (LOW) then the watchdog is held off and when XRST is released (HIGH) then the watchdog function is reset requiring a pulse of WDI to begin the fault detection.

The watchdog is default enabled but can be disabled by setting AFE.STATE_CONTROL [WDDIS]. If [WDDIS] is set then [WDRST] is ignored.

Once the AFE.STATUS [WDF] flag is set then it can only be cleared by toggling the LTCLR bit in AFE.OUTPUT_CONTROL.



15.1.5 Low Drop Out Regulators

The inputs for this regulator can be derived from the VCC or BAT terminals. The output (REG33) is typically 3.3 V with the minimum output capacitance for stable operation of $1\mu F$ and is also internally current limited. During normal operation, the regulator limits output current to typically 50 mA. Until the internal regulator circuit is correctly powered, the DSG and CHG FET drives are low (FETs = OFF).

The REG33 LDO powers the REG25 (2.5V) LDO which powers the AGG section of bq8050 and also requires a $1\mu F$ external capacitor for operational stability. The REG25 output is limited to 40mA.

15.1.6 Initialization

From a shutdown situation, the bq8050 requires a voltage greater than start-up voltage ($V_{STARTUP}$) applied to the PACK pin to enable its integrated regulator. Once the REG33 output is stable, the power source of the regulator is switched to BAT, PACK or VCC.

If a voltage at PACK is lower than $V_{STARTUP}$ the bq8050 will not startup.

After the regulator has started, it then continues to operate through the VCC or BAT inputs. If the VCC or BAT input is below the minimum operating range, then the bq8050 will not operate if the supply to the PACK input is removed. If the voltage at REG33 falls below the POR threshold, the internal circuit turns off the FETs and disables all controllable functions. The initial state of the FETs is low (OFF).

If PMS is bonded HIGH to PACK (bq8050A) then the CHG FET is default ON at initialization, if PMS is bonded LOW (bq8050) then the CHG FET is default OFF at initialization. The PMS bond option is reflected in the AFE:DEVICE_CONFIG [PMS].

If the AFE re-initializes through a reset condition then the XRST pin is driven low resetting the AGG.

15.2 N-Channel High Side Charge (CHG) and Discharge(DSG) FET Drive

The bq8050 controls 2 external N-CH MOSFETs in a back-to-back configuration for battery protection. The charge (CHG) and discharge (DSG) FETs are automatically turned OFF as a result of appropriate safety controls and can also be turned OFF via command control. When the CHG FET drive is turned off an internal circuit is enabled to discharge the FET drive charge pump. This enables the CHG pin to fall to GND when an external fuse is blown.

The bq8050 can be enabled to auto recover from current based-faults (OCD, SCD1 and SCD2) but can ONLY turn the CHG and DSG FETs ON via command control when the protection circuit allows. The CHG drive FET can be powered by BAT and the DSG FET can be powered by PACK. When the bq8050 is powered down the NCH FET drivers power down also causing the FETs to turn off.

15.3 Pre-Charge and Zero-Volt Charging Support

The bq8050 provide the capability to provide a current limited charging path typically used for low battery voltage or low temperature charging. The pre-charge (PCHG) FET connects to an external pre-charge load resistor via the PCR pin through the PCHGIN input. The internal PCHG FET can be controlled via OUTPUT_CONTROL[PCHG].

To ensure normal operation within the power dissipation limits of the package the calculation of the external resistance should be calculated per the following equation:

$$R_{PCR} = \frac{Pd}{I_{PRECHG(MAX)}^2}$$

Where:

R_{PCR} = External resistance value connected to PCR pin

Pd = maximum power dissipation of the package

$I_{PRECHG(MAX)}^2$ = Maximum specified current for given cell configuration

Note: Care should be taken to ensure maximum power dissipation ratings of the package are not exceeded when the PCHG FET is enabled.

If a higher current is the required then the GPOD pin can be used with an external FET and external Resistor. In this instance no connection to PCHGIN or PCR is required. The state of GPOD output can be controlled via AFE.OUTPUT_CONTROL[GPOD].

To support ultra low battery voltage, or zero-volt, charging the bq8050 can be configured to enable the CHG FET to be OFF (PMS=0) or ON (PMS=1) when a charger is connected. The PMS bond option is reflected in AFE:OUTPUT_STATUS[PMS]. When the device is below its operating voltage then the PMS pin status is used to configure the CHG FET state, so the AFE register bit is ignored in this state where the register is in an unknown state. When the device reaches normal operating voltage then the register bit is used only if the PMS bond option is HIGH. Also once the bq8050 input voltage has reached the

minimum operating level then the zero-volt charging circuit can be turned OFF via OUTPUT_CONTROL [PMS_CHG].

15.4 Thermal Protection Using PTC

The bq8050 offers the ability to drive the FUSE output when the Positive Temperature Coefficient Thermistor (PTC) input reaches a fixed threshold for a fixed period of time. A positive temperature coefficient thermistor should be connected from Vss to PTC. This feature is available during SHUTDOWN.

When the PTC input rises above V_{PTC_REF} for a period longer than t_{PTC} then the FUSE output is driven high and AFE.STATUS[PTC] is set. [PTC] is only reset through a full device reset and cannot be cleared through the 'latch clear' function. When not used the PTC input should be tied to VSS via a resistor although this is not required for normal operation.

Note: If VPTC rises above 7.5V then the current sourced by the PTC pin will increase by ~100uA/V.

15.5 Thermal Protection of bq8050

The bq8050 contains two integrated thermal shutdown circuits. The first is located at the integrated pre-charge FET and has a threshold of T_{MAX1} . When triggered, the V_{GS} of the current through the PCHG FET is restricted in proportion to the excessive temperature and eventually turning OFF the FET. The second is located on the integrated 3.3V regulator and has a threshold of T_{MAX2} . When triggered, the REG33 regulator will reduce the maximum output load current in proportion to the excessive temperature eventually turning off the regulator output. Both of the thermal shutdown circuits have a hysteresis of -10°C before they will begin recovering.

15.6 Fuse Control via Register

The bq8050 FUSE output can be enabled through setting AFE.STATE_CONTROL[FUSEA] AND AFE.OUTPUT_CONTROL[FUSEB].

15.7 2-, 3-, or 4-Cell Configuration

In a 2-cell configuration, VC1 is shorted to VC2 and VC3. In a 3-cell configuration, VC1 is shorted to VC2.

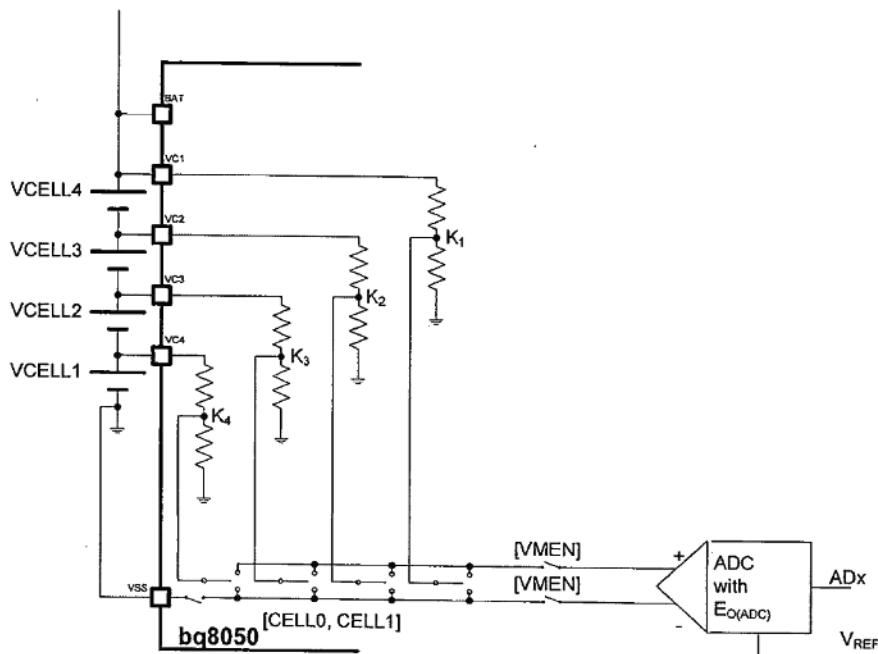
15.8 Cell Connection

The cells should be connected with VC4-VSS first then VC3-VC4 then VC2-VC3 if it exists then VC1-VC2 if it exists then BAT.

It is advised that the device F/W verify the voltage at VCx and BAT input measurement periodically to establish that the VCx and BAT pin are correctly connected as this could cause incorrect voltage measurements although if BAT is not connected then the charge pump for the DSG FET cannot be turned ON.

15.9 Cell Voltage Translation

The internal circuit uses a proprietary passive technique to condition each voltage input for processing by the integrated ADC with maximum precision. For the VCx inputs there is ~1MΩ total resistance to VSS when enabled and for the PACK and BAT inputs there is ~800kΩ total resistance to VSS when enabled. The current used by this circuit is <10µA when enabled.



15.9.1 Configuring the High Voltage Translation Circuit

The high voltage translation circuit is communicated with via an I²C-like interface using the RA Port, specifically RA1 (SCLK) and RA2 (SDATA). Using the I²C-like interface the high voltage interface is configured to present the selected nodal input to the required ADC input channel. Selecting the correct output is achieved through the FUNCTION_CONTROL [0x04] and CEL_SEL [0x05] registers. Configuring which VCx input is to be measured requires the CELL1:0 bits in CEL_SEL[0x05] to be configured appropriately.

VCx Input	CELL1	CELL0
VC1:VC2	1	1
VC2:VC3	1	0
VC3:VC4	0	1
VC4:VSS	0	0

Note: CEL_SEL [CAL] must be 0 for this feature to work correctly.

To enable the high voltage translation output the FUNCTION_CONTROL [VMEN] should also be set. If BAT is set in the FUNCTION_CONTROL register then the CELL1:0 selection is ignored and the differential voltage between VC1:VSS is multiplied by 0.049 and presented to the high voltage translations circuit output. Also, if PACK is set in the FUNCTION_CONTROL register then the CELL1:0 selection and BAT bit state is ignored and the differential voltage between PACK:VSS is multiplied by 0.049 and presented to the high voltage translations circuit output. The priority of the VMEN output control bits is as follows:

Pack	Bat	Input to the ADC
0	0	Per FUNCTION_CONTROL[CELL0,CELL1]
0	1	BAT
1	0	PACK
1	1	BAT

During the time when VMEN is enabled and voltages are being measured any cell balancing FETs that are on will cause an error in the measurement proportional to the cell balancing current and the series resistance connected to the IC. It is recommended to allow 9 μ s ($t_{SETTLE:MAX}$) between changing between the CELL1:0 configurations (assuming VMEN remains 1) and using the ADC to measure the high voltage translation circuit. The value for t_{SETTLE} is derived from simulation data and it cannot be directly characterized as it is an internal signal. The value covers the full operating temperature range of the device.

15.10 Cell Voltage Translation Calibration

The VCx input voltage translation gain (K) for each VCx input, BAT and PACK is provided in the Instruction Flash Information Block. To calibrate the K-factor values the following equations are used:

To calculate K4 use:

$$K_4 = \frac{VC_4}{AD_4}$$

To calculate K3, 2, and K1 use:

$$K_x = \frac{VC_x}{AD_x + \frac{VC_{x+1}}{K_{x+1}}}$$

The K factor must be calculated AFTER ADC offset and Gain has been calculated so it can be removed from the K-Factor value and the K-Factors should be measured in the following order: K4, then K3, then K2 and finally K1. Otherwise the K factors will be wrong.

To calculate voltage from the ADC data the following equations should be used:

For VC4 use:

$$VC_4 = K_4 AD_4$$

For VC3, VC2 and VC1 use

$$VC_x = K_x AD_x + \frac{VC_{x+1}}{K_{x+1}}$$

15.11 Cell Balance Control

The cell balance control allows a small bypass path to be controlled for any one series element. The purpose of this bypass path is to reduce the current into any one cell during charging to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes control the bypass current value. Individual series element selection is made using bits 4 through 7 of AFE:CELL_SEL register. Series input resistors between 100 Ω and 1k Ω are recommended for effective cell balancing.

15.12 Reverse Connection Protection

The bq8050 can withstand reverse connection of PACK+ and PACK- to a charger with no miss operation although a resistor in series between the PACK+ node of the battery and the PACK pin is required. This value should be ~1k Ω for stable operation.

15.13 Over Current Protection

The over current (OCD) detection is used to detect abnormal currents in the discharge direction. This feature is used to protect the pass FETs, cells, and any other inline components from excessive

discharge current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state.

The over current sense voltage is set in the OCDV register, and delay time is set in the OCDD register. The thresholds can be individually programmed from 50 mV to 200 mV in 10-mV steps with the default being 50 mV when AFE:STATE_CTL[RSNS] = 0. When AFE:STATE_CTL[RSNS] = 1 then the options are from 25mV to 100mV in 5mV steps.

15.14 Short Circuit Protection

The short current circuit in charge (SCC) and short circuit in discharge (SCD1, SCD2) detections are used to detect severe abnormal current in the charge and discharge directions, respectively. This safety feature is used to protect the pass FETs, cells, and any other inline components from excessive current conditions.

The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state. The short circuit in charge threshold and delay time are set in the AFE:SCC register and the short circuit in discharge (SCD1 and SCD2) delay times are set in AFE:SCD1 and AFE:SCD2 registers respectively.

The short-circuit in charge thresholds can be programmed from -100mV to -300mV in -50mV steps when AFE:STATE_CTL[RSNS] = 0. When AFE: STATE _CTL[RSNS] = 1 the options are -50mV to -225mV in 25mV steps.

The 2 short circuit in discharge thresholds can be programmed from 100 mV to 450 mV in 50-mV steps when AFE: STATE _CTL[RSNS] = 0. When AFE: STATE _CTL[RSNS] = 1 the options are 50mV to 225mV in 25mV steps.

15.15 Over Current and Short Circuit Protection Delay

For the Over Current and Short Circuit protection features there is a t_{DETECT} period between the fault being presented to the SRP/SRN pins to the beginning of the delay time.

The over current delay allows the system to momentarily accept a high current condition without disconnecting the supply to the load. The delay time can be increased via the AFE:OCD register which can be programmed for a range of 1 ms to 31 ms with 2-ms steps.

The short circuit in charge and short circuit in discharge delays (default = 0 μ s) are programmable in the AFE:SCC and AFE:SCD1 registers, respectively. These registers can be programmed from 0 μ s to 915 μ s with 61- μ s steps. The SCD2 timings range from 0 μ s to 457 μ s with ~30- μ s steps.

The time between a fault signal presented to SRP/SRN and the CHG or DSG pin changing state is $t_{DETECT} + t_{DELAY}$, where t_{DELAY} is the programmable fault delay.

The accuracy of the delay timing is based on the WDI input accuracy (f_{LFO}). However, if the WDI input is not used then the accuracy will be based on the backup oscillator which has an error up to t_{ACC} .

15.16 Over Current and Short Circuit Protection Response

When an over current, short circuit in charge, or short circuit in discharge fault is detected, the FETs are turned off. The AFE:STATUS register reports the details of over current, short circuit in charge or short-circuit discharge.

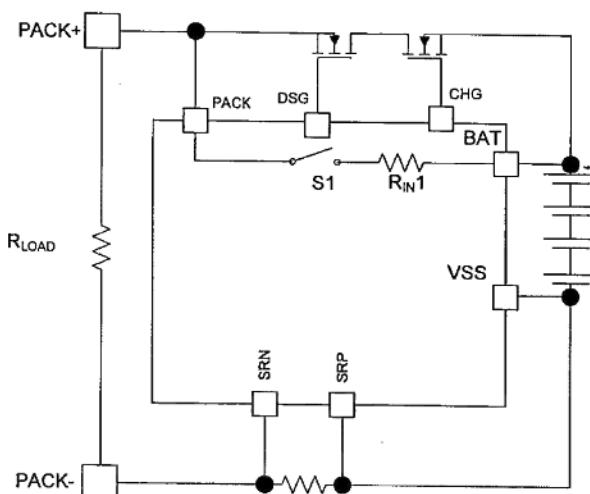
The respective STATUS bits are set to 1 and the XALERT output is triggered. This condition is latched until the AFE:OUTPUT_CONTROL[LTCLR] is set and then reset AND the fault condition has been removed.

15.17 Over Current and Short Circuit Protection Recovery

There is no autonomous recovery for the Over Current and Short Circuit protection features. This condition is latched until the OUTPUT_CONTROL (b0) [LTCLR] is set and then reset. If a FET is turned on after resetting [LTCLR] and the error condition is still present on the system, then the device again enters the protection response state.

Once the over current in discharge or either short circuit in discharge has been detected a removal of the load detection circuit can be enabled (S1 turned ON) through host control by connecting a resistive (R_{IN1}) path between PACK and BAT. Where the value of R_{IN1} can be configured via FUNCTION_CONTROL[RV1:RV0]. S1 is not controlled automatically and it operation is not restricted by fault condition status.

The PACK terminal voltage falls to approx VSS because the external load resistance is very low compared with R_{IN1} in this condition. When the load is removed, the PACK voltage increases because R_{IN1} is now connected to BAT. The bq8050 AGG can monitor the state of the PACK voltage as part of the firmware controlled current fault recovery mechanism and via AFE:FUNCTION_CTL [SC_REC] enable or disable (default) S1. This feature does NOT automatically recover the FETs when the load is removed.



15.18 Customer Test Mode Support

When STATE_CONTROL[CTM_ENA] is set and OUTPUT_CONTROL[CTM_ENB] transitions from high to low then the VCELLP output is presented on the PTC pin and VCELLM output is presented on the GPOD pin. This is independent of the AGG.

15.19 Internal Device Communication

The two wire inter-device communications provides read and write access to the bq8050 AFE data area. The data is clocked via separate data (SDATA – open drain type) and clock (SCLK – push pull type)) pins. The bq8050 AFE data space acts as a dedicated slave device with no address and does not generate clock pulses.

The data location address is 7 bits

The ba8050 AFE data space does NOT have the following functions compatible with the I²C specification:

- Always regarded as a slave.
 - Does not support the Address Auto Increment, which allows continuous reading and writing.

16 Hardware AFE Configuration and Control Interaction

16.1 Hardware AFE Registers

NAME	ADDR	TYPE	DESCRIPTION
'RAM			
STATUS	0x00	R	Status register
STATE_CONTROL	0x01	R/W	State control
OUTPUT_CONTROL	0x02	R/W	Output pin control from system host and external pin status
OUTPUT_STATUS	0x03	R	Output pin status
FUNCTION_CONTROL	0x04	R/W	Function control
CELL_SEL	0x05	R/W	Battery cell select for cell translation and balance bypass and select mode for calibration
OCDV	0x06	R/W	Overload voltage threshold
OCDD	0x07	R/W	Overload delay time
SCC	0x08	R/W	Short circuit in charge current threshold voltage and delay
SCD1	0x09	R/W	First Short circuit in discharge current threshold voltage and delay
SCD2	0x0a	R/W	Second Short circuit in discharge current threshold voltage and delay

16.2 Register Bit Map

NAME	ADDR	TYPE	B7	B6	B5	B4	B3	B2	B1	B0
STATUS	0x00	R	FUSE	PTC	-	WDF	OCD	SCC	SCD2	SCD1
STATE_	0x01	R/W	FUSEA	CTM_ENA	SCDDx2	RSNS	WDRST	WDDIS	SHUT-DOWN	-
CONTROL_	0x02	R/W	FUSEB	CTM_ENB	PMS_CHG	GPOD	PCHG	CHG	DSG	LTCLR
OUTPUT_	0x03	R	PMS	CTM	PMS_CHG	GPOD	PCHG	CHG	DSG	-
FUNCTION_	0x04	R/W	-	-	RV1	RV0	SCREC	BAT	PACK	VMEN
CONTROL_	0x05	R/W	CB3	CB2	CB1	CB0	-	CAL	CELL1	CELL0
OCDV	0x06	R/W	-	-	-	OCDV4	OCDV3	OCDV2	OCDV1	OCDV0
OCDD	0x07	R/W	-	-	-	-	OCD3	OCD2	OCD1	OCD0
SCC	0x08	R/W	SCCD3	SCCD2	SCCD1	SCCD0	SCCV3	SCCV2	SCCV1	SCCV0
SCD1	0x09	R/W	SCD1D3	SCD1D2	SCD1D1	SCD1D0	-	SCD1V2	SCD1V1	SCD1V0
SCD2	0x0a	R/W	SCD2D3	SCD2D2	SCD2D1	SCD2D0	-	SCD2V2	SCD2V1	SCD2V0

16.3 STATUS: Status register

STATUS REGISTER (0x00)							
7	6	5	4	3	2	1	0
FUSE	PTC	-	WDF	OCD	SCC	SCD2	SCD1

The STATUS register provides information about the current state of the bq8050.

STATUS b0 (SCD1): This bit indicates a short circuit in discharge condition.

0 = Voltage below the short circuit in discharge threshold (default).

1 = Voltage greater than or equal to the short circuit in discharge threshold.

STATUS b1 (SCD2): This bit indicates a short circuit in discharge 2 condition.

0 = Voltage below the short circuit in discharge 2 threshold (default).

1 = Voltage greater than or equal to the short circuit in discharge 2 threshold.

STATUS b2 (SCC): This bit indicates a short circuit in charge condition in the charge direction.

0 = Voltage below the short circuit in charge threshold (default).

1 = Voltage greater than or equal to the short circuit in charge threshold.

STATUS b3 (OCD): This bit indicates an over current in discharge condition.

0 = Voltage less than or equal to the over current in discharge threshold (default).

1 = Voltage greater than over current in discharge threshold.

STATUS b4 (WDF): This bit indicates a watchdog fault condition has occurred.

0 = 32-kHz oscillation is normal (default).

1 = 32-kHz oscillation has stopped and the watchdog has timed out.

STATUS b6 (PTC): This bit indicates the PTC threshold has been reached for a period of t_{PTC} .

0 = PTC input is below the V_{PTC} threshold and not yet reached the V_{PTC} threshold (default).

1 = PTC input has reached the V_{PTC} threshold for a period of t_{PTC}

STATUS b7 (FUSE): This bit indicates the FUSE pin is active (high). This could be caused by external stimulus including the PTC function as well as under bq8050 control

0 = FUSE output is low (default).

1 = FUSE output is high

16.4 STATE_CONTROL : State control register

STATE_CONTROL REGISTER (0x01)							
7	6	5	4	3	2	1	0
FUSEA	CTM_ENA	SCDDx2	RSNS	WDRST	WDDIS	SHUTDOWN	-

The STATE_CONTROL register controls some of the outputs of the bq8050 and can be used to clear certain states.

STATE_CONTROL b1 (SHUTDOWN): This bit is used to enter the shutdown power mode when Pack supply voltage is not applied.

0 = bq8050 in normal mode (default)

1 = bq8050 enters shutdown mode when pack voltage is removed.

STATE_CONTROL b2 (WDDIS): This bit is used to enable the watchdog timer.

0 = Watchdog timer enabled (default)

1 = Watchdog timer disabled

STATE_CONTROL b3 (WDRST): This bit is used to enable the reset for internal device interaction, when watchdog timer is active.

0 = Reset output is disabled, when watchdog timer is active (default).

1 = Reset output is enabled, when watchdog timer is active.

STATE_CONTROL b4 (RSNS): This bit sets the OCD, SCC, SCD1 and SCD2 thresholds into a range suitable for a low sense resistor value by dividing the OCDV, SCCV, SCD1V and SCD2V selected voltage thresholds by 2.

0 = Current protection voltage threshold as programmed (default)

1 = Current protection voltage thresholds divided by 2 as programmed

STATE_CONTROL b5 (SCDDx2): This bit doubles the SCD1 and SCD2 delay periods

0 = Short Circuit current protection delay is as programmed (default)

1 = Short Circuit current protection delay is twice that programmed

STATE_CONTROL b6 (CTM_ENA): This bit is used to enable and disable the customer test mode (CTM).

0 = CTM is disabled (default).

1 = CTM is enabled IF CTM_ENB transitions from High to Low when CTM_ENA is set

STATE_CONTROL b7 (FUSEA): This bit is used as part of the control sequence to enable the FUSE output.

0 = FUSE output is controlled automatically (default).

1 = FUSE output is enabled IF FUSEB transitions from High to Low when FUSEA is set.

16.5 OUTPUT_CONTROL : Output control register

OUTPUT_CONTROL REGISTER (0x02)							
7	6	5	4	3	2	1	0
FUSEB	CTM_ENB	PMS_CHG	GPOD	PCHG	CHG	DSG	LTCLR

The OUTPUT_CONTROL register controls some of the outputs of the bq8050 and can show the state of the external pin corresponding to the control. **Note:** If a fault exists then the output control register bits is ignored.

OUTPUT_CONTROL b0 (LTCLR): When a fault is latched, this bit releases the fault latch when toggled from 0 to 1 and back to 0 (default =0).

0 = (default)

0->1 ->0 clears the fault latches, allowing STATUS to be cleared on its next read.

OUTPUT_CONTROL b1 (DSG): This bit controls the external discharge FET.

0 = Discharge FET is turned off (default).

1 = Discharge FET is on

OUTPUT_CONTROL b2 (CHG): This bit controls the external charge FET.

0 = Charge FET is off (default).

1 = Charge FET is on

OUTPUT_CONTROL b3 (PCHG): This bit enables or disables the precharge function.

0 = PCHG FET is off (default).

1 = PCHG FET is on

OUTPUT_CONTROL b4 (GPOD): This bit enables or disables the GPOD output.

0 = GPOD is high impedance and is controlled by the system host if (default).

1 = GPOD output is active (GND).

OUTPUT_CONTROL b5 (PMS_CHG): This bit enables the CHG output for 0-V charge.

0 = Disables ZVCHG control of CHG FET and turns CHG FET off.

1 = Enables ZVCHG control of CHG FET and turns CHG FET on. (Default)

OUTPUT_CONTROL b6 (CTM_ENB): This bit is used to enable and disable the customer test mode (CTM).

0 = CTM is disabled (default).

1 = CTM is enabled IF CTM_ENA also set when CTM_ENB transitions from High to Low

OUTPUT_CONTROL b7 (FUSEB): This bit is used as part of the control sequence to enable the FUSE output.

0 = FUSE output is controlled automatically (default).

1 = FUSE output is enabled IF FUSEA also set when FUSE B transitions from High to Low

16.6 OUTPUT_STATUS : Output status register

OUTPUT_STATUS REGISTER (0x03)							
7	6	5	4	3	2	1	0
PMS	CTM	PMS_CHG	GPOD	PCHG	CHG	DSG	-

The OUTPUT_STATUS register provides the status of some of the outputs of the bq8050.

OUTPUT_STATUS b1 (DSG): This bit reports the external discharge FET state

- 0 = Discharge FET is off (default)
- 1 = Discharge FET is on

OUTPUT_STATUS b2 (CHG): This bit reports the external charge FET state

- 0 = Charge FET is off (default)
- 1 = Charge FET is on

OUTPUT_STATUS b3 (PCHG): This bit reports the precharge FET state

- 0 = PCHG FET is off (default)
- 1 = PCHG FET is on

OUTPUT_STATUS b4 (GPOD): This bit reports the GPOD output state

- 0 = GPOD is high impedance (default)
- 1 = GPOD output is active (GND)

OUTPUT_STATUS b5 (PMS_CHG): This bit reports the ZVCHG control status

- 0 = ZVCHG control is OFF (default)
- 1 = ZVCHG control is ON

OUTPUT_STATUS b6 (CTM): This bit reports the Customer Test Mode status

- 0 = bq8050 AFE in Normal mode (default)
- 1 = bq8050 AFE in Customer Test Mode

OUTPUT_STATUS b7 (PMS): This bit reflects the bond out option of the PMS pin which enables the CHG output for 0-V charge.

- 0 = CHG FET is off at initialization (default)
- 1 = CHG FET is on at initialization

OUTPUT_STATUS b0 (0): This bit is not used

16.7 FUNCTION_CONTROL : Function control register

FUNCTION_CTL REGISTER (0x04)							
7	6	5	4	3	2	1	0
-	-	RV1	RV0	SC_REC	BAT	PACK	VMEN

The FUNCTION_CONTROL register enables and disables features of the bq8050.

FUNCTION_CONTROL b0 (VMEN): This bit enables or disables the cell and battery high voltage translation function.

- 0 = Disable high voltage translation (default). Internal CELL node is pulled down to GND level.
- 1 = Enable voltage translation.

FUNCTION_CONTROL b1 (PACK): This bit is used to translate the PACK input to the internal CELL node when VMEN = 1. The PACK input voltage is divided by 20 and is presented on the CELL pin regardless of the CELL_SEL register settings.

- 0 = CELL_SEL (b0, b1) settings determine CELL output when VMEN = 1 (default).
- 1 = PACK input translated to CELL output regardless of CELL_SEL (b0, b1) selection when VMEN=1

FUNCTION_CTL b2 (BAT): This bit is used to translate the VC1 input to the internal CELL node when VMEN=1. The VC1 input voltage is divided by 20 and is presented on CELL regardless of the CELL_SEL register settings.

- 0 = CELL_SEL (b0, b1) settings determine CELL output when VMEN = 1 (default).
- 1 = BAT input translated to CELL+, CELL- output regardless of CELL_SEL (b0, b1) selection when VMEN = 1. This bit priority is higher than PACK(b1).

FUNCTION_CONTROL b3 (SC_REC): This bit enables or disables the short circuit recovery detection circuit. This bit can only be set when OCD, SCD1 or SDC2 faults have been detected.

- 0 = Disable SC Recovery detection circuit (default)
- 1 = Enable SC Recovery detection circuit

FUNCTION_CONTROL b4...b5 (RV0...RV1): These bit set the short circuit recovery detection circuit resistance value.

RV1	RV0	RIN1 Value
0	0	6.5k ⁽¹⁾
0	1	13k
1	0	26k
1	1	52k

1 = default

FUNCTION_CONTROL b7, b6 (7, 6): These bits are not used

16.8 CELL_SEL : Cell select register

CELL_SEL REGISTER (0x05)							
7	6	5	4	3	2	1	0
CB3	CB2	CB1	CB0	-	CAL	CELL1	CELL0

This register determines cell selection for voltage measurement and translation, cell balancing, and the operational mode of the cell voltage translation.

CELL_SEL b0-b1 (CELL0–CELL1): These two bits select the series cell for voltage measurement translation.

CELL1	CELL0	SELECTED CELL
0	0	VC4-VSS, Bottom series element (default)
0	1	VC4-VC3, Second lowest series element
1	0	VC3-VC2, Second highest series element
1	1	VC1-VC2, Top series element

CELL_SEL b2 (CAL): This bit enables the Offset presented on CELL+/CELL- pins when VMEN is set.

- 0 = Cell translation for selected cell (default)
- 1 = Cell translation offset for selected cell

CELL_SEL b3 (-): This bit is not used.

CELL_SEL b4-b7 (CB0 – CB3): These 4 bits select the series cell for cell balance bypass path.

CELL_SEL b4 (CB0): This bit enables or disables the bottom series cell balance charge bypass path.

- 0 = Disable bottom series cell balance charge bypass path (default)
- 1 = Enable bottom series cell balance charge bypass path

CELL_SEL b5 (CB1): This bit enables or disables the second lowest series cell balance charge bypass path.

- 0 = Disable series cell balance charge bypass path (default)
- 1 = Enable series cell balance charge bypass path

CELL_SEL b6 (CB2): This bit enables or disables the second highest series cell balance charge bypass path.

- 0 = Disable series cell balance charge bypass path (default)
- 1 = Enable series cell balance charge bypass path

CELL_SEL b7 (CB3): This bit enables or disables the highest series cell balance charge bypass path.

- 0 = Disable series cell balance charge bypass path (default)
- 1 = Enable series cell balance charge bypass path

16.9 OCDV: Over Current in Discharge Voltage threshold register

OCDV REGISTER (0x06)							
7	6	5	4	3	2	1	0
-	-	-	-	OCDV3	OCDV2	OCDV1	OCDV0

OCDV (b3-b0): These four bits select the value of the over current in discharge threshold with a default of 0000.

OCDV (b7-b4): Not Used

When STATE_CTL[RSNS] = 0 these settings are available

OCDV (b3-b0) configuration bits with corresponding voltage threshold(1)			
0x00	0.050 V	0x08	0.130 V
0x01	0.060 V	0x09	0.140 V
0x02	0.070 V	0x0a	0.150 V
0x03	0.080 V	0x0b	0.160 V
0x04	0.090 V	0x0c	0.170 V
0x05	0.100 V	0x0d	0.180 V
0x06	0.110 V	0x0e	0.190 V
0x07	0.120 V	0x0f	0.200 V

When STATE_CTL[RSNS] = 1 these settings are available

OCDV (b3-b0) configuration bits with corresponding voltage threshold(1)			
0x00	0.025 V	0x08	0.065 V
0x01	0.030 V	0x09	0.070 V
0x02	0.035 V	0x0a	0.075 V
0x03	0.040 V	0x0b	0.080 V
0x04	0.045 V	0x0c	0.085 V
0x05	0.050 V	0x0d	0.090 V
0x06	0.055 V	0x0e	0.095 V
0x07	0.060 V	0x0f	0.100 V

16.10 OCDD: Over Current in Discharge Delay time configuration register

OCDD REGISTER (0x07)							
7	6	5	4	3	2	1	0
-	-	-	-	OCDD3	OCDD2	OCDD1	OCDD0

OCDD(b3-b0): These four bits select the value of the delay time for overload with a default of 0000.

Setting	Time	Setting	Time	Setting	Time	Setting	Time
0x00	1 ms	0x04	9 ms	0x08	17 ms	0x0c	25 ms
0x01	3 ms	0x05	11 ms	0x09	19 ms	0x0d	27 ms
0x02	5 ms	0x06	13 ms	0x0a	21 ms	0x0e	29 ms
0x03	7 ms	0x07	15 ms	0x0b	23 ms	0x0f	31 ms

OCDD (b7-4): Not used

16.11 SCC : Short Circuit In Charge configuration register

SCC REGISTER (0x08)							
7	6	5	4	3	2	1	0
SCCD3	SCCD2	SCCD1	SCCD0	-	SCCV2	SCCV1	SCCV0

This register selects the short circuit in charge voltage threshold and delay.

SCCV (b2-b0): These lower nibble bits select the value of the short circuit in charge voltage threshold with 0000 as the default.(1)

When STATE_CTL[RSNS] = 0 these settings are available

Setting	Threshold	Setting	Threshold
0x00	-0.100 V	0x04	-0.300 V
0x01	-0.150 V	0x05	N/A
0x02	-0.200 V	0x06	N/A
0x03	-0.250 V	0x07	N/A

When STATE_CTL[RSNS] = 1 these settings are available

Setting	Threshold	Setting	Threshold
0x00	-0.050 V	0x04	-0.150 V
0x01	-0.075 V	0x05	-0.175 V
0x02	-0.100 V	0x06	-0.200 V
0x03	-0.125 V	0x07	-0.225 V

SCCD (b7-b4): These upper nibble bits select the value of the short circuit in charge delay time. Exceeding the short circuit in charge voltage threshold for longer than this period turns off the CHG and DSG outputs. 0000 is the default.

Setting	Time	Setting	Time	Setting	Time	Setting	Time
0x00	0 µs	0x04	244 µs	0x08	488 µs	0x0c	732 µs
0x01	61 µs	0x05	305 µs	0x09	549 µs	0x0d	793 µs
0x02	122 µs	0x06	366 µs	0x0a	610 µs	0x0e	854 µs
0x03	183 µs	0x07	427 µs	0x0b	671 µs	0x0f	915 µs

SCC (b3): Not used

16.12 SCD1 : First Short Circuit In Discharge configuration register

SCD REGISTER (0x09)							
7	6	5	4	3	2	1	0
SCD1D3	SCD1D2	SCD1D1	SCD1D0	-	SCD1V2	SCD1V1	SCD1V0

This register selects the short circuit in discharge voltage threshold and delay.

SCD1V(b2-b0) : These lower nibble bits select the value of the short circuit in discharge voltage threshold with 0000 as the default.(1)

When STATE_CTL[RSNS] = 0 these settings are available

Setting	Threshold	Setting	Threshold
0x00	0.100 V	0x04	0.300 V
0x01	0.150 V	0x05	0.350 V
0x02	0.200 V	0x06	0.400 V
0x03	0.250 V	0x07	0.450 V

When STATE_CTL[RSNS] = 1 these settings are available

Setting	Threshold	Setting	Threshold
0x00	0.050 V	0x04	0.150 V
0x01	0.075 V	0x05	0.175 V
0x02	0.100 V	0x06	0.200 V
0x03	0.125 V	0x07	0.225 V

SCD1D (b7-b4): These upper nibble bits select the value of the short circuit in charge delay time. Exceeding the Short Circuit in charge voltage threshold for longer than this period will turn off the CHG and DSG outputs. 0000 is the default. . If STATE_CNTL[SCDDx2] is set then the delay time is double of that programmed in this register.

Setting	Time	Setting	Time	Setting	Time	Setting	Time
0x00	0 μ s	0x04	244 μ s	0x08	488 μ s	0x0c	732 μ s
0x01	61 μ s	0x05	305 μ s	0x09	549 μ s	0x0d	793 μ s
0x02	122 μ s	0x06	366 μ s	0x0a	610 μ s	0x0e	854 μ s
0x03	183 μ s	0x07	427 μ s	0x0b	671 μ s	0x0f	915 μ s

SCD1 (b3): Not used

16.13 SCD2 : Short Circuit In Discharge 2 configuration register

SCD2 REGISTER (0x0a)							
7	6	5	4	3	2	1	0
SCD2D3	SCD2D2	SCD2D1	SCD2D0	-	SCD2V2	SCD2V1	SCD2V0

This register selects the short circuit in discharge voltage threshold and delay.

SCD2V(b2-b0) : These lower nibble bits select the value of the short circuit in discharge voltage threshold with 0000 as the default.(1)

When STATE_CTL[RSNS] = 0 these settings are available

Setting	Threshold	Setting	Threshold
0x00	0.100 V	0x04	0.300 V
0x01	0.150 V	0x05	0.350 V
0x02	0.200 V	0x06	0.400 V
0x03	0.250 V	0x07	0.450 V

When STATE_CTL[RSNS] = 1 these settings are available

Setting	Threshold	Setting	Threshold
0x00	0.050 V	0x04	0.150 V
0x01	0.075 V	0x05	0.175 V
0x02	0.100 V	0x06	0.200 V
0x03	0.125 V	0x07	0.225 V

SCD2D (b7-b4): These upper nibble bits select the value of the short circuit in charge delay time.

Exceeding the Short Circuit in charge voltage threshold for longer than this period will turn off the CHG and DSG outputs. 0000 is the default. If STATE_CRTL[SCDDx2] is set then the delay time is double of that programmed in this register.

Setting	Time	Setting	Time	Setting	Time	Setting	Time
0x00	0 μ s	0x04	122 μ s	0x08	244 μ s	0x0c	366 μ s
0x01	30 μ s	0x05	152 μ s	0x09	275 μ s	0x0d	396 μ s
0x02	61 μ s	0x06	183 μ s	0x0a	305 μ s	0x0e	426 μ s
0x03	91 μ s	0x07	213 μ s	0x0b	335 μ s	0x0f	458 μ s

SCD2 (b3): Not used

17 Power Modes

The bq8050 has 2 main power modes, Normal and Shutdown. Hibernate is an additional mode available to the bq8050-AGG to further reduce power but this has no affect on the bq8050 AFE. Also, several additional power modes can be created under firmware control, such as Normal-Full Power and Normal-Low Power. The bq8050 can be placed in various other power modes by enabling or disabling a variety of features within the device.

The following table shows in which power mode the major blocks are typically enabled.

	Normal - Full Power	Normal	Normal - Low Power	Sleep	Hibernate	Shutdown
AGG						
High Frequency Osc	ON	ON	ON	OFF	OFF	OFF
Low Frequency Osc	ON	ON	ON	ON	OFF	OFF
CPU	ON	OFF ⁽¹⁾	OFF ⁽¹⁾	OFF	OFF	OFF
Coulomb Counter	ON	ON	ON	OFF	OFF	OFF
ADC	ON	ON	OFF	OFF	OFF	OFF
IWAKE	OFF	OFF	OFF	ON	ON	OFF
I/O Support	ON	ON	ON	ON	ON	OFF
Flash Update	ON	OFF	OFF	OFF	OFF	OFF
AFE						
LDO	ON	ON	ON	ON	ON	OFF
VCELL	ON	ON	OFF	OFF	OFF	OFF
CB FETs	OFF	OFF	ON	OFF	OFF	OFF
Protection	ON	ON	ON	ON	ON	OFF
PTC Fault	ON	ON	ON	ON	ON	ON
Shutdown Recover	OFF	OFF	OFF	OFF	OFF	ON

(1) = HALT State

17.1 Shutdown

Entry

Setting of SHUTDOWN bit in AFE:FUNCTION_CTL
OR

POR of the bq8050

Actions

All FETs turned OFF

LDO turned OFF

AFE functions turned OFF

Exit to Normal Mode

VPACK > VSTARTUP

Actions

AFE functions turned ON

XRST driven low

LDO turned ON

XRST driven high

Note: FETs NOT turned ON specifically at this mode transition

17.2 Normal

Entry

Exit from Shutdown

Actions

F/W running and controlling the operational features including FETs

In this mode the enabling and disabling of feature through F/W control and access to Hibernate mode of the AGG

Exit to Shutdown

See Shutdown

Actions

See Shutdown

18 SHA-1 Authentication

18.1 Description

For authenticating the battery pack the bq8050 uses a SHA-1 cryptographic hash function with a 128 bit split key (64 bits per key). More complete explanations of the SHA-1 algorithm are available on the WWW, see www.faqs.org/rfcs/rfc3174.html

A modified form of the SHA-1/HMAC provides the authentication function of the bq8050. Both the host and the bq8050 share two 64-bit keys used in the authentication calculation. To authenticate a battery pack, the host writes a random 20-byte message to the bq8050. The bq8050 calculates the HMAC digest in less than 50ms, replacing the random message sent by the host with the HMAC result. To complete the authentication process, the host computes the HMAC function with the same 20-byte random message originally written to the bq8050. The result is compared to the HMAC result computed by the bq8050. If the values match, the pack is authenticated.

18.2 Key programming

The bq8050 allows each of the 2 keys to be programmed individually enabling each one to be able to be programmed at different stages of the battery pack production. EG: k_1 at Texas Instruments and k_2 at the pack maker.

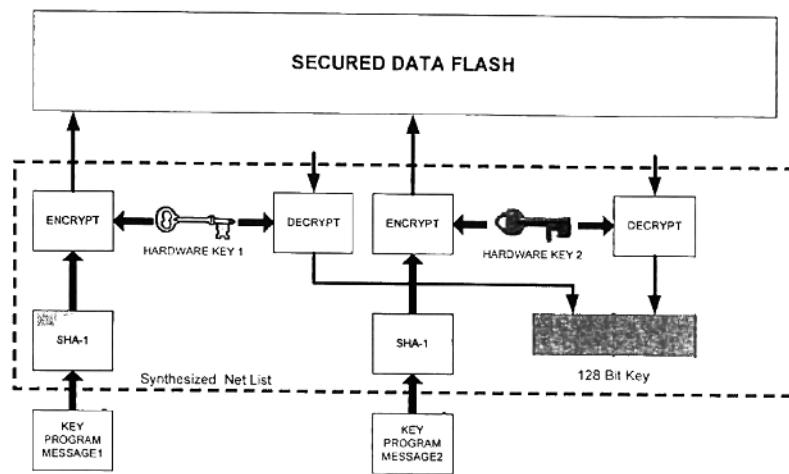
Each key consists of 64 bits providing a total key length of 128 bits which is programmed through 2 separate programming events with two separate internally generated locking bytes.

The default keys are written using the Write_Default_Keys ROM command. This command is only available if NO lock byte has been set AND the device has been reset.

KEY1 must be programmed first and during this programming the internal lock byte is set. Until a POR occurs the Write_Default_Keys command can be used to reset the keys to correct any programming errors. Once the device is reset and the newly programmed key is locked and cannot be re-programmed.

The 1st default key is cb a4 cb a4 cb a4 (in hex) and the 2nd default key is c3 17 c3 17 c3 17 c3 17 (in hex). However, the lock bytes will NOT have been set so the key can be modified.

Each key programming requires a known 160 bit message to be written to the bq8050 which pads this up to 512-bits. The bq8050 will run this message through a SHA-1/HASH cipher, take the lower 64 bits of the result and encrypt it prior to being written to the secure data flash.



18.3 Secure Flash Block

This block consists of 1 page of data (32 bytes) which has the following flash control commands

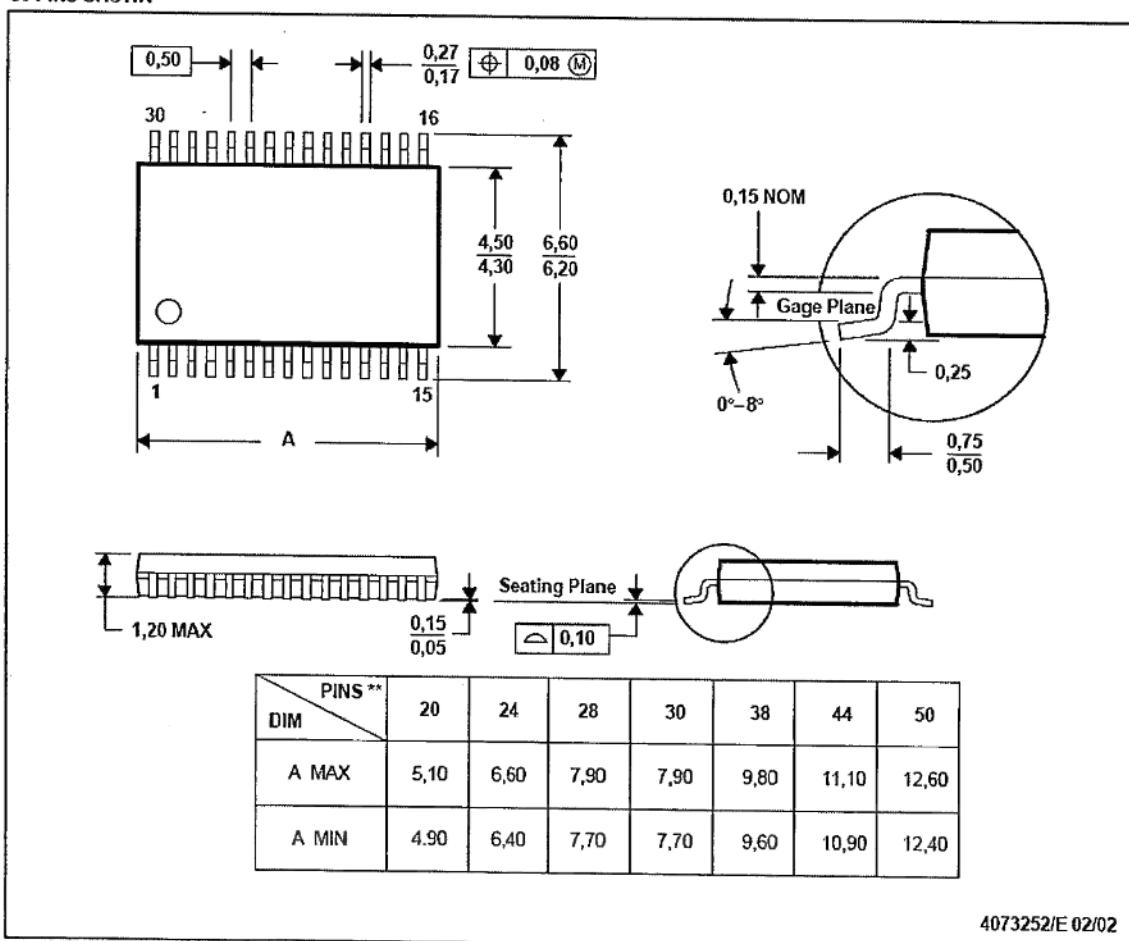
- Write_Default_Keys
 - Writes the DFIB key area with the default keys only if NO lock bytes have been set
- Write_KEY1
 - Host provides a message to ROM command, K is the default key for the write function
 - The lock byte is set and if POR is experienced then the KEY1 is locked.
 - If POR is NOT experienced then the Write_Default_Keys command is still available so KEY1 can be re-written.
- Write_KEY2
 - Host provides a message to ROM command, K is the default key for the write function
 - The lock byte is internally set and if POR is experienced then the KEY2 is locked.
 - KEY2 cannot be re-programmed (One Time Programmable)

All keys are scrambled/descrambled and the default keys will be provided to the customer.

18.4 Key Verification

KEY1 can be verified through SHA-1 authentication without programming the second key as the KEY2 will be the publicly known default key.

KEY2 will be verified through authentication. However, the owner of BOTH keys, such as an OEM, will need to provide a Message/Response combination for the party programming KEY2 for verification as they will not have KEY1.

19 Mechanical Information
DBT (R-PDSO-G)**
30 PINS SHOWN
PLASTIC SMALL-OUTLINE PACKAGE


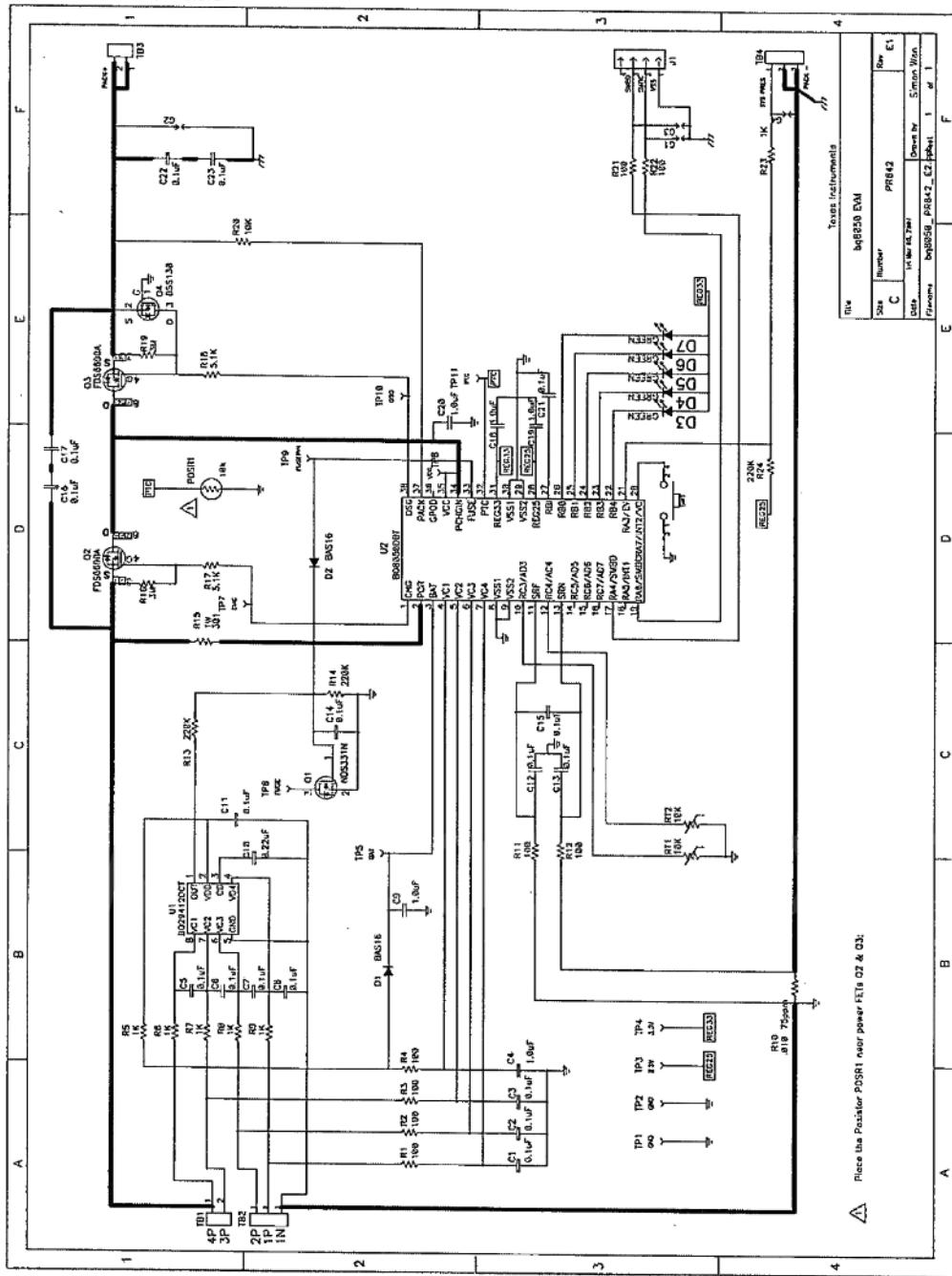
4073252/E 02/02

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-153



bq8050

20 Reference Schematic





bq8050

IMPORTANT NOTICE

Texas Instruments ("TI") warrants performance of its semiconductor products to the mutually agreed upon written specifications applicable at the time of sale, in accordance with TI's standard warranty. TI assumes no liability for applications assistance, customer product design, software performance or infringement of patents, unless expressly agreed to in a written contract with the customer.

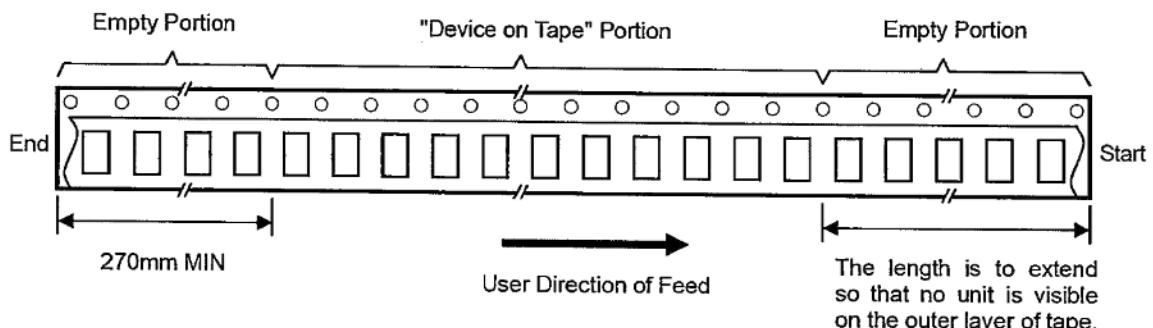
In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Testing and other quality control techniques are utilized to the extent TI deems necessary to support its product warranty. Specific testing of all parameters of semiconductor products is not necessarily performed. Only those tests mutually agreed upon in writing, including failure modes & effects analyses, will be performed for custom product, except as mandated by government requirements.

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE, FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS (i.e., applications which may involve potential risks of death, personal injury, or severe property or environmental damage). Inclusion of TI products in such applications is understood to be fully at the risk of the customer and requires written approval from an appropriate TI officer. Questions concerning potential risk applications should be directed to the appropriate TI sales contact.

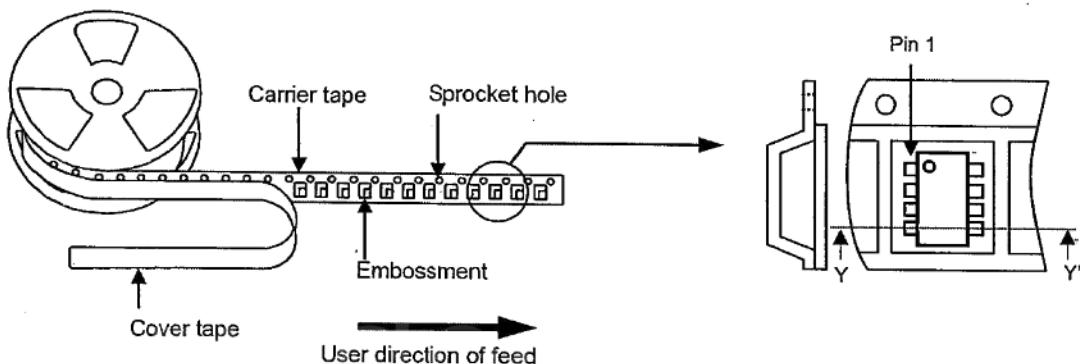
TI does not warrant or represent that any license, either expressed or implied, is granted under any patent right, copyright, maskwork right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which TI semiconductor products or services might be or are used.

信頼性試験項目（対象：プラスチックパッケージ品）

No.	試験項目	試験条件	準拠規格
1	高温連続動作	温度：125°C 時間：1,000 ^{+48/-0} h	STM-1159-7. 8
2	高温高湿バイアス	SMD の場合前処理として項目 7.2a を実施 温度：85±2°C、85±5%RH 時間：1,000 ^{+48/-0} h	STM-1159-7. 12
3	高温放置	温度：125°C以上、放置 時間：1,000 ^{+48/-0} h	STM-1159-7. 9
4	P C T	SMD の場合前処理として項目 7.2a を実施 温度：120±2°C、85±5%RH、気圧約 1.7×10^6 Pa 時間：96±4h	STM-1159-7. 13
5	温度サイクル	SMD の場合前処理として項目 7.2a を実施 以下の温度サイクルを繰り返し 100 サイクル行う +125°C/30 分→常温 10~15 分→-55°C/30 分→常温 10~15 分	STM-1159-7. 5
6	はんだ濡れ性	前処理条件：100°C、100%RH、4h (SMD) /8h (THD) 使用フラックス：NA200 使用はんだ：無鉛 Sn-3Ag-0.5Cu、有鉛 Sn-37Pb はんだ温度：無鉛 245±3°C、有鉛 230±2°C はんだ浸漬時間：無鉛 2~3 秒、有鉛 3 秒	STM-1159-7. 1a STM-1254-1 STM-1254-2
7	はんだ耐熱性	リフロー：ピーカ 250 ^{+5/-0} °C リフロー：230°C以上、30±10 秒 予備加熱：150~180°C、90±30 秒 リフロー回数：2 回（1 回目と 2 回目の間に吸湿） 吸湿条件：SS-00254-5-5.1 中の各レベルに従う 手はんだ：こて先温度 350°C±10°C、3 ^{+1/-0} 秒	STM-1159-7. 2a, b STM-1254-4, 5
8	端子強度	引張り強度：SS-00159-6 中の表 1 の引張力を 10±1 秒加える 曲げ強度：90° 曲げ 2 回	STM-1159-6. 5a, b
9	塩水噴霧	温度：35±2°C 塩濃度：5±1wt% 放置時間：24 時間	STM-1159-7. 6
10	はんだ接合耐久性	前処理条件：100°C、100%RH、4h (SMD) /8h (THD) 温度サイクル条件：-35±5°C/105±5°C、各 15 分、1000 サイクル	STM-1159-7. 3a, b STM-1254-6 STM-1254-7
11	ウイスカ	温度サイクル条件：-35±5°C/125±5°C、各 7 分、500±4 サイクル 高温高湿条件：85±2°C、85±5%RH、500±4h	STM-1159-7. 17 STM-1254-8
12	静電耐圧	HBM : C=100pF, R=1.5kΩ > ±1000V CDM : R=1, Ω±10% > ±500V	STM-1159-7. 14 STM-1159-7. 15

Emboss taping specification for TSSOP**Package code : DBT 38 pin****1. Emboss taping specification****1.1 Empty tape portion****Carrier tape and pockets****1.2 Device quantity and direction**

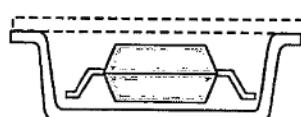
Toward pulling out direction of tape, polarity mark (Pin 1) is at the left side.

**Direction of device**

PACKAGE SUFFIX	T & R SUFFIX	PIECES / REEL
DBT	R	2,000

1.3 Insertion of device

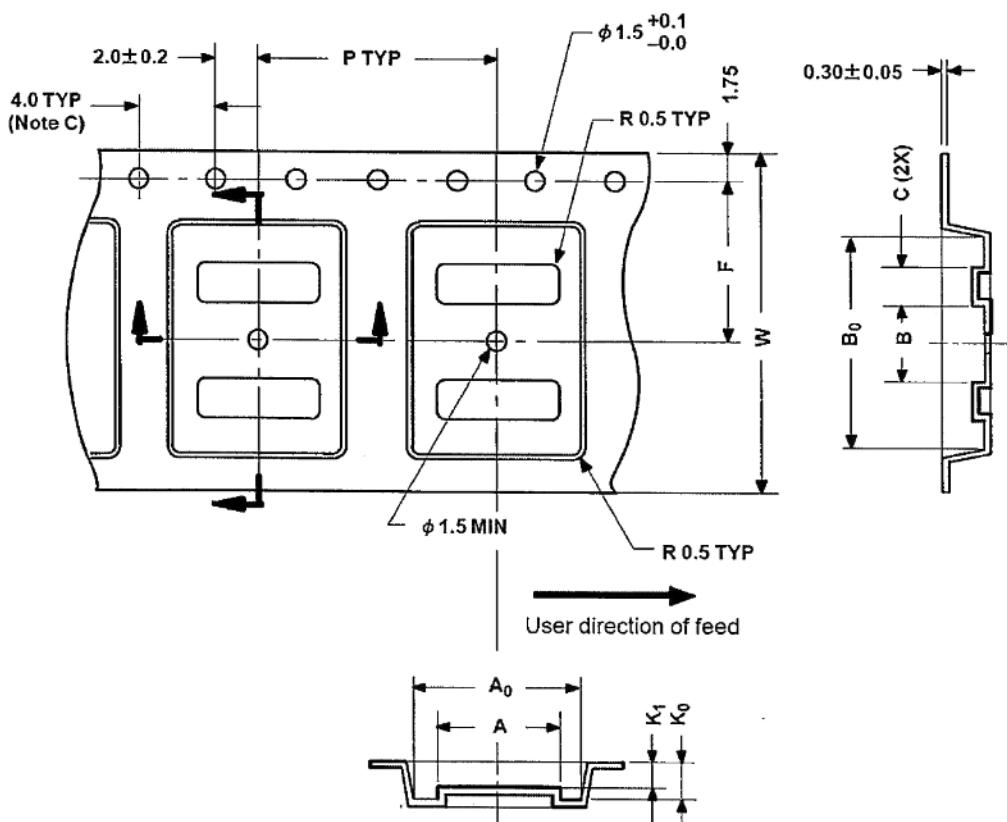
The device is located such as symbolization in upper side and lead pins in lower side.



SECTION Y-Y'

1.4 Tape Specification

a) Tape dimension (16 mm width Tape) (Notes A, B)



NOTES : A. Tolerance unless otherwise specified : ± 0.10 .

B. Unless otherwise noted, R = 0.3 MAX.

C. 10 pitch cumulative tolerance : ± 0.20 .

PACKAGE SUFFIX	PIN	A	A ₀	B	B ₀	C	K ₀
DBT	38	2.6	6.9	4.0	10.2	2.1	1.8

K ₁	F	P	W
1.3	7.5	12.0	16.0 ± 0.3

Tape dimension (UNIT : mm)

b) Cover tape

The cover tape does not cover the index hole and does not shift to outside from carrier tape.

c) Tape structure

The carrier tape is made of plastic and the structure is shown in above schematic.

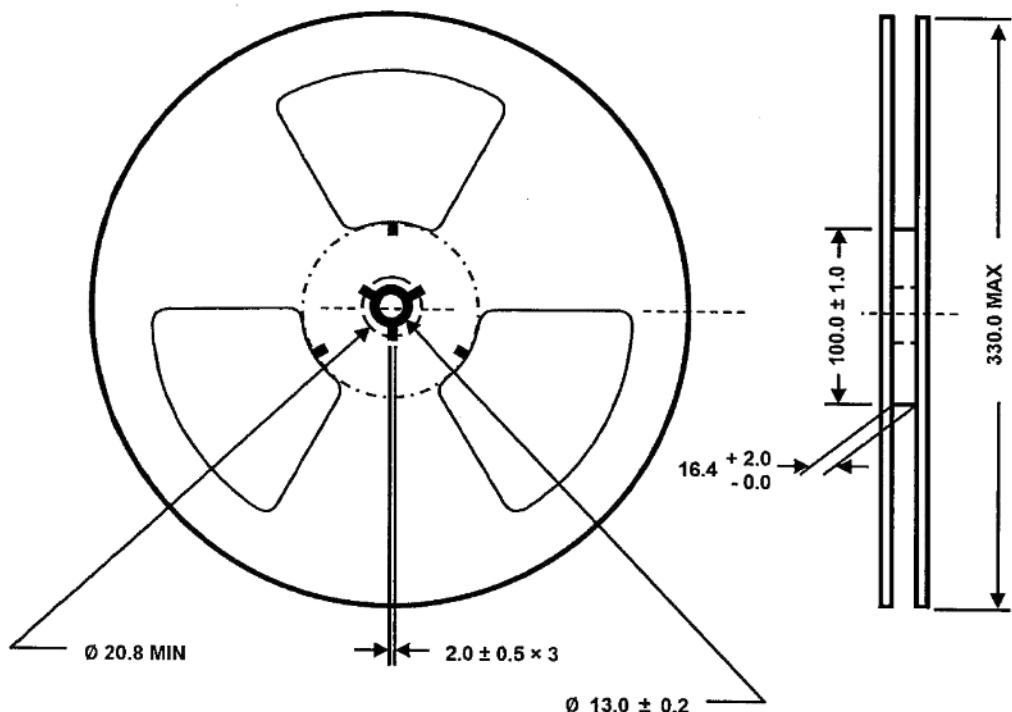
The device is put on embossed area of carrier tape, and covered by cover tape made of plastic.

d) ESD Countermeasure

Plastic material used in both carrier tape and cover tape are static dissipative.

1.5 Reel Specification

a) Reel dimension (\varnothing 330 mm Reel, 16 mm width Tape)



Reel dimension (UNIT : mm)

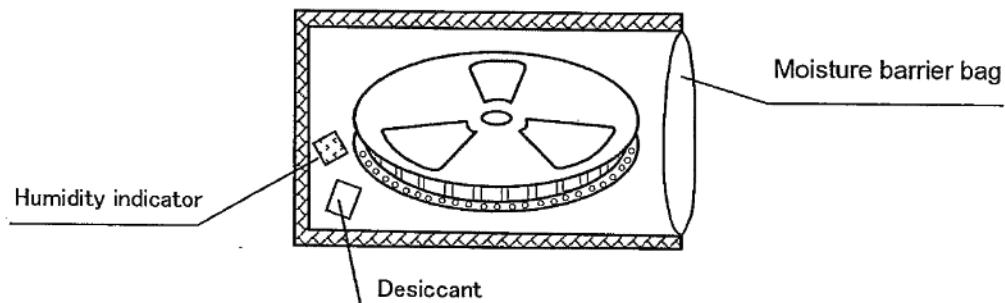
This reel drawing is just for showing dimensions, so the design may be different.

b) Material

Polystyrene (Static Dissipative / Antistatic)

2. Packing method

The reel is packed into Moisture Barrier bag with desiccant, humidity indicator, and fastened by heat-sealing after fixed the end of leader tape by tape.

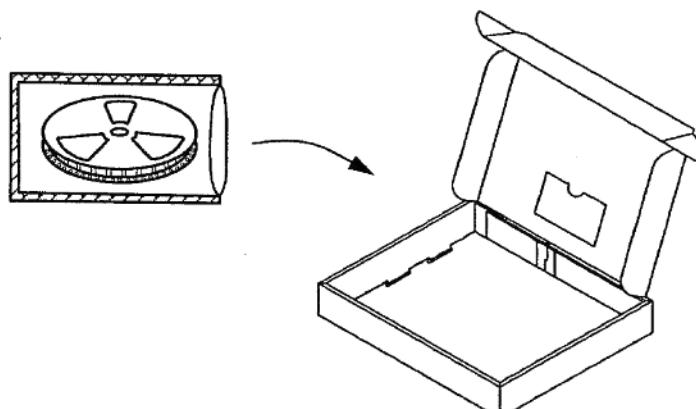


Reel dry packing method

3. Packing Specification

3.1 Reel Box

Each Moisture Barrier bag is packed into reel box.

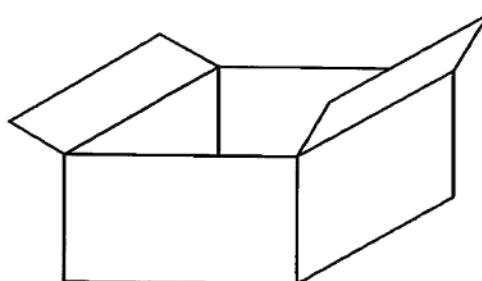


3.2 Reel Box Material

Corrugated Fiberboard

3.3 Shipping Box

The filler such as cushion is added if space exists inside.
The size of shipping box will be changed per packing quantity of reel box.



Shipping box (carton)

3.4 Shipping Box Material

Corrugated fiberboard



保管条件、実装条件

1. 対象製品

BQ8050DBTR

2. 推奨保管条件

① 保管環境（梱包開封前後共）

温度：5～30°C

湿度：40～60%RH

② 保管期間

● 防湿梱包開封後：JEDEC Moisture Sensitibity (MS) Level-2/260°Cで認定。

開封後、1年以内に実装して下さい。

リフロー回数は2回までとして下さい。

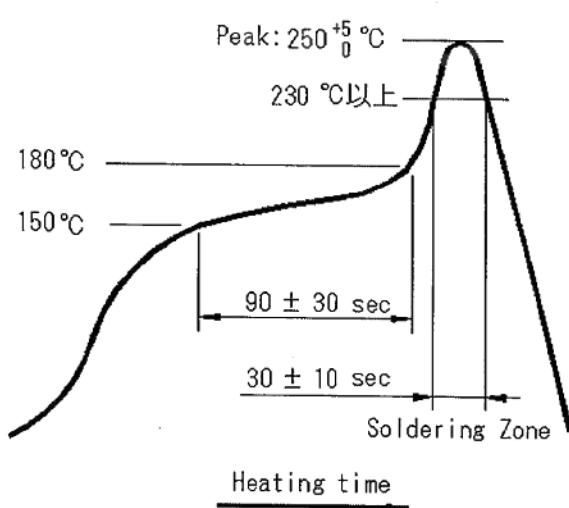
上記保管期間を過ぎた場合、125°C/24時間でドライバークを行い
実装して下さい。尚、再ベークは2回以内にして下さい。

3. STM-1254（初版）表面実装部品はんだ耐熱性レベル

STM-1254【C】相当 30°C 70%RH 192h (1回目、2回目とも)

* JEDEC及びSTM-1254-5についての相関データは別途取得しております。
ご要求いただければ提出させていただきます。

4. 推奨リフロープロファイル



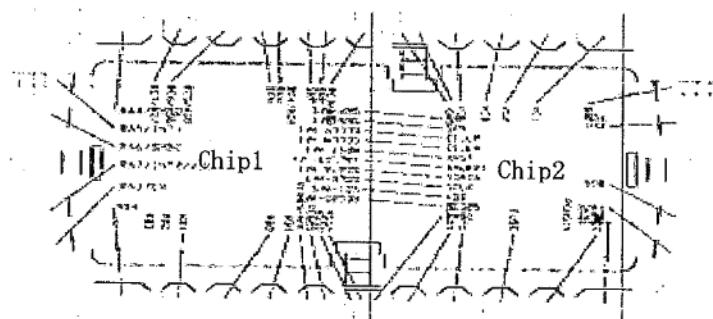
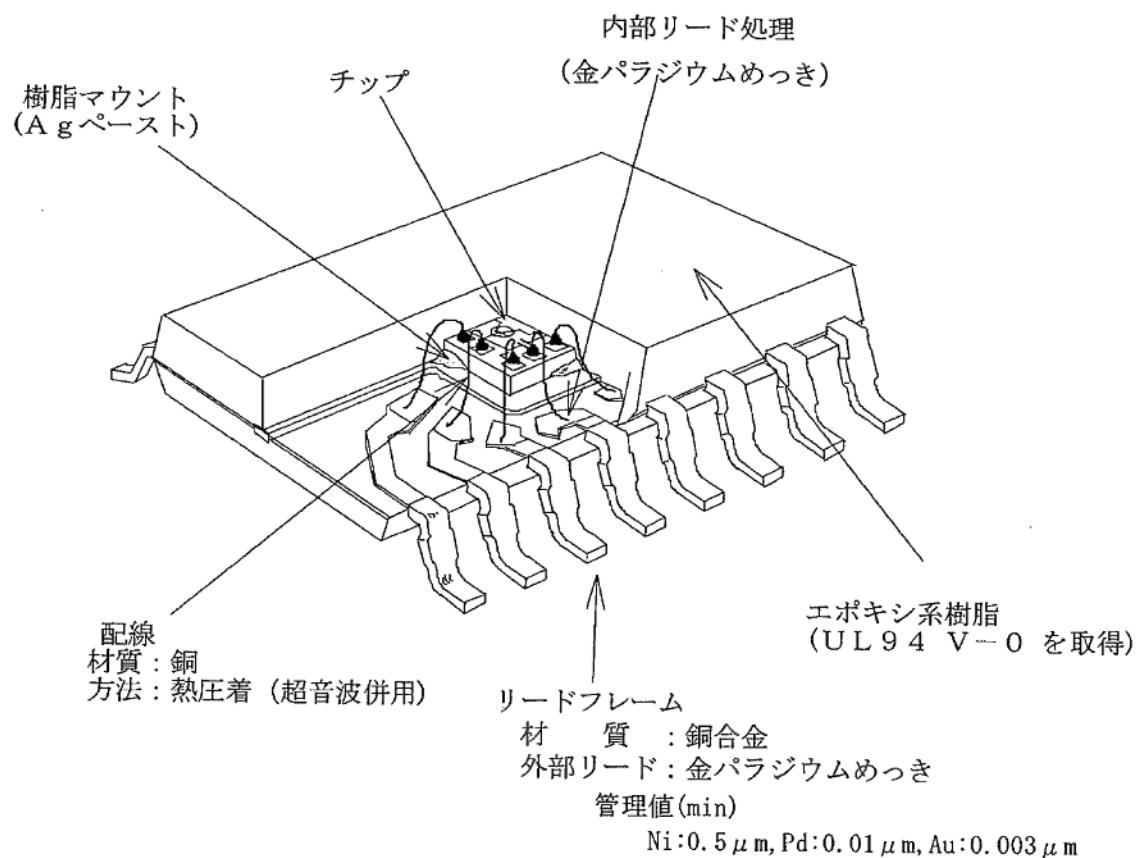
温度測定箇所は、本体表面部温度での温度プロファイルを示しております。

5. 手はんだ条件

$350^{\circ}\text{C} \pm 10^{\circ}\text{C}$ $3^{+1/-0}\text{秒}$ 推奨可能

◆ パッケージの構造図
(T S S O P)

《 代表例 》



Q C 工 程 図

● ウエハー工程

フロー	工程名	管理項目	点検項目	検査項目	実施部門	標準類	備考
	酸化		生成条件	時間・温度 ガス流量	製造	社内標準による	※酸化、フォトリソグラフィーに必要事項をインプットすることによりステップトラベラーが発行される。
		酸化膜の品質		酸化膜厚・外観			
	フォトリソグラフィー		形成条件	レジスト塗布 露光量 エッチング時間	製造	社内標準による	
		パターン形状		外観			
	拡散		生成条件	時間 ガス流量	製造	社内標準による	
		拡散の状態		酸化膜厚・外観 シート抵抗			
	エピタキシャル		生成条件	時間・温度 ガス流量	製造	社内標準による	
		エピ層の品質		外観 エピ層の厚み 比抵抗			
	メタライゼーション		生成条件	時間・温度 真空度	製造	社内標準による	
		金属膜の品質		外観 金属膜厚			
	配線形成		形成条件	レジスト塗布 露光量 エッチング時間	製造	社内標準による	
		パターン形成		外観			
	保護膜生成		生成条件	時間・温度 ガス流量	製造	社内標準による	
		保護膜の品質		屈折率 保護膜の厚み			
	素子特性検査	電気的特性		トランジスタ特性 抵抗値	製造	社内標準による	
	電気的特性検査		使用プログラム テスター精度	歩留り	製造	社内標準による	
	出荷検査	外観特性		外観全般			
			ロット履歴	トラベラー	品質保証	社内標準による	
	梱包	デバイス/数量		梱包外観	製造	社内標準による	
			特殊仕様				
	各工程における異常発生時は、工程異常処理標準による。						
	保管・出荷	デバイス/数量	出荷計画				
			出荷先				



TSSOP QC 工程図

フロー	工程名	管理項目	点検項目	検査項目	実施部門	関連標準
	セットアップ	生産・日程管理	デバイスタイプ 進捗度	トラベラ内容	製造	社内標準による
	ダイアッブ	ダイシング条件	速度・ピッチ 水の電導度	設定条件	製造	社内標準による
		ダイシング		外観(チップクラック)		
	ダイマウント	マウント条件	樹脂保管条件	温度	製造	社内標準による
				設定条件		
		マウント状態	キュア条件	温度・時間		
	リヤーポイント	ボンド条件		設定条件	製造	社内標準による
			ヒート条件	温度		
		ボンド状態		外観(位置・形状)		
			配線強度	引っ張り強度		
	プラスチック樹脂成形	モールド条件	材料保管条件		製造	社内標準による
			金型温度	外観		
			ラムスピード	流れ中断・位置		
			キュア条件	温度・時間		
		モールド状態		外観全般		
	捺印切断形状成形	捺印条件			製造	社内標準による
		切断成形条件				
		切断成形状態		外観・特性		
	電気的特性選別	電気特性(全数検査)	使用プログラム	歩留り	製造	社内標準による
			テスト精度			
	出荷保証検査	電気特性	使用プログラム	DC/AC 特性	品質保証	社内標準による
				初期故障モニター		
	外観選別	PKG外観		外観全般	製造	社内標準による
				デバイスタイプ		
	出荷保証検査	外観		外観・形状	品質保証	社内標準による
			ロット履歴	トラベラ内容		
	入庫	デバイス数量	ロット履歴	トラベラ	製造	社内標準による
				特殊仕様		
	テーピング	テーピング条件	使用材	デバイス・数量	製造	社内標準による
		テーピング状態		テーピング外観		
	出荷検査	出荷先		特殊仕様	品質保証	社内標準による
	梱包出荷	デバイス・数量	納品計画		製造	社内標準による
		出荷先	納品伝票			
	輸送・納品					
		各工程における異常発生時は、工程異常処理標準による。				

信頼性データ報告書

デバイス名 : B Q 8 0 5 0 D B T R

◆前処理

ベーグ : 125°C 24 時間 → 加湿 : 168 時間 (85°C/60%) → IR リフロー 260°C+0°C/-5°C × 3 回

試験内容	試料数	試験時間
	(個)	96H
(1) 不飽和蒸気加圧連続通電試験 130°C/85%RH	40	0
(2) 高温放置試験 T A=150°C	77	1000H
		0
(3) プレッシャークッカー試験 121°C/100%RH	77	240H
		0
(4) 热衝撃試験 -65°C/+150°C	77	1000cyc
		0
(5) 温度サイクル試験 -65°C/+150°C	77	1000cyc
		0
(6) 高温動作寿命試験 T A=125°C	116	1000H
		0

★ 推定故障率 (FITS) : EA = 0.7EV, 60%U.C.L. にて
周囲温度 55°Cへの換算値

デバイスアワー = 116 Khrs

$$0.917 / (116K \times 77.82) = 101.6 \text{ FIT}$$

上記(6)の限られた試料数に基づきます。

(6) 静 電 耐 压 試 驗	Machine Model	印加電圧 (V)	+/-200
		R=0Ω, C=200pF	0/3
	Human Body Model	印加電圧 (kV)	+/-1.0
		R=1.5kΩ, C=100pF	0/3
	CDM	印加電圧 (V)	+/-500
		R=1Ω +/-10%	0/3

コメント :

半導体製品構造説明資料

2010年12月9日

製品名	用途・機能 AGG and AFE for 2 to 4 cells application			メーカー名 日本テキサス・インスツルメンツ株式会社
				Z101209020
ウェハー製造工場 Chip1: ダラス工場 (米国) Chip2: 協力工場 (TSMC-F10中国)	組立工場 TI タイwan TI マレーシア	テスト工場 TI タイwan TI マレーシア 協力工場 (台湾アーティック)	責任者  2010/12/10	作成者  2010/12/10
営業・技術本部 カスタマ・ドキュメント・センタ				
外形 ピン数	DIP SOP(SOIC) HSOP SSOP TSSOP VSSOP HTSSOP SOT QFP HTQFP QFJ(PLCC) QFN(SON) W CSP BGA 他 () . ピン数 38 ピン			
リードフレーム素材	銅系 鉄系 () 他 ()			
インナーリード部処理	Agメッキ Auメッキ 他 (NiPdAuメッキ)			
アウターリード部処理	NiPdAu SnAgCu Auメッキ Snメッキ 他 ()			
チップマウント方法	Agペースト Au-Si共晶 はんだ 他 ()			
ワイヤーボンド方法	TSB(超音波熱圧着), TSB(熱圧着), USB(超音波), 他 ()			
ワイヤー 材質・線径	Au Al Cu 他 () . 線径 24 μm			
モールド材質	エポキシ シリコーン 他 ()			
モールド方法	トランスマルチモールド キャスティング ポッティング 流動浸漬 他 ()			
パッケージ (ケース) 材質	セラミック 他 ()			
シール方法	ハーメチック 樹脂 はんだ ガラス 他 ()			
インナーコート材	有 () . 無			
プロセス	Chip-1 CMOS NMOS BIPOROR Chip-2 BiCMOS 他 ()			
構成素子数 (ゲート数)	500以下 501~1,000 1,001~3,000 3,001~5,000 5,001以上			
チップサイズ (mm)	Chip1 2.10mm × 2.07mm / Chip2 2.25mm × 2.89mm			
オーバー パシベーション	SiO ₂ Si ₃ N ₄ PSG ポリイミド 他 (窒化膜) . 無			
ソニー記入欄				

※ 上記内容が記載されていれば別フォーマットでも可。

半導体製品品質説明資料

BQ8050DBTR

工程概略及び品質管理工程表	別紙添付、提出済の _____ 製品と同、他()							
出荷検査(入庫検査)規準	別紙添付、提出済の _____ 製品と同、他()							
信頼性管理規準	別紙添付、提出済の _____ 製品と同、他()							
信頼性試験成績	Lot No. _____				Human Body Model 静電強度(ピンNoを記入) $C = 100\text{pF}$ $R = 1.5\text{k}\Omega$ 全ピン対 全ピン対 GND 電源ピン			
条件はソニー技術標準SS-00159~162による 又は MIL 又は、JEDECに準拠 本資料は、下記代表デバイスでの信頼性試験結果です。 代表デバイス名: BQ29330DBT								
選考理由: 弊社信頼性評価基準に従って、最大チップサイズ、最大ピン数、も しくは最もセンシティブなデバイス等のシミュレーションにて最悪 条件になるデバイスを選出していきます。PCN20100508000								
試験項目	試験条件	試験時間	試験数	故障数	破壊電圧	(+/-)		
温度サイクル試験	-65°C/+150°C	500cyc	77	0	~1.0 kV	-		
高温放置試験	TA=170°C	420h	77	0	~1.5 kV	-		
プレッシャークッカー	121°C	96h	77	0	~2.0 kV	-		
熱衝撃試験	-65°C/+150°C	1000cyc	77	0	Charged Device Model $R = 1\Omega \pm 10\%$ 全ピン			
					破壊電圧	(+/-)		
					~250 V	-		
					~500 V	-		
動作試験回路図		測定項目及び故障判定基準						
項目	測定条件	規格	故障					
	カタログ規格値							
S: 初期値 U: 規格上限値 L: 規格下限値								

※ 上記内容が記載されていれば別フォーマットでも可。