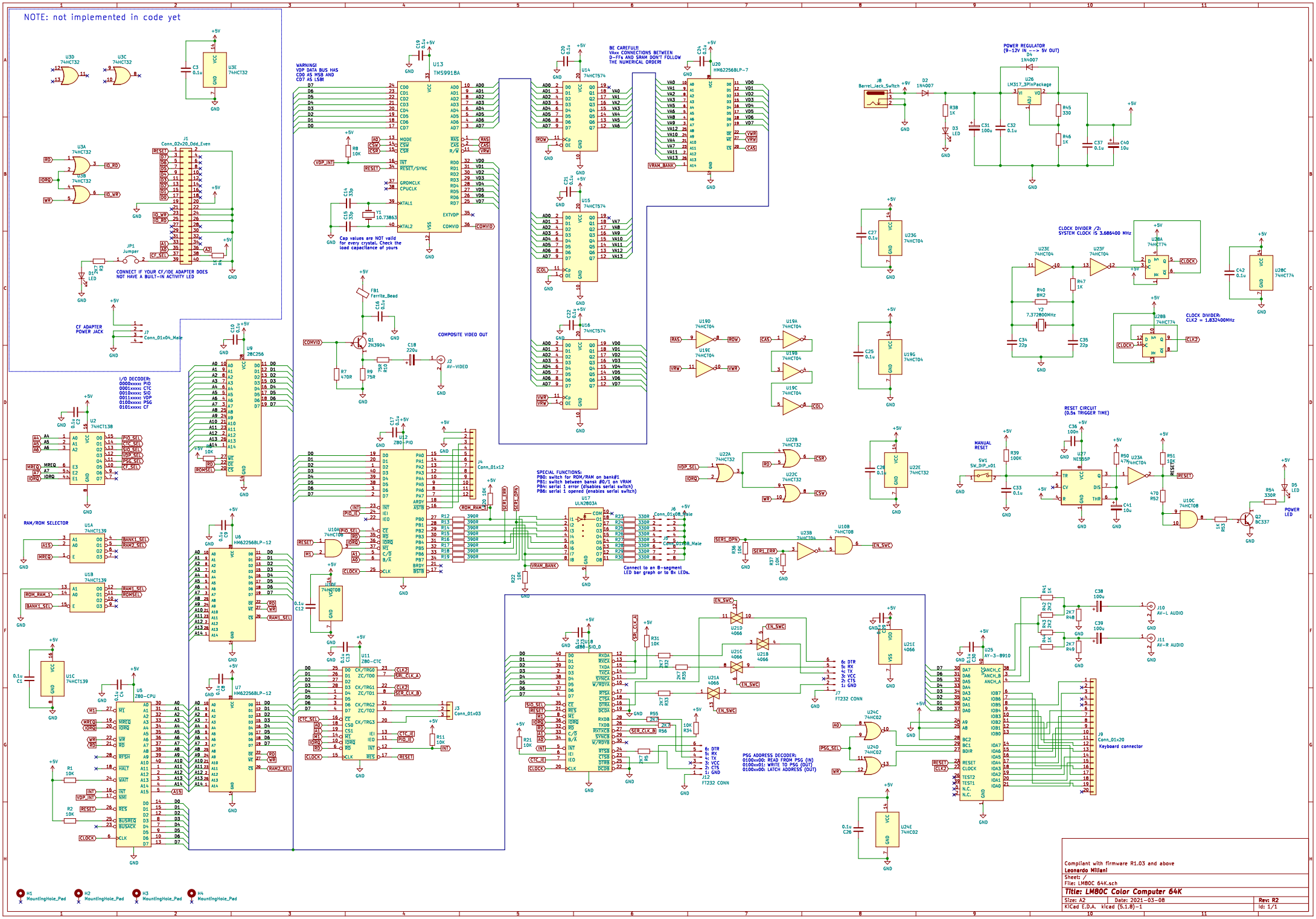
NOTE: not implemented in code yet
WARNING!
VDP DATA BUS HAS
CD0 AS MSB AND
CD7 AS LSB!
BE CAREFUL!!
Vxxx CONNECTIONS BETWEEN
D-FFs AND SRAM DON'T FOLLOW
THE NUMERICAL ORDER!
POWER REGULATOR
(9-12V IN ---> 5V OUT)
CONNECT IF YOUR CF/IDE ADAPTER DOES
NOT HAVE A BUILT-IN ACTIVITY LED
CF ADAPTER
POWER JACK
Cap values are NOT valid
for every crystal. Check the
load capacitance of yours
COMPOSITE VIDEO OUT
I/O DECODER:
0000xxxx: PIO
0001xxxx: CTC
0010xxxx: SIO
0011xxxx: VDP
0100xxxx: PSG
0101xxxx: CF
CLOCK DIVIDER /2:
SYSTEM CLOCK IS 3.686400 MHz
CLOCK DIVIDER:
CLK2 = 1.8324000MHz
RESET CIRCUIT
(0.5s TRIGGER TIME)
MANUAL
RESET
POWER
LED
RAM/ROM SELECTOR
SPECIAL FUNCTIONS:
PB0: switch for ROM/RAM on bank#1
PB1: switch between bank #0/1 on VRAM
PB4: serial 1 error (disables serial switch)
PB6: serial 1 opened (enables serial switch)
Connect to an 8-segment
LED bar graph or to 8x LEDs.
6: DTR
5: RX
4: TX
3: VCC
2: CTS
1: GND
FT232 CONN
PSG ADDRESS DECODER:
0100xx00: READ FROM PSG (IN)
0100xx01: WRITE TO PSG (OUT)
0100xx00: LATCH ADDRESS (OUT)
Keyboard connector
Compilant with firmware R1.03 and above
Leonardo Milani
Sheet: /
Files: LM80C 64K.sch
Title: LM80C Color Computer 64K
Size: A2
Date: 2021-03-08
Rev: R2
KiCad E.D.A. kicad (5.1.8)-1
Id: 1/1