The Simplest CPU Arch Possible

(SCAP)

1: System Specs

1.0: Registers

BIN	HEX	NAME	BITS	INIT VAL
00	0x0	A	8	0x00
01	0x1	В	8	0x00
inaccessible	inaccessible	PC	16	0x0000
10 (upper) 11 (lower)	0x2 (upper) 0x3 (lower)	SP	16	0x00FF
inaccessible	inaccessible	FLAGS	8	0x00

1.1: Instructions

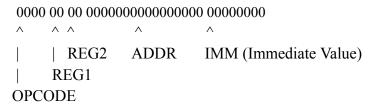
BIN	HEX	NAME	I/O
0000	0x0	LD	REG1, ADDR
0001	0x1	ST	REG1, ADDR
0010	0x2	MV	REG1, REG2
0011	0x3	ADD	REG1, REG2
0100	0x4	SUB	REG1, REG2
0101	0x5	SL	REG1
0110	0x6	PUSH	REG1
0111	0x7	РОР	REG1
1000	0x8	JMP	ADDR
1001	0x9	JZ	ADDR
1010	0xA	JNZ	ADDR
1011	$\theta x B$	LDP	REG1, ADDR
1100	θxC	LDI	REG1, IMM
1101	θxD	CALL	ADDR
1110	0xE	RET	-
1111	$\theta x F$	NOP	-

2: Memory

2.0: Details for external hardware support

The SCAP has an 8 bit data bus and a 16 bit address bus. The memory layout can be anything on devices using SCAP, so you may want to keep the devices mapped between 0xFF00 and 0xFFFD.

3: Instruction Format



4: Interrupts

When the interrupt line is pulsed, the CPU jumps to the address whose lower byte is the byte read from 0xFFFE and upper one is the byte read from 0xFFFF. Interrupts behave like CALL instructions.