

# The Simplest CPU Arch Possible

(SCAP)

## 1: System Specs

### 1.0: Registers

BIN	HEX	NAME	BITS	INIT VAL
<i>00</i>	<i>0x0</i>	A	8	0x00
<i>01</i>	<i>0x1</i>	B	8	0x00
<i>inaccessible</i>	<i>inaccessible</i>	PC	16	0x0000
<i>10 (upper) 11 (lower)</i>	<i>0x2 (upper) 0x3 (lower)</i>	SP	16	0x00FF
<i>inaccessible</i>	<i>inaccessible</i>	FLAGS	8	0x00

### 1.1: Instructions

BIN	HEX	NAME	I/O
<i>0000</i>	<i>0x0</i>	LD	REG1, ADDR
<i>0001</i>	<i>0x1</i>	ST	REG1, ADDR
<i>0010</i>	<i>0x2</i>	MV	REG1, REG2
<i>0011</i>	<i>0x3</i>	ADD	REG1, REG2
<i>0100</i>	<i>0x4</i>	SUB	REG1, REG2
<i>0101</i>	<i>0x5</i>	SL	REG1
<i>0110</i>	<i>0x6</i>	PUSH	REG1
<i>0111</i>	<i>0x7</i>	POP	REG1
<i>1000</i>	<i>0x8</i>	JMP	ADDR
<i>1001</i>	<i>0x9</i>	JZ	ADDR
<i>1010</i>	<i>0xA</i>	JNZ	ADDR
<i>1011</i>	<i>0xB</i>	LDP	REG1, ADDR
<i>1100</i>	<i>0xC</i>	LDI	REG1, IMM
<i>1101</i>	<i>0xD</i>	CALL	ADDR
<i>1110</i>	<i>0xE</i>	RET	-
<i>1111</i>	<i>0xF</i>	NOP	-

## 2: Memory

### 2.0: Details for external hardware support

The SCAP has an 8 bit data bus and a 16 bit address bus. The memory layout can be anything on devices using SCAP, so you may want to keep the devices mapped between 0xFF00 and 0xFFFD.

## 3: Instruction Format

```
0000 00 00 0000000000000000 00000000
^      ^ ^      ^      ^
|      | REG2   ADDR    IMM (Immediate Value)
|      REG1
OPCODE
```

## 4: Interrupts

When the interrupt line is pulsed, the CPU jumps to the address whose lower byte is the byte read from 0xFFFFE and upper one is the byte read from 0xFFFF. Interrupts behave like CALL instructions.