HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6513

512 x 4 CMOS RAM

Features

- LOW POWER STANDBY — 250μW MAX.
- LOW POWER OPERATION — 35mW/MHz MAX.
- DATA RETENTION — @ 2.0V MIN.
- TTL COMPATIBILITY INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- FAST ACCESS TIME — 300nsec MAX.
- INDUSTRIAL OR COMMERCIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- PINOUT ALLOWS UPGRADE TO HM-6514

Description

The HM-6513 is a 512 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6513 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6513 is supplied in two versions, the HM-6513H and the HM-6513L. The H or L is used to designate the logic level to be connected to the Y input. If a HM-6513H is procured the user must connect the input to VCC in the system. If a HM-6513L is used the Y input must be connected to system ground.

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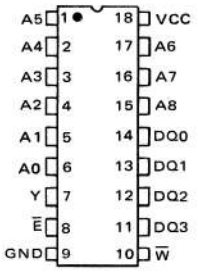
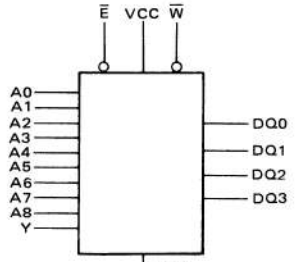
Pinout

TOP VIEW

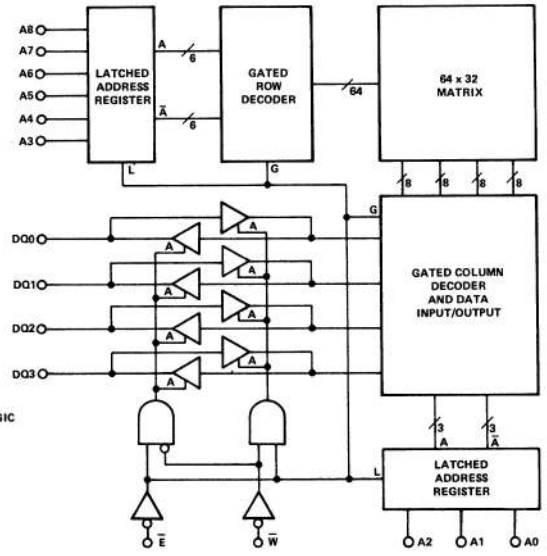


Logic Symbol



A – Address Input
Ē – Chip Enable
W̄ – Write Enable
DQ – Data In/Out
Y – Hard Wired Input

Functional Diagram



ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTERS:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Range Industrial (-9)	-40°C to 85°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	µA	IO = 0VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	170	ns	(4)
	TAVQV	Address Access Time		320	170	ns	(4)
	TELQX	Chip Enable Output Enable Time		100	50	ns	(4)
	TWLQZ	Write Enable Output Disable Time	20	100	40	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	300		150	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	300		150	ns	(4)
	TELWH	Write Enable Pulse Hold Time	300		150	ns	(4)
	TDVWH	Data Setup Time	200		100	ns	(4)
	TWHDZ	Data Hold Time	0		-10	ns	(4)
	TWLDV	Write Data Delay Time	100		50	ns	(4)
	TWLEL	Early Output High-Z Time	0		-10	ns	(4)
	TEHWH	Late Output High-Z Time	0		-10	ns	(4)
	TELEL	Read or Write Cycle Time	420		240	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

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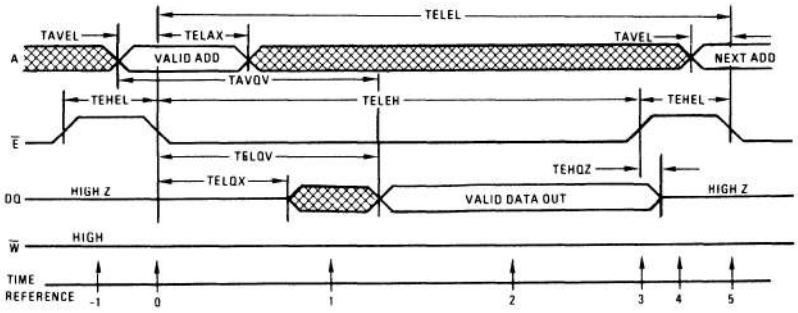
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Commercial	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Range Commercial	0°C to +75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C (1) VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	50	µA	VI = VCC or GND IO = 0
	ICCOP	Operating Supply Current (2)		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	10	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	±0.5	µA	GND ≤ VIO ≤ VCC
	VIL	Logical "0" Input Voltage	-0.3	0.8	2.0	V	
	VIH	Logical "1" Input Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Logical "0" Output Voltage		0.45	0.35	V	IO = 1.6mA
	VOH	Logical "1" Output Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	(4)
	TAVQV	Address Access Time		370	200	ns	(4)
	TELQX	Chip Enable Output Enable Time		100	50	ns	(4)
	TWLQZ	Write Enable Output Disable Time	20	100	50	ns	(4)
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	150		100	ns	(4)
	TAVEL	Address Setup Time	20		0	ns	(4)
	TELAX	Address Hold Time	50		20	ns	(4)
	TWLWH	Write Enable Pulse Width	350		200	ns	(4)
	TWLEH	Write Enable Pulse Setup Time	350		200	ns	(4)
	TELWH	Write Enable Pulse Hold Time	350		200	ns	(4)
	TDVWH	Data Setup Time	250		150	ns	(4)
	TWHDZ	Data Hold Time	0		-10	ns	(4)
	TWLDV	Write Data Delay Time	100		50	ns	(4)
	TWLEL	Early Output High-Z Time	0		-10	ns	(4)
	TEHWH	Late Output High-Z Time	0		-10	ns	(4)
	TELEL	Read or Write Cycle Time	500		320	ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle

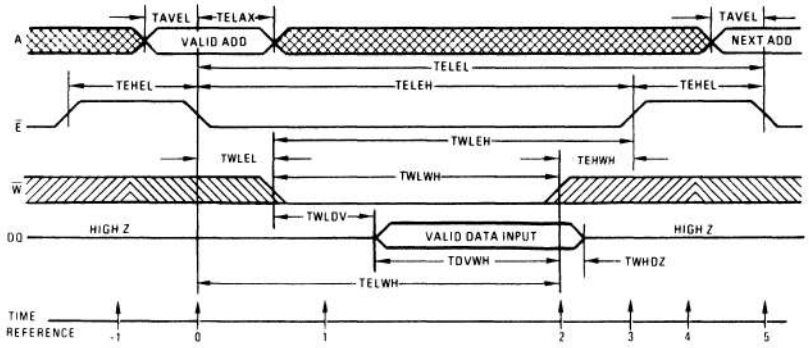


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TLWDV must be met to allow the $\overline{W}$ signal time to disable the outputs before

applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before E. The RAM outputs will disable (three-state) after E rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

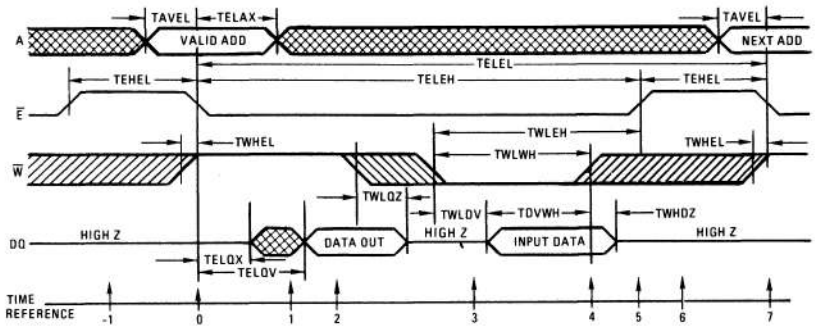
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Read Modify Write Cycle



TRUTH TABLE

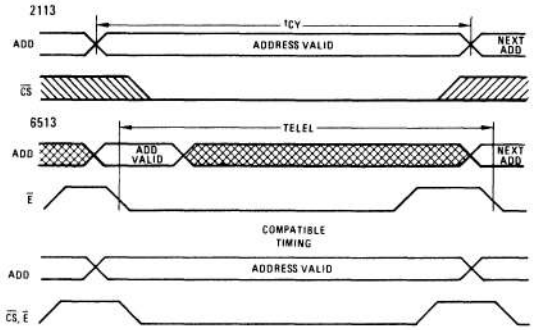
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = X) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2113 Compatibility



2113 – Requires the Address to Remain Valid Throughout the Cycle.

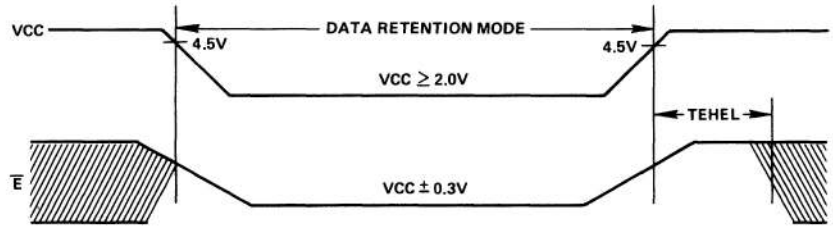
6513 – Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Suggestions For 6513 Memory Array Design

The HM-6513 is a device that can be used to good advantage in systems which are offered with choices of memory array size. With one common memory board layout the designer can easily offer two different array sizes. This is accomplished by using the conveniently similar pinouts of the HM-6513 (512 by 4) and the HM-6514 (1K by 4). For example, a 4K by 8 bit array using HM-6513s and a 8K word by 8 bit array using HM-6514s can be easily implemented on the same printed circuit card. The circuit diagram suggests one implementation requiring only one jumper wire for 4K or 8K word selection. This simple jumper wire also allows the 4K array to utilize the HM-6513H or the HM-6513L version.