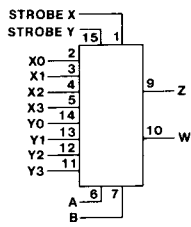


NOT  
RECOMMENDED FOR  
NEW DESIGNS



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8

92CS-39293

#### FUNCTIONAL DIAGRAM

## CMOS Dual 4-Channel Analog Data Selector

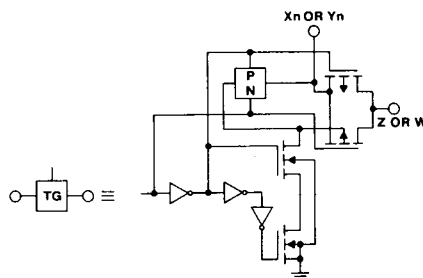
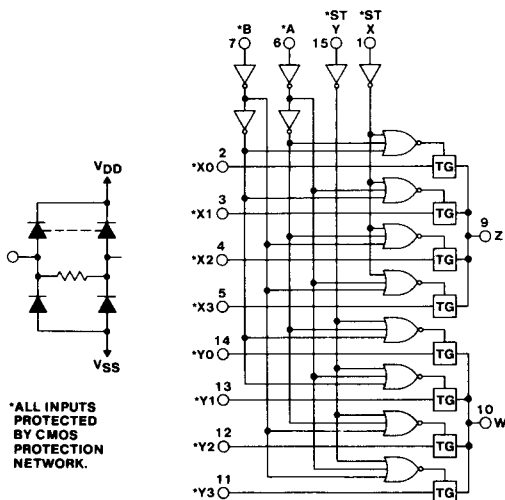
High-Voltage Types (20-Volt Rating)

#### Features:

- Wide range of digital and analog signal levels:  
Digital: 3 to 20 V  
Analog: 0 to 20 V<sub>p-p</sub>
- Low ON-state resistance:  
120 Ω typ. at 15 V
- Break-Before-Make switching eliminates channel overlap
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at V<sub>DD</sub>=5 V  
2 V at V<sub>DD</sub>=10 V  
2.5 V at V<sub>DD</sub>=15 V
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4529B CMOS dual 4-channel analog data selector consists of digitally controlled analog switches having low on-impedance and very low off-leakage current. The CD4529B is bidirectional and can also be used in digital applications. By tying Z and W together the device can be used as a single 8-channel analog data selector.

The CD4529B device is supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line package (E suffix), and in chip form (H suffix).



#### LOGIC DIAGRAM

92CM-39301

Fig. 1 - Schematic and logic diagram.

## CD4529B Types

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	..... -0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal)	..... -0.5V to $V_{DD} + 0.5V$
INPUT VOLTAGE RANGE, ALL INPUTS	..... $\pm 10mA$
DC INPUT CURRENT, ANY ONE INPUT	..... 500mW
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	..... Derate Linearity at 12mW/°C to 200mW
For $T_A = -55^\circ C$ to $+100^\circ C$	
For $T_A = +100^\circ C$ to $+125^\circ C$	
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	..... 100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	..... $-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	..... $-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79mm$ ) from case for 10s max	..... $+265^\circ C$

### RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ C$ (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

CHARACTERISTIC	$V_{DD}$	Min.	Max.	UNITS
Supply-Voltage Range ( $T_A =$ Full Package-Temperature Range)	—	3	18	V
Multiplexer Switch Input Current Capability*	—	—	25	mA
Output Load Resistance	—	100	—	$\Omega$

\* In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch

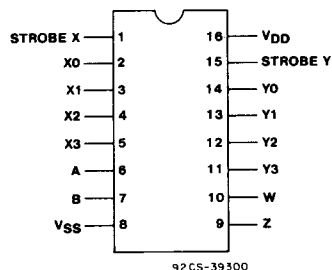
must not exceed 0.8 volt (calculated from  $R_{ON}$  values shown in Electrical Characteristics Chart). No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminals 9 and 10 (Z and W, respectively).

### TRUTH TABLE

INPUT				OUTPUT	
STROBE X	STROBE Y	B	A	Z	W
1	1	0	0	X0	Y0
1	1	0	1	X1	Y1
1	1	1	0	X2	Y2
1	1	1	1	X3	Y3
1	0	0	0	X0	
1	0	0	1	X1	
1	0	1	0	X2	
1	0	1	1	X3	
0	1	0	0	Y0	
0	1	0	1	Y1	
0	1	1	0	Y2	
0	1	1	1	Y3	
0	0	*	*	High Impedance	

Dual 4-Channel Mode  
(2 Outputs)

Single 8-Channel Mode  
(1 Output: Z and W  
tied together)



### TERMINAL ASSIGNMENT

\* = Don't Care

# CD4529B Types

## ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS	LIMITS AT INDICATED TEMPERATURES (°C)									UNITS		
		VSS (V)	VDD (V)	-55	-40	+85	+125	+25					
								Min.	Typ.	Max.			
SIGNAL INPUTS (VIN) AND OUTPUTS (VOUT)													
Quiescent Device Current, IDD Max.			5	5	5	150	150	—	0.04	5	μA		
			10	10	10	300	300	—	0.04	10			
			15	20	20	600	600	—	0.04	20			
			20	100	100	3000	3000	—	0.08	100			
On-State Resistance 0 ≤ VIN ≤ VDD ION Max.			-5	5	400	410	560	640	—	240	480	Ω	
			-7.5	7.5	240	250	350	400	—	135	270		
			0	5	800	850	1200	1300	—	470	1050		
			0	10	400	410	560	640	—	240	480		
			0	15	250	250	350	400	—	135	270		
Change in On-State Resistance (Between Any Two Channels) ΔION			0	5	—	—	—	—	15	—	Ω		
			0	10	—	—	—	—	10	—			
			0	15	—	—	—	—	5	—			
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.			0	18	±100*		±1000*		—	±0.01	±100*	nA	
Capacitance: Input, CIN Output, COUT Feedthrough, CIOS			-5	5	—	—	—	—	—	5	—	pF	
					—	—	—	—	—	18	—		
					—	—	—	—	—	0.2	—		
Propagation Delay Time (Signal Input to Output) (tPHL,tPLH)	VSS=0, RL=1 kΩ, CL=50 pF, VIN=VDD-VSS (Square Wave), tr,tr=20 ns	0	5	—	—	—	—	—	20	40	ns		
			10	—	—	—	—	—	10	20			
			15	—	—	—	—	—	8	15			
CONTROL (ADDRESS OR STROBE) VC													
Input Low Voltage, VILC Max.	VIN=VDD, RL=1 kΩ to VSS  fis < 2 μA on all OFF Channels		5	1.5				—	—	1.5	V		
			10	3				—	—	3			
			15	4				—	—	4			
Input High Voltage, VIHc Min.			5	3.5				3.5	—	—			
			10	7				7	—	—			
			15	11				11	—	—			
Input Current, IIN Max.	VIN=0, 18		18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA		
Propagation Delay Time: Control to Signal OUT (tPHL, tPLH)	tr,tr=20 ns, RL=1 kΩ, CL=50 pF, VIN=VDD-VSS (Square Wave)		5	—	—	—	—	—	200	400	ns		
			10	—	—	—	—	—	80	160			
			15	—	—	—	—	—	60	120			
Input Capacitance, CIN (Any Address or Strobe Input)			—	—	—	—	—	—	5	7.5	pF		

\*Determined by minimum feasible leakage measurement for automatic testing.

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

## CD4529B Types

### ELECTRICAL CHARACTERISTICS (Cont'd) at $T_A = 25^\circ\text{C}$

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		$V_{DD}$	Min.	Typ.	Max.	
Crosstalk Voltage, Control to Output	$R_L = 1\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , $R_{OUT} = 10\text{ k}\Omega$	5 10 15	— — —	5 5 5	— — —	mV
Maximum Control Input Pulse Frequency	$R_L = 1\text{ k}\Omega$ , $C_L = 50\text{ pF}$	5 10 15	— — —	5 10 12	— — —	MHz
Noise Voltage	$f = 100\text{ Hz}$	5 10 15	— — —	24 25 30	— — —	$\frac{\text{nV}}{\sqrt{\text{cycle}}}$
		5 10 15	— — —	12 12 15	— — —	
		5 10 15	— — —	12 12 15	— — —	
	$f = 100\text{ kHz}$	5 10 15	— — —	12 12 15	— — —	
Sine Wave Distortion	$V_{IN} = 1.77\text{ V dc (RMS)}$ centered at 0 V dc, $R_L = 10\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $V_{SS} = -5\text{ V}$	5	—	0.36	—	%
Insertion Loss	$V_{IN} = 1.77\text{ V dc (RMS)}$ centered at 0 V dc, $f = 1\text{ MHz}$ , $V_{SS} = -5\text{ V}$ , $I_{LOSS} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$ $R = 1\text{ k}\Omega$ $R = 10\text{ k}\Omega$ $R = 100\text{ k}\Omega$ $R = 1\text{ M}\Omega$	5	—	2	—	dB
			—	0.8	—	
			—	0.25	—	
			—	0.01	—	
Bandwidth (-3 dB)	$V_{IN} = 1.77\text{ V dc (RMS)}$ centered at 0 V dc, $V_{SS} = -5\text{ V}$ $R = 1\text{ k}\Omega$ $R = 10\text{ k}\Omega$ $R = 100\text{ k}\Omega$ $R = 1\text{ M}\Omega$	5	—	35	—	MHz
			—	28	—	
			—	27	—	
			—	26	—	
Feedthrough and Crosstalk	$V_{SS} = -5\text{ V}$ $20 \log_{10} \frac{V_{OUT}}{V_{IN}} = -50\text{ dB}$ $R = 1\text{ k}\Omega$ $R = 10\text{ k}\Omega$ $R = 100\text{ k}\Omega$ $R = 1\text{ M}\Omega$	5	—	850	—	kHz
			—	100	—	
			—	12	—	
			—	1.5	—	

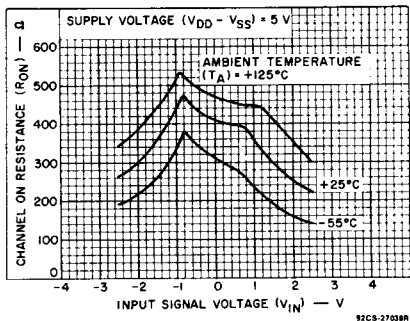


Fig. 2 - Typical channel ON resistance vs. input signal voltage.

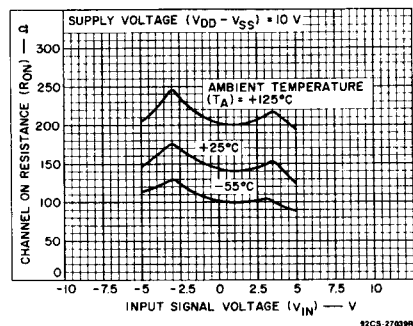


Fig. 3 - Typical channel ON resistance vs. input signal voltage.

## CD4529B Types

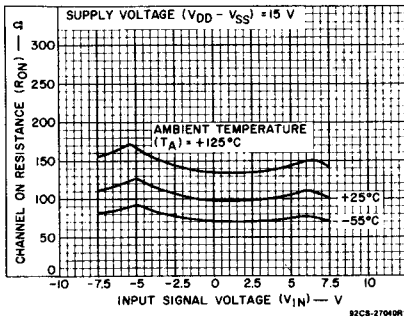


Fig. 4 - Typical channel ON resistance vs. input signal voltage.

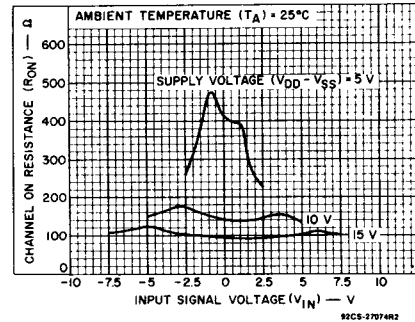


Fig. 5 - Typical channel ON resistance vs. input signal voltage.

### TEST CIRCUITS

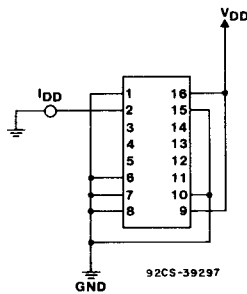


Fig. 6 - OFF channel leakage current-any channel OFF.

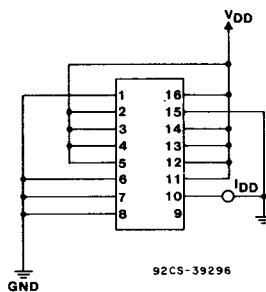


Fig. 7 - OFF channel leakage current, all channels OFF.

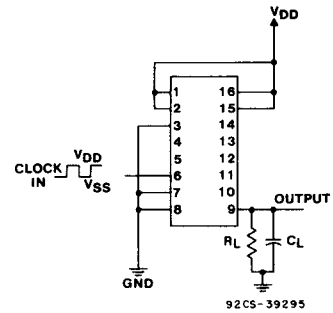


Fig. 8 - Propagation delay address input to signal output.

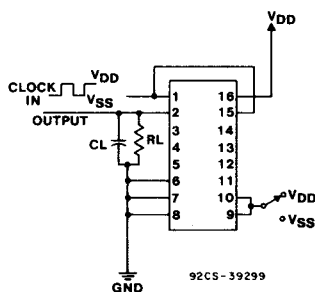


Fig. 9 - Propagation delay-strobe input to signal output.

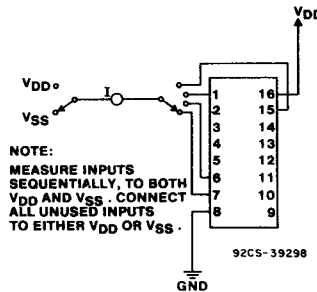


Fig. 10 - Quiescent device current.

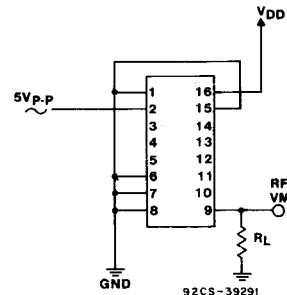
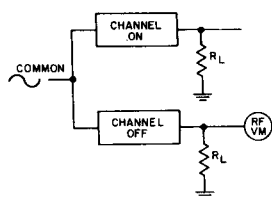


Fig. 11 - Feedthrough.

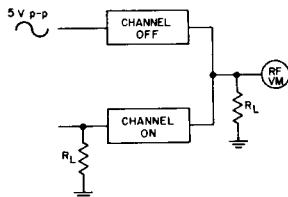
## CD4529B Types

### TEST CIRCUITS (Cont'd)



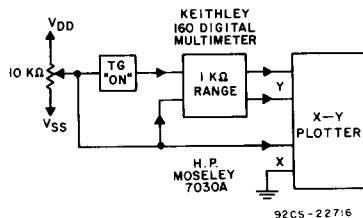
92CS-27050

Fig. 12 - Crosstalk between any two channels.



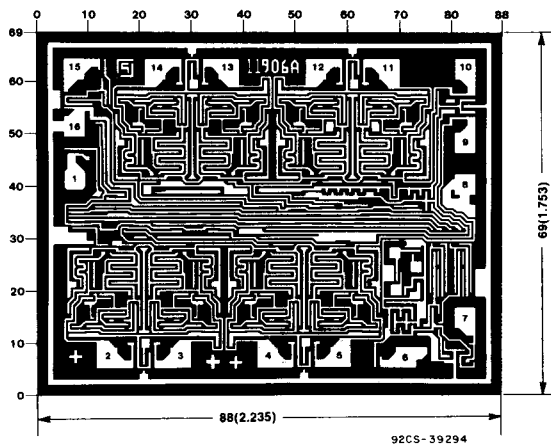
92CS-27051

Fig. 13 - Crosstalk between sections.



92CS-22716

Fig. 14 - Channel ON resistance measurement circuit.



Dimensions and pad layout for CD4529B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).