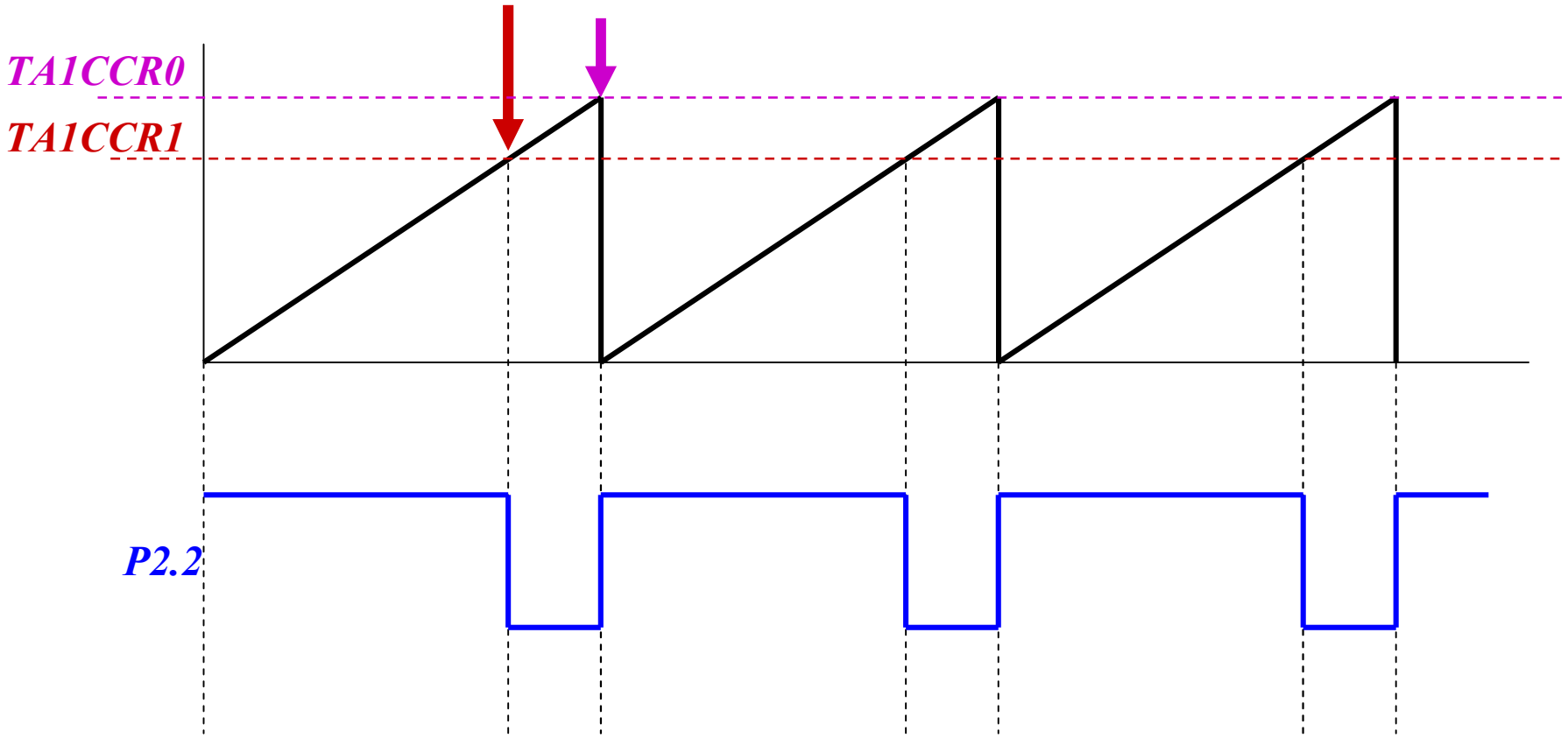
Exercício: **Escrever um programa para controlar um motor DC através de PWM.**

- **Utilizar o *ADC* para controlar a velocidade do motor**
- **Utilizar o *Timer1_A* para gerar o PWM;**
- **Inverter o sentido de rotação do motor quando a interrupção do pino *P1.3* for ativada;**

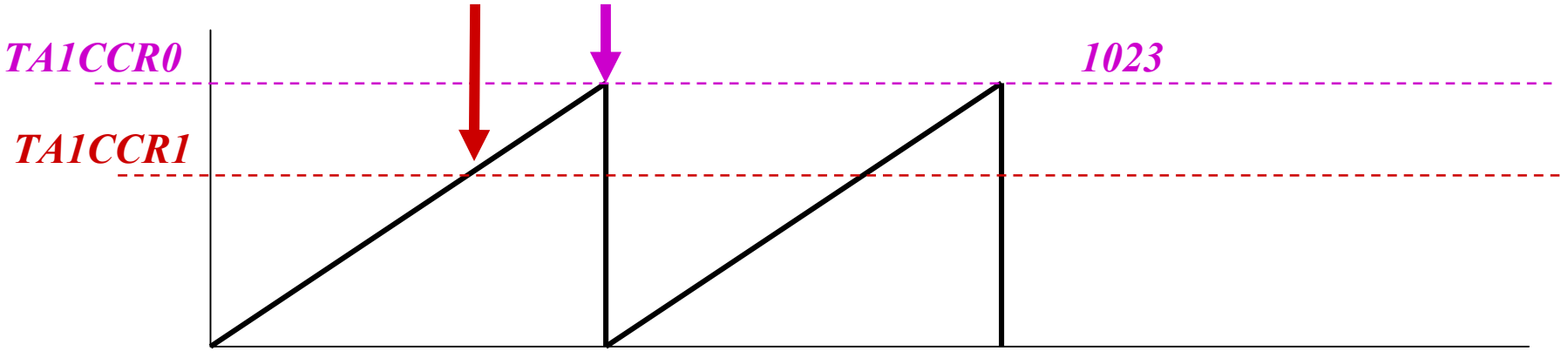
•Interrupção do pino *P1.3* ativada na borda de descida

•Frequência do *DCO* = 16MHz

Geração de *PWM* através do *Timer1_A – UP Mode*



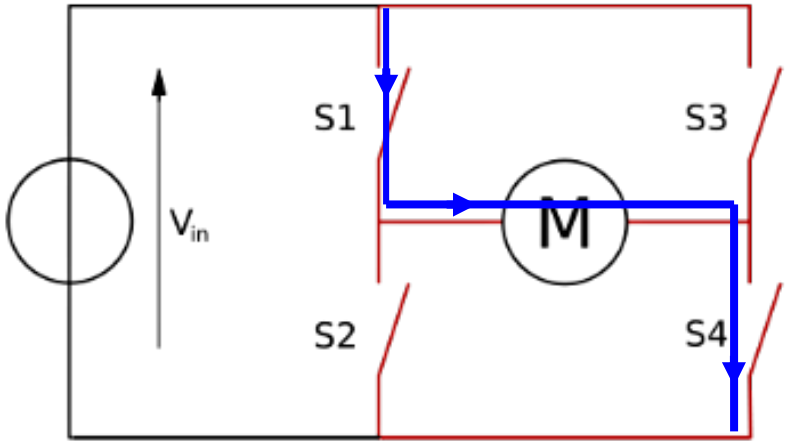
Geração de *PWM* através do *Timer1_A – UP Mode*

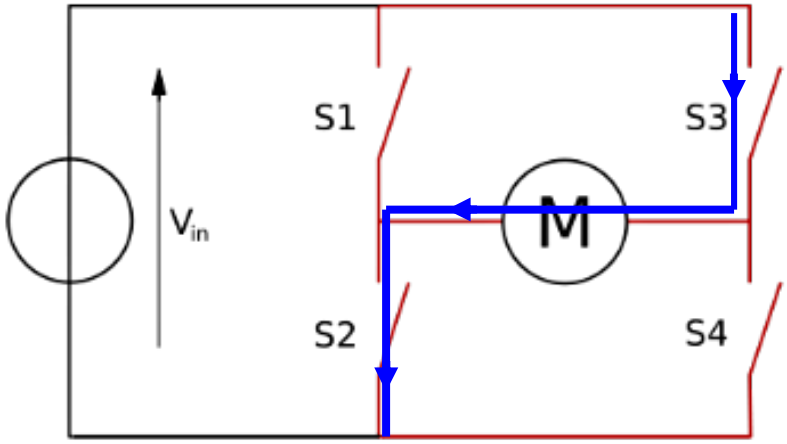


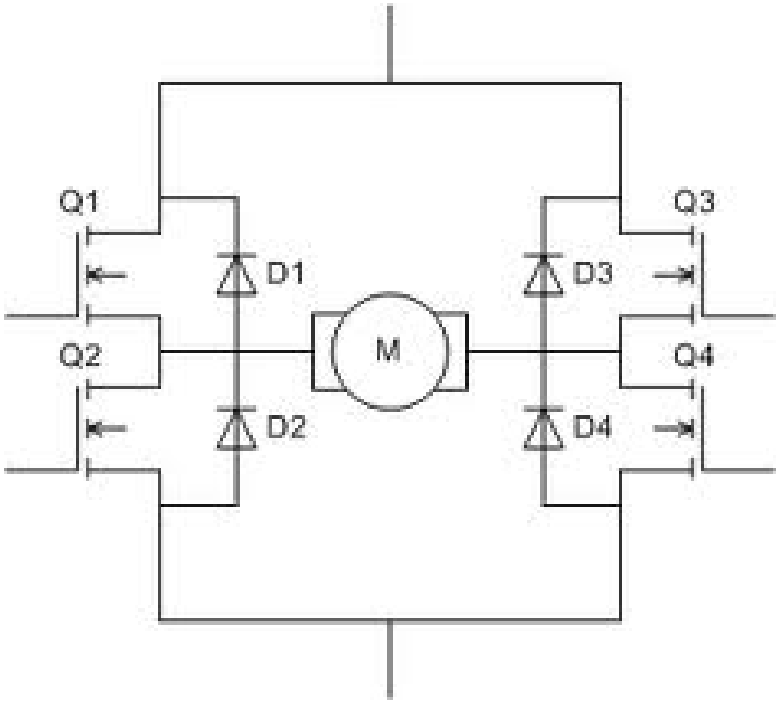
***TA1CCR1*: Utilizar o valor lido do canal 5 ADC, com referência Vcc**

Iniciar uma conversão do ADC à cada 10ms, através da saída OUT0 do Timer0_A

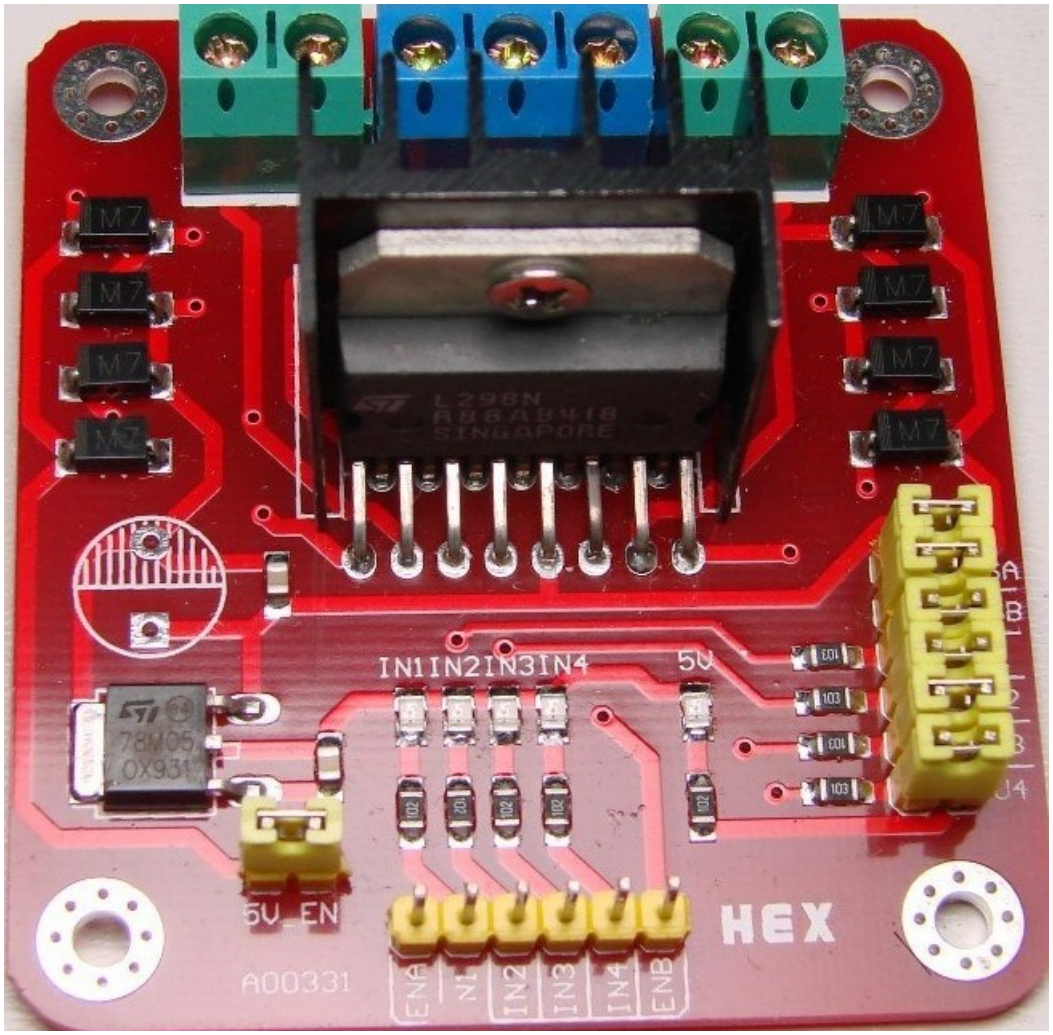
Ponte H para controle de motor DC



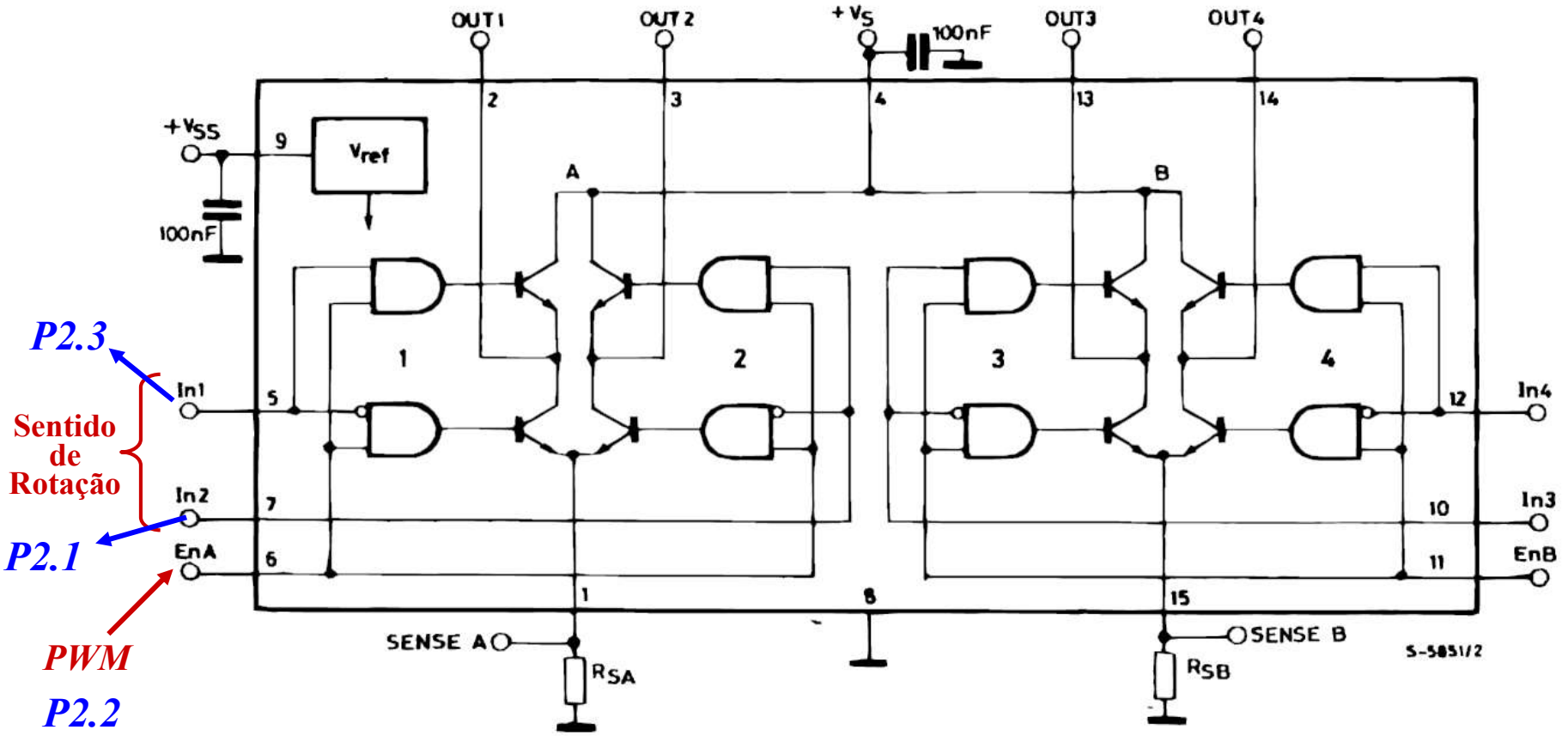




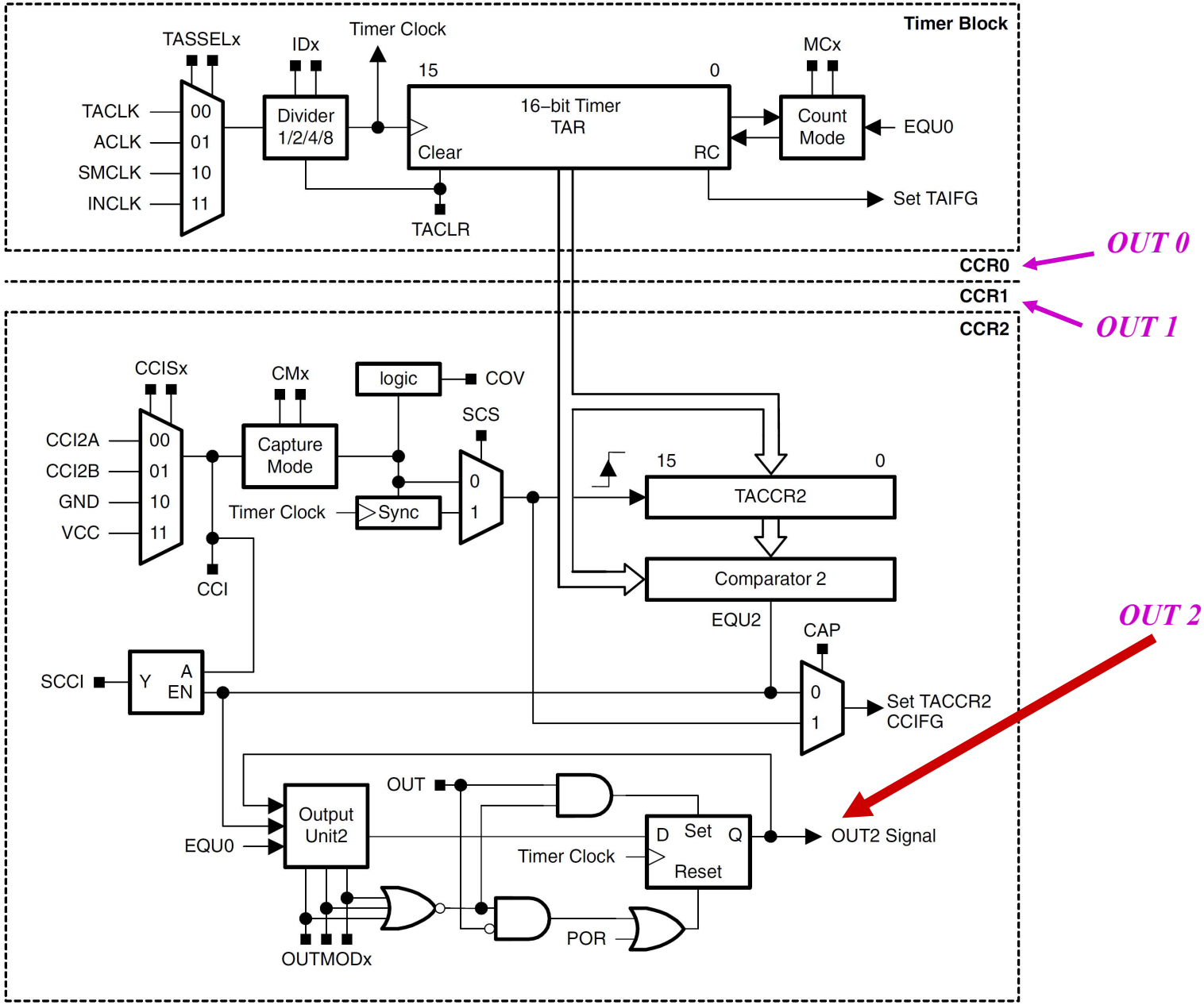
Placa para Controlar o Motor DC



L298 - DUAL FULL-BRIDGE DRIVER

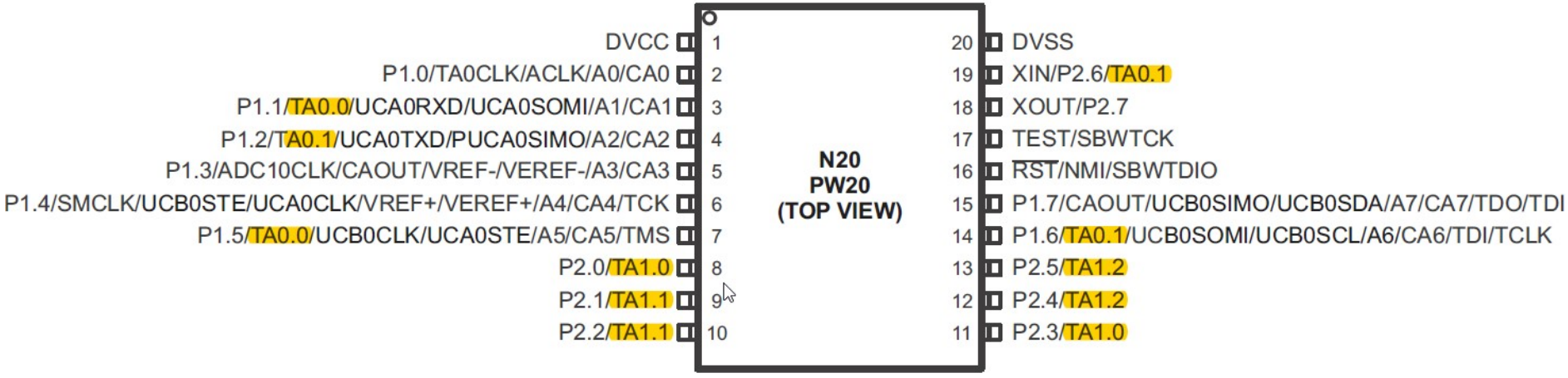


C: *Exercício 19*

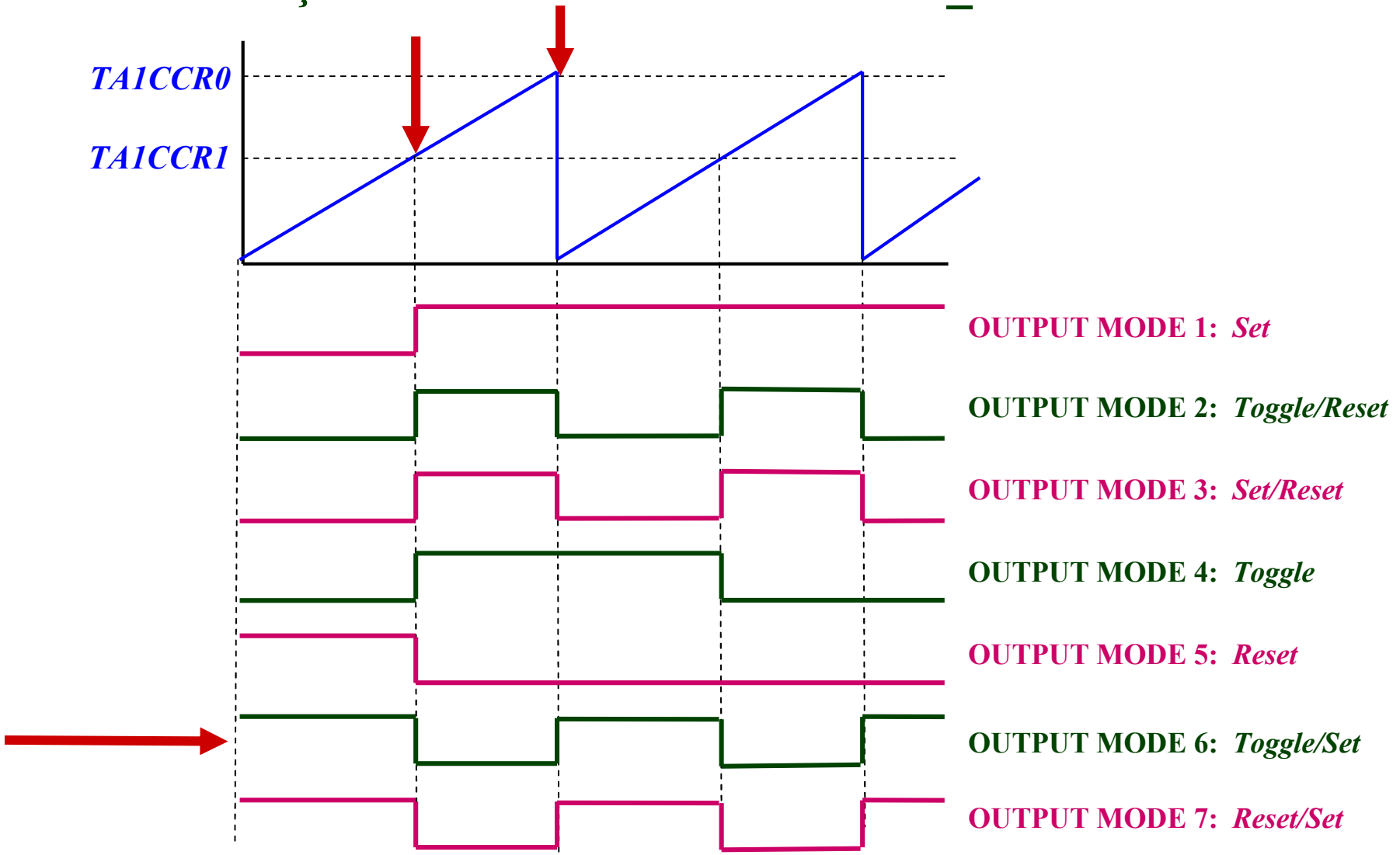


Pinos Utilizados

In1:	*P2.3*
In2:	*P2.1*
Enable_A:	*P2.2 (TA1.1)*



Geração de *PWM* através do *Timer1_A* – *UP Mode*



Funções do Pinos da Porta 2

P2.0/ TA1.0	8	10	9	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI0A input, compare: Out0 output
P2.1/ TA1.1	9	11	10	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI1A input, compare: Out1 output
P2.2/ TA1.1	10	12	11	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI1B input, compare: Out1 output
P2.3/ TA1.0	11	16	15	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI0B input, compare: Out0 output
P2.4/ TA1.2	12	17	16	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI2A input, compare: Out2 output
P2.5/ TA1.2	13	18	17	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI2B input, compare: Out2 output
XIN/ P2.6/ TA0.1	19	27	26	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer0_A, compare: Out1 output
XOUT/ P2.7	18	26	25	I/O	Output terminal of crystal oscillator(3) General-purpose digital I/O pin

Table 20. Port P2 (P2.0 to P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]		
			P2DIR.x	P2SEL.x	P2SEL2.x
P2.0/	0	P2.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.CCI0A	0	1	0
		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.1/	1	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1A	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.2/	2	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1B	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.3/	3	P2.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.CCI0B	0	1	0
		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.4/	4	P2.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.CCI2A	0	1	0
		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.5/	5	P2.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.CCI2B	0	1	0
		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1

TACTL, Timer_A Control Register *TA1CTL*

15	14	13	12	11	10	9	8
Unused						TASSELx	
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

7	6	5	4	3	2	1	0
IDx		MCx		Unused	TACLR	TAIE	TAIFG
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	w–(0)	rw–(0)	rw–(0)

Unused Bits 15-10 Unused

TASSELx Bits 9-8 Timer_A clock source select
- 00 TACLK
- 01 ACLK
- 10 SMCLK
- 11 INCLK

IDx Bits Input divider. These bits select the divider for the input clock.
- 00 /1
- 01 /2
- 10 /4
- 11 /8

MCx Bits 5-4 Mode control. Setting MCx = 00h when Timer_A is not in use conserves power.
- 00 Stop mode: the timer is halted.
- 01 Up mode: the timer counts up to TACCR0.
- 10 Continuous mode: the timer counts up to 0FFFFh.
- 11 Up/down mode: the timer counts up to TACCR0 then down to 0000h.

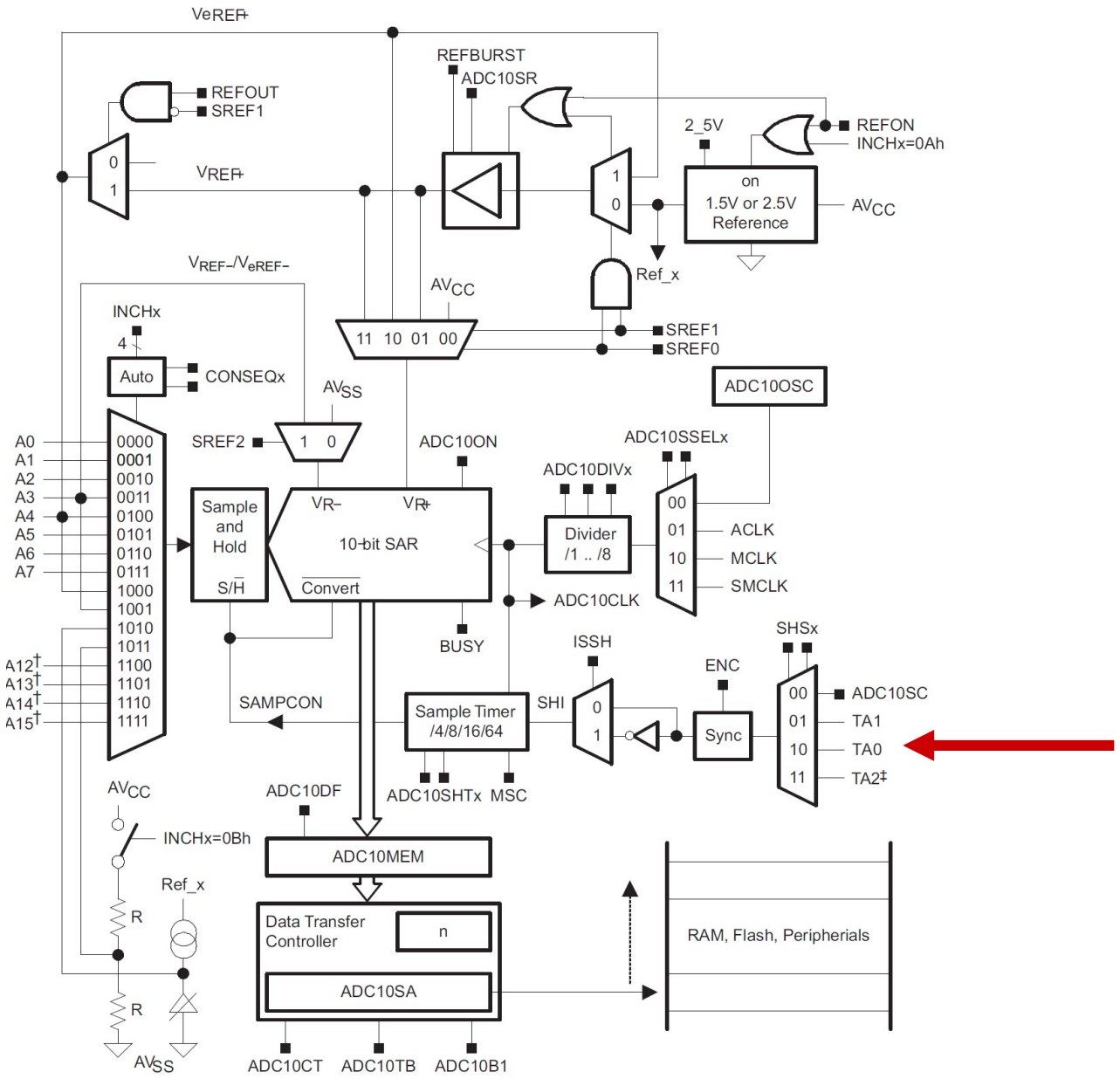
TACCTLx, Capture/Compare Control Register *TA1CCTL1*

15	14	13	12	11	10	9	8
CMx		CCISx		SCS	SCCI	Unused	CAP
rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	r	r0	rw–(0)

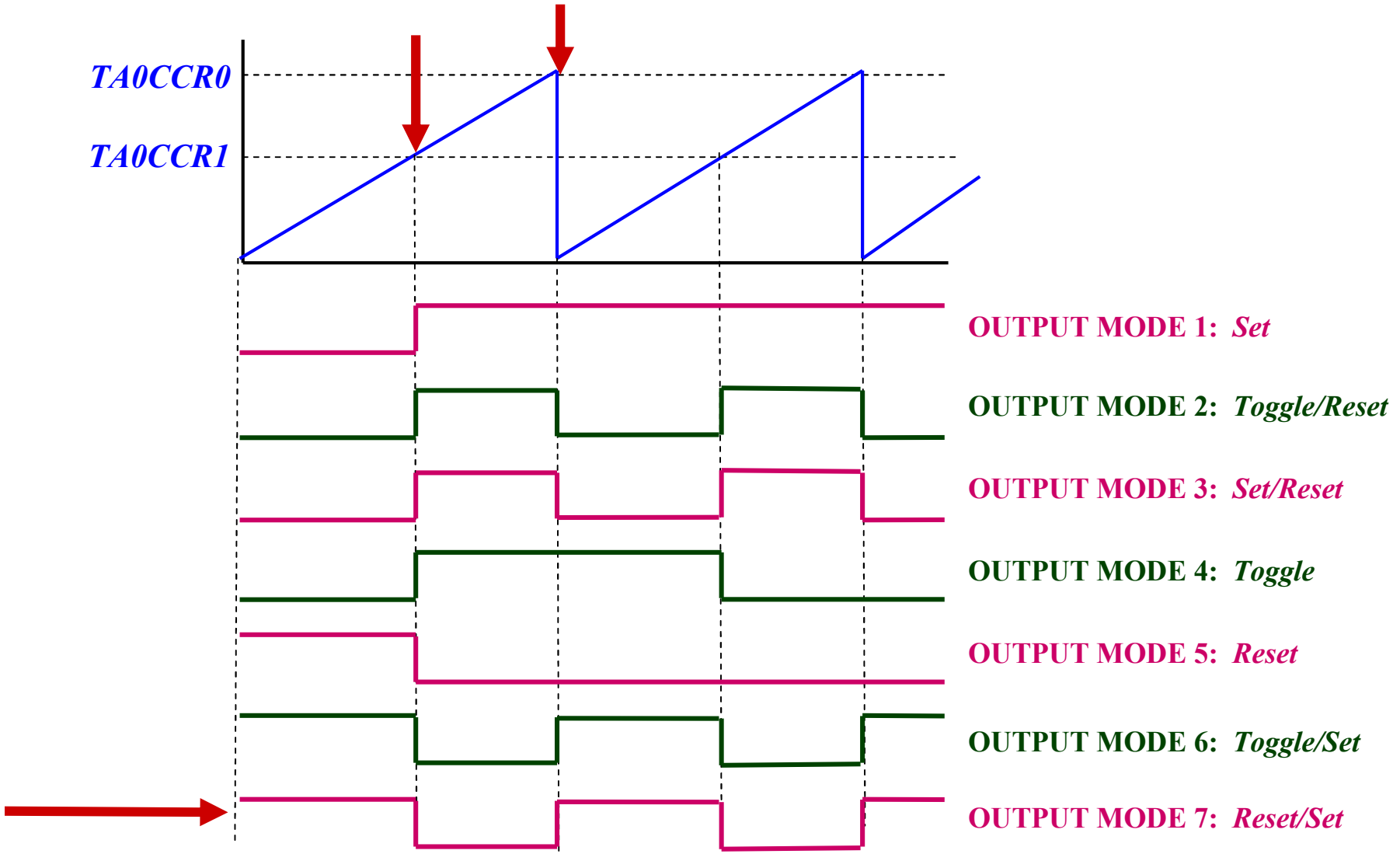
7	6	5	4	3	2	1	0
OUTMODx			CCIE	CCI	OUT	COV	CCIFG
rw–(0)	rw–(0)	rw–(0)	rw–(0)	r	rw–(0)	rw–(0)	rw–(0)

OUTMODx Bits 7-5 Output mode. Modes 2, 3, 6, and 7 are not useful for TACCR0 because EQUx = EQU0.

000 OUT bit value
001 Set
010 Toggle/reset
011 Set/reset
100 Toggle
101 Reset
110 Toggle/set
111 Reset/set


VeREF+
REFBURST
ADC10SR
REFOUT
SREF1
VREF+
2_5V
REFON
INCHx=0Ah
on
1.5V or 2.5V
Reference
AVCC
Ref_x
VREF-/VeREF-
INCHx
4
Auto
CONSEQx
AVSS
11 10 01 00
SREF1
SREF0
ADC10OSC
SREF2
1 0
ADC10ON
ADC10SSELx
ADC10DIVx
A0
A1
A2
A3
A4
A5
A6
A7
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
A12†
A13†
A14†
A15†
Sample
and
Hold
S/H
VR-
VR+
10-bit SAR
Convert
Divider
/1 .. /8
00
01
10
11
ACLK
MCLK
SMCLK
ADC10CLK
BUSY
ISSH
SHSx
ENC
SAMPCON
Sample Timer
/4/8/16/64
SHI
Sync
ADC10SC
TA1
TA0
TA2‡
ADC10SHTx
MSC
AVCC
ADC10DF
INCHx=0Bh
ADC10MEM
Ref_x
R
Data Transfer
Controller
n
RAM, Flash, Peripherials
ADC10SA
R
AVSS
ADC10CT
ADC10TB
ADC10B1

Início da conversão do *ADC* através do *Timer0_A – OUT0*



22.3.2 ADC10CTL1, ADC10 Control Register 1

15	14	13	12	11	10	9	8
INCHx				**SHSx**		**ADC10DF**	**ISSH**
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC10DIVx			**ADC10SSELx**		**CONSEQx**		**ADC10BUSY**
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-0

Can be modified only when ENC = 0

SHSx Bits 11-10 Sample-and-hold source select

- 00 ADC10SC bit
- 01 Timer_A.OUT1
- 10 Timer_A.OUT0
- 11 Timer_A.OUT2 (Timer_A.OUT1 on MSP430x20x2 devices)

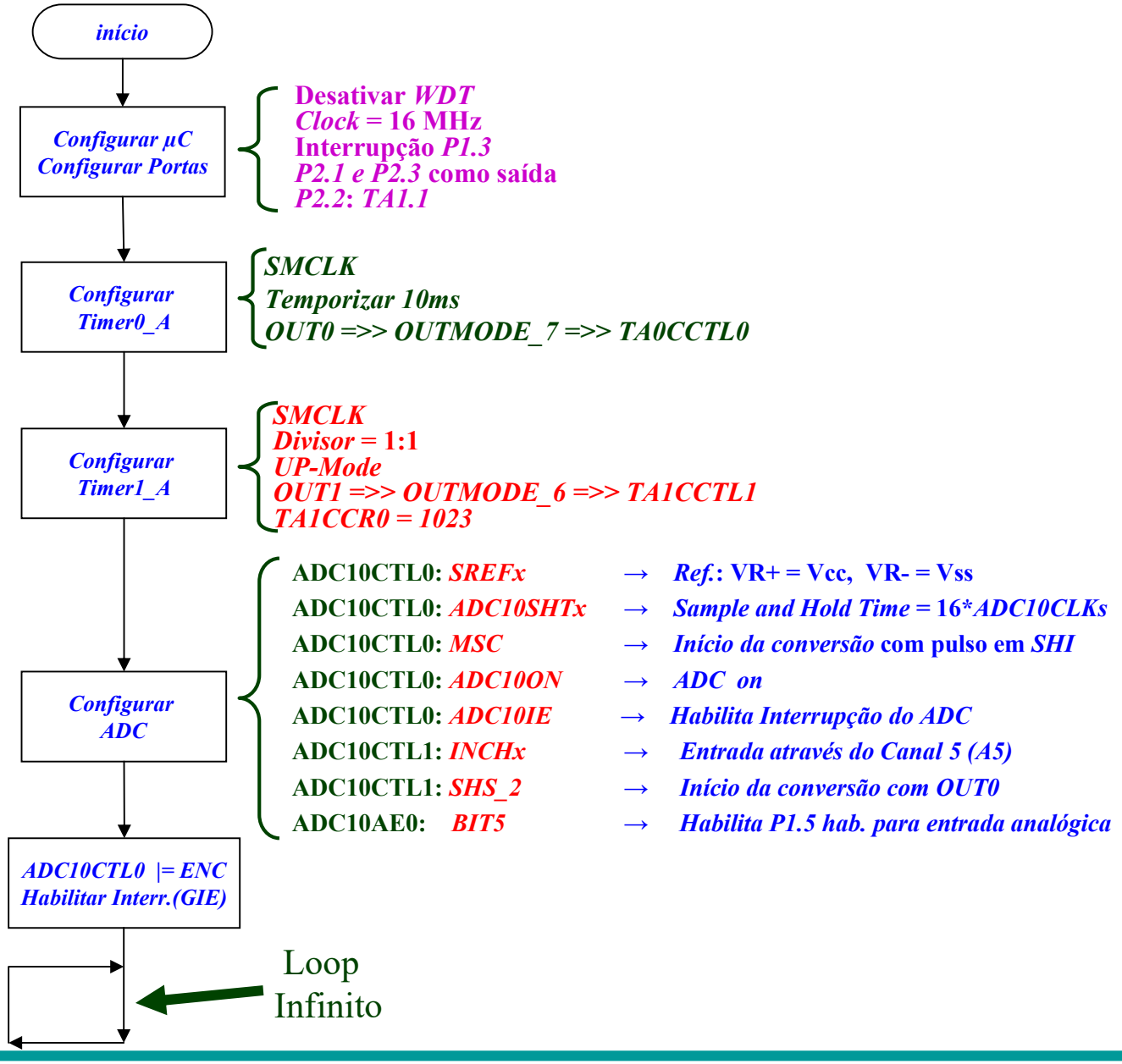
ADC10DF Bit 9 ADC10 data format

- 0 Straight binary
- 1 2s complement

ISSH Bit 8 Invert signal sample-and-hold

- 0 The sample-input signal is not inverted.
- 1 The sample-input signal is inverted.

C: *Exercício 19*



Rotinas de Interrupção