Exercício 09:
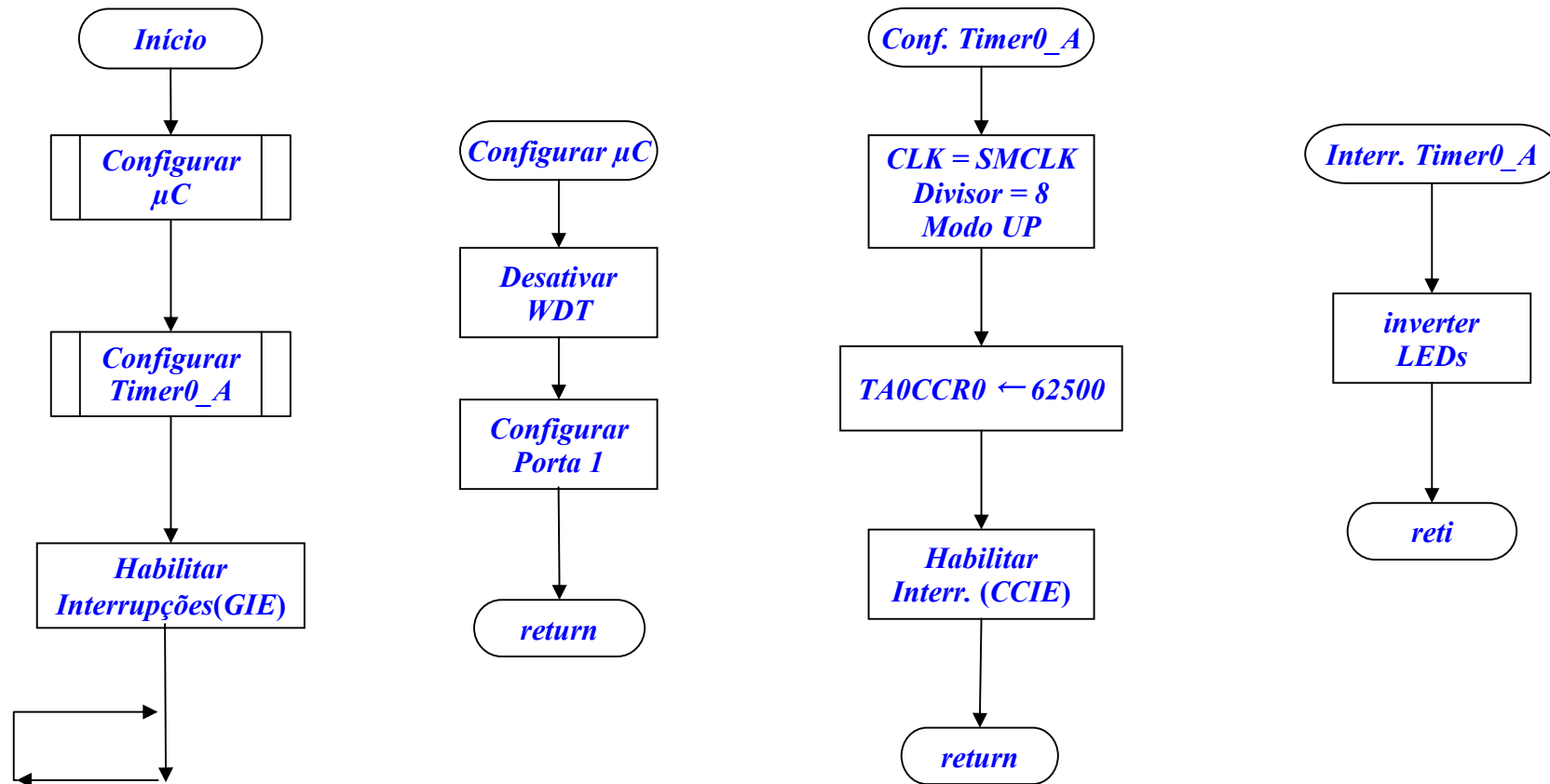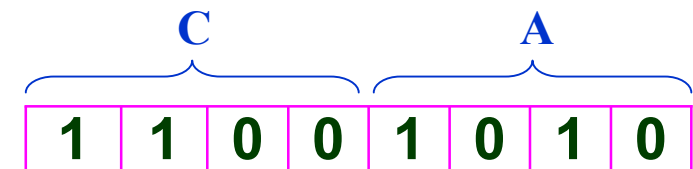
- **Escrever um programa para alternar o estado dos LEDs vermelho e verde da placa MSP-EXP430G2 a cada 500.000 ciclos de *clock*.**

- **Utilizar o *Timer0_A* para a temporização.**
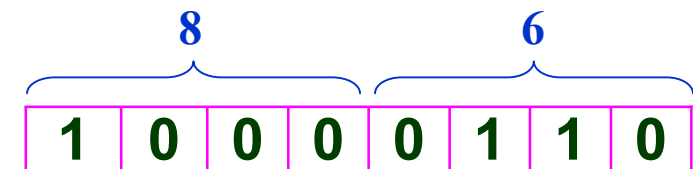
Início

Configurar µC

Configurar Timer0_A

Habilitar Interrupções(GIE)

Configurar µC

Desativar WDT

Configurar Porta 1

return

Conf. Timer0_A

CLK = SMCLK Divisor = 8 Modo UP

TA0CCR0 ← 62500

Habilitar Interr. (CCIE)

return

Interr. Timer0_A

inverter LEDs

reti

Configuração do µC:

mov.b   **#0*x*CA, &DCOCTL**

mov.b   **#0*x*86, &BCSCTL1**

	C			A			
1	1	0	0	1	0	1	0

DCOCTL

	8			6			
1	0	0	0	0	1	1	0

BCSCTL1

Configuração do Microcontrolador:

```
//mov.b      #0xCA,  &DCOCTL
//mov.b      #0x86,  &BCSCTL1

mov.b       &0x10FE,  &DCOCTL
mov.b       &0x10FF,  &BCSCTL1

mov.b       &0x10FC,  &DCOCTL
mov.b       &0x10FD,  &BCSCTL1

mov.b       &0x10FA,  &DCOCTL
mov.b       &0x10FB,  &BCSCTL1

mov.b       &0x10F8,  &DCOCTL
mov.b       &0x10F9,  &BCSCTL1
```
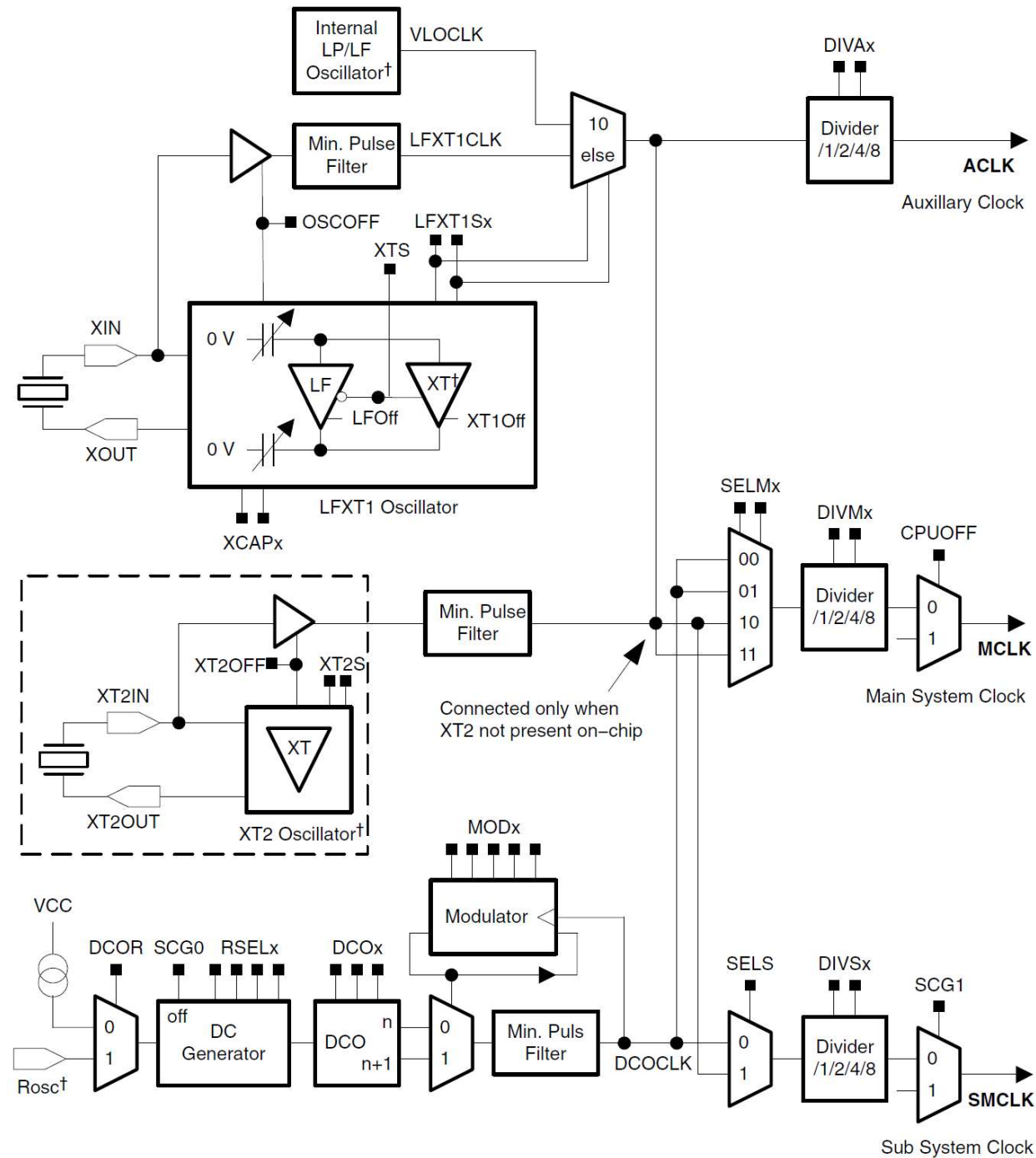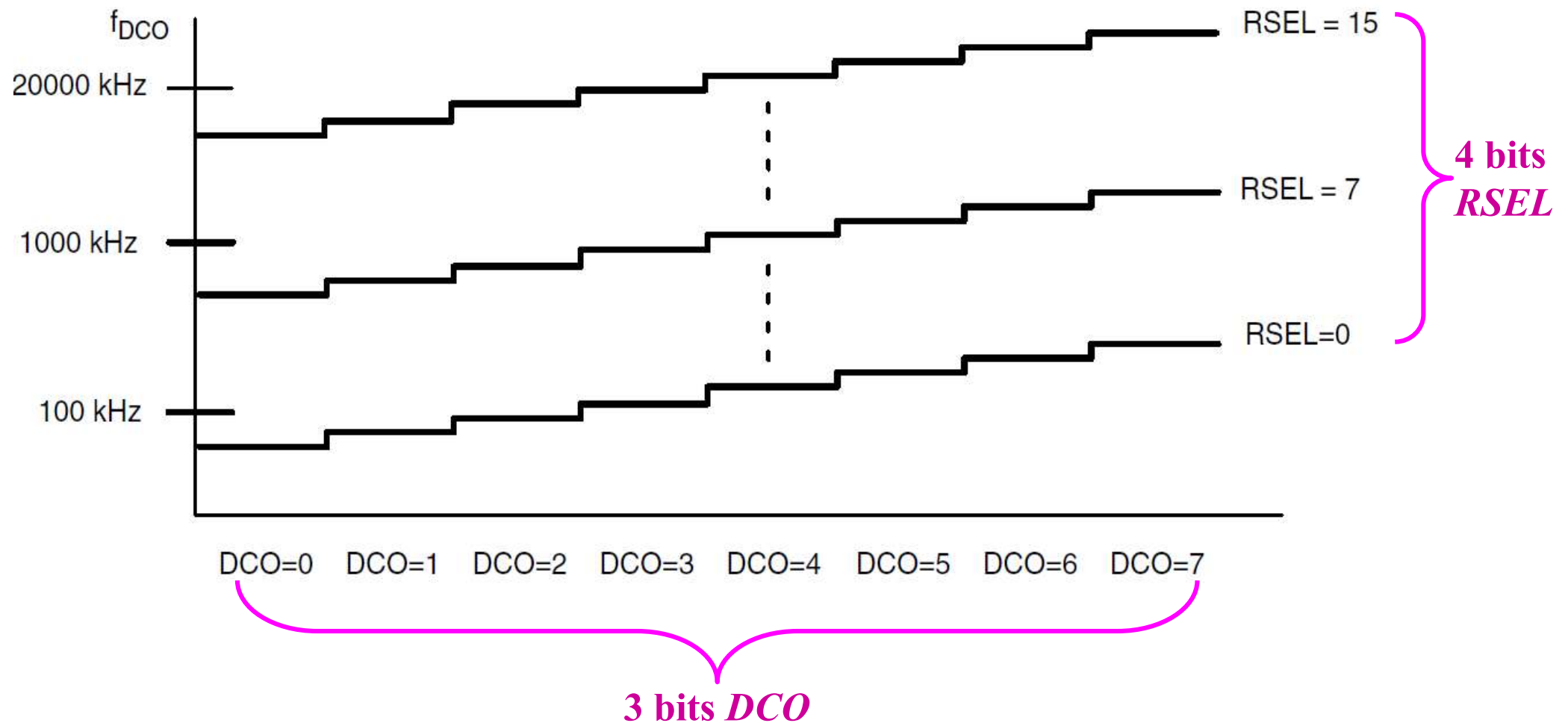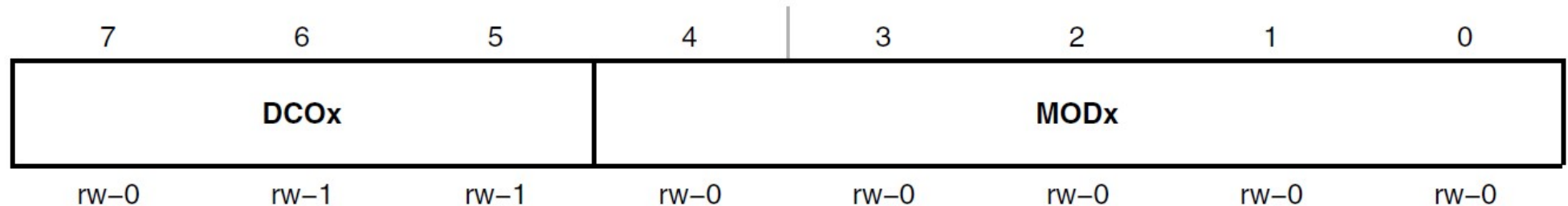
Executar o programa com cada uma das configurações acima

Configuração do *DCO*

DCOCTL, DCO Control Register

7	6	5	4	3	2	1	0
	DCOx				MODx		
rw–0	rw–1	rw–1	rw–0	rw–0	rw–0	rw–0	rw–0

DCOx   Bits 7-5   DCO frequency select. These bits select which of the eight discrete DCO frequencies within the range defined by the RSELx setting is selected.

MODx   Bits 4-0   Modulator selection. These bits define how often the f_{DCO+1} frequency is used within a period of 32 DCOCLK cycles. During the remaining clock cycles (32–MOD) the f_{DCO} frequency is used. Not useable when DCOx=7.

BCSCTL1, Basic Clock System Control Register 1

7	6	5	4	3	2	1	0
XT2OFF	XTS†	DIVAx		RSELx			
rw–(1)	rw–(0)	rw–(0)	rw–(0)	rw–0	rw–1	rw–1	rw–1

† XTS = 1 is not supported in MSP430x20xx devices.

XT2OFF Bit 7 XT2 off. This bit turns off the XT2 oscillator
   0   XT2 is on
   1   XT2 is off if it is not used for MCLK or SMCLK.

XTS Bit 6 LFXT1 mode select.
   0   Low frequency mode
   1   High frequency mode

DIVAx Bits 5-4 Divider for ACLK
   00   /1
   01   /2
   10   /4
   11   /8

RSELx Bits 3-0 Range Select. Sixteen different frequency ranges are available. The lowest frequency range is selected by setting RSELx=0. RSEL3 is ignored when DCOR = 1.

	0	DCO0	DCO1	DCO1 + DCO0	DCO2	DCO2 + DCO0	DCO2 + DCO1	DCO2 + DCO1 + DCO0
0	94.9	101.0	108.1	116.2	125.6	136.7	149.9	166.0
RSEL0	118.1	125.8	134.5	144.6	156.4	170.1	186.6	206.5
RSEL1	166.6	177.4	189.7	203.8	220.2	239.6	262.7	290.7
RSEL1 + RSEL0	232.1	247.2	264.3	283.9	306.8	333.8	365.8	404.8
RSEL2	326.5	347.7	371.7	399.3	431.1	468.8	513.5	567.8
RSEL2 + RSEL0	465.0	497.8	528.8	567.6	612.8	665.5	728.9	805.8
RSEL2 + RSEL1	650.1	691.5	738.5	792.4	855.1	927.5	1015.1	1121.4
RSEL2 + RSEL1 + RSEL0	921.6	980.2	1046.1	1121.1	1209.3	1310.3	1433.0	1581.1
RSEL3	1308.5	1390.7	1483.5	1588.5	1712.0	1852.8	2023.4	2229.9
RSEL3 + RSEL0	1871.1	1986.2	2116.6	2263.4	2436.6	2634.8	2874.5	3165.0
RSEL3 + RSEL1	2698.8	2861.8	3046.5	3252.6	3497.6	3776.8	4114.9	4529.0
RSEL3 + RSEL1 + RSEL0	3413.7	3623.8	3862.5	4129.0	4446.5	4812.9	5255.0	5786.7
RSEL3 + RSEL2	4629.0	4910.4	5229.8	5579.2	5994.8	6501.5	7121.3	7796.6
RSEL3 + RSEL2 + RSEL0	6281.3	6678.6	7118.2	7564.9	8056.5	8640.2	9469.0	10522.0
RSEL3 + RSEL2 + RSEL1	8917.6	9499.4	10187.0	10928.9	11788.0	12680.8	13824.4	15197.5
RSEL3 + RSEL2 + RSEL1 + RSEL0	12584.2	13266.5	14093.8	14939.9	15895.6	16915.7	18199.7	20405.3

MSP430G2553.h :

#define CALDCO_16MHZ_   (0x10F8u) /* DCOCTL Calibration Data for 16MHz */

#define CALBC1_16MHZ_   (0x10F9u) /* BCSCTL1 Calibration Data for 16MHz */

#define CALDCO_12MHZ_   (0x10FAu) /* DCOCTL Calibration Data for 12MHz*/

#define CALBC1_12MHZ_   (0x10FBu) /* BCSCTL1 Calibration Data for 12MHz */

#define CALDCO_8MHZ_   (0x10FCu) /* DCOCTL Calibration Data for 8MHz */

#define CALBC1_8MHZ_   (0x10FDu) /* BCSCTL1 Calibration Data for 8MHz */

#define CALDCO_1MHZ_   (0x10FEu) /* DCOCTL Calibration Data for 1MHz */

#define CALBC1_1MHZ_   (0x10FFu) /* BCSCTL1 Calibration Data for 1MHz */

CONFIGURAÇÃO DO DCO:

mov.b   &CALDCO_xMHZ, &DCOCTL;

mov.b   &CALBC1_xMHZ,   &BCSCTL1