FYP: Weekly Progress Report 3

Group members:

- Imad Al Assir
- Mohammad El Iskandarani
- Hadi Rayan El Sandid

Name: Imad Al Assir and Mohammad El Iskandarani

Note that since Imad and Mohammad are working together on the same tasks for now, they will have a combined report.

Our contribution to the project during the last week:
We met up several times this week to test bench the address generator in conjunction with the register file. Unmasked operations were successful but we found some trouble with masked operations in the address generator. We communicated these problems to Dr. Saghir and he is looking into a fix. We also connected the register file to the controller and started setting up the testbench. Moreover, we assisted to our first FYP meeting with Dr. Saghir on 30/09/2020, where he went over the scope and expected deliverables of our project.

Total time spent of the project this week was: 4 hours.

Our planned contribution to the project next week will be to:

- Complete testing the register file+controller subsystem.
- Fix the address generator issue with masked operations.
- Add the ALU to the register file+controller subsystem and testbench it.
- Review problems faced during EECE 499 and start solving them with Dr. Saghir.

As of today, the teamwork is: Excellent

Name: Hadi Rayan Al Sandid

My personal contribution to the project during the last week:

- I've assisted to our first FYP meeting on 30/09/2020, where Dr. Saghir went over the scope and expected deliverables of our project.
- I have started looking into the GEM5 simulator, and how it is used to simulate complete systems.
- In our FYP website, I have added a section titled 'Website Contribution' which explains in detail the software/file manipulation required for team members to upload their own documentation to the website.

Total time spent of the project this week was: 5 hours.

Our planned contribution to the project next week will be to:

- Have a running configuration of GEM5 on my personal machine, and follow tutorial on how to use the simulation tool.
- Familiarize myself with MicroBlaze and development for FPGA using Xilinx Vivado. This will be mainly done with the help of team member Imad Al Assir, which has experience in those fields.

As of today, the teamwork is: Excellent

Final Year Project Meeting Minutes

Meeting #3		
Date: 9.30.2020	Time: from 12:00 to 13:00	Location: Zoom
Meeting called by	Group	
Attendees	Imad Al Assir, Hadi El Sandid, Mohammad El Iskandarani, Dr. Mazen Saghir	
Minutes taker	Imad Al Assir	

Agenda Item: Description of FYP

Discussion	**Scope of FYP**

Dr. Saghir went over the scope and the end-goal of the FYP.

Conclusions	

- Design a RISC-V vector processor as per the RISC-V Vector Extension ISA.
- Integrate the processor into a RISC-V core (sweRV core), but first into MicroBlaze.
- Build hardware on Nexys Video FPGA
- Create a model on the GEM5 simulator to simulate the complete system with cache and memory in software. Can help debug hardware issues and compare to other existing solutions
- Ideally, would be able to run ML algorithms with none to few changes.
- Benchmark using MLPerf
- Low priority: Configure accelerators and generate VHDL code through a Python script to facilitate setup.

Action Items	**Person Responsible**	**Deadline**
Finalize and test hardware of RISC-V vector processor	Imad Al Assir, Mohammad El Iskandarani	End of Fall
Support evaluation and validation of the hardware by developing APIs for MicroBlaze in software	Hadi El Sandid, Imad Al Assir	End of Fall
Migrate from MicroBlaze to RISC-V sweRV core	Hadi El Sandid, Imad Al Assir	End of Spring
Model the vector processor in GEM5	Hadi El Sandid	End of Fall
Study how to run ML algorithms on vector processor	Mohammad El Iskandarani	End of Spring
Benchmark using MLPerf	Mohammad El Iskandarani	End of Spring
Low priority: Write a Python script to configure accelerators and generate VHDL code automatically.	Hadi El Sandid	End of Spring

Agenda Item: Choice of Processor

Discussion	

Discussed which processor to use: MicroBlaze softcore processor vs RISC-V sweRV core

Conclusions	

Final Year Project Meeting Minutes

- MicroBlaze:
  - Pros: accessible, have prior experience with it.
  - Cons: vector processor does not integrate very well with it. It will be a co-processor, not autonomous (e.g. able to access memory on its own) as it should be.
- RISC-V sweRV:
  - Pros: compatibility with RISC-V Vector Processor, better integration, can use native RISC-V compiler to vectorize code.
  - Cons: no prior experience, harder to get started

Action Items	Person Responsible	Deadline
Implement platform with MicroBlaze softcore processor	Hadi El Sandid, Imad Al Assir	End of Fall
Migrate to RISC-V sweRV	Hadi El Sandid, Imad Al Assir	End of Spring

Agenda Item: Tasks for the near future

Discussion	

Discussed where we should start, what to do in the near future

Conclusions	

- Hadi should familiarize himself with MicroBlaze and development for FPGA using Xilinx Vivado, by building a simple application. Imad can help with that since he has significant experience.
- Hadi should start looking into GEM5 and get it running on his machine.
- Since Imad and Mohammad had previously started the project in EECE 499, need to revisit previously faced problems and document them. Dr. Saghir will then help solve them.
- Imad, Mohammad and Dr. Saghir should meet again to review design choices made previously (e.g. number of lanes, scheduling mechanism, ...)

Action Items	Person Responsible	Deadline
Build simple MicroBlaze application on FPGA	Hadi El Sandid	By next meeting
Setup GEM5 on personal machine and get up to speed	Hadi El Sandid	In 2 weeks
Review and report problems faced previously	Imad Al Assir, Mohammad El Iskandarani	By next meeting
Review previous design choices	Imad Al Assir, Mohammad El Iskandarani	By next meeting